17

OPERATIONS SUPPORT SYSTEMS
COMMON
SMAS 5A/B & RTS 5A
CONTROL CIRCUIT

CHANGES

D. Description of Changes

D.1 Group number information for SARTS GENERIC 2A features on PROM circuit packs CP2( ) and CP58( ) have been added.

D.2 Data set interconnection information between RTS 5A and CMS 1 have been added for the 53A test position configuration. The 53A test position is required when testing No. 4 ESS trunks. FS20 shows these data set connections. Normal operation has plug P4 EIA from RTS 5A connected to a CSU-24B EIA transfer switch which is then switched manually to a 202T data set. The 202T private line data set is used as the link to the CMS1. If this link is lost, the EIA transfer unit is switched manually to the 202S data set and the testers on the RTS and CMS 1 ends use telephone sets to establish a DDD link. When the DDD link is established using the 202S data sets, the RTS 5A and CMS 1 will again start communicating. The PL1 and PL2 relays must be de-energized for the 202T or 202S operation to work.

D.3 Note 4 has been added to Sheet B17 to clarify DDS testing when only one clock is available or testing is done in a 53A TP environment.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-LO-EGS



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# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/B & RTS 5A
# CONTROL CIRCUIT

## CHANGES

B. Changes in Apparatus (Components)

B.1 Added

Capacitors C6, C7, C8, C9, C10 have been added to CP45.

D. Description of Changes

D.1 Noise suppression capacitors have been added to CP45 logic leads to prevent -48 volt relay noise on contacts K1 through K26 from crosstalking input leads 29, 35, 36, 37, and 38. This crosstalk can set latches IC 1, 2, 11, and 12 incorrectly, which will cause an alarm condition on SMAS access. Capacitors C6 through C10, 220pF, have been connected between logic ground and pins 29, 35, 36, 37, 38 on CP45. This eliminates an alarm condition that arises when a SMAS access is done.

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D.T.SAHS



OPERATIONS SUPPORT SYSTEMS
COMMON
SMAS 5A/B & RTS 5A
CONTROL CIRCUIT

CHANGES

D. Description of Changes

D.1 A new circuit pack, CP58( ), "Auxiliary 12-K byte PROM" has been added to the system. This circuit pack is required for new features beyond GENERIC 2. An example of a new feature beyond GENERIC 2 is TERMINATE and LEAVE. CP58( ) is also required when using a 53A test position for testing No. 4 ESS trunks.

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DEPT 9232-LO-EGS



Printed in U.S.A.

# OPERATIONS SUPPORT SYSTEMS COMMON SMAC 5A/B AND RTS 5A CONTROL CIRCUIT

## CHANGES

### D. Description of Changes

D.1 CP2 generic 1 has been rated A&M since the software can no longer be supported.

D.2 Add backplane wiring, options, information notes, and new circuit packs 53, 54, and 58( ) to implement the terminate and leave function.

D.3 Add extra contacts to ENR relay circuit to increase contact life when carrying worse case current of 750 mA.

D.4 Note 216 changed to include maximum allowed length.

D.5 Pullup resistors were added to CP4 open leads to improve noise margin.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-OL-EGS

# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/5 AND RTS 5A
# CONTROL CIRCUIT

CHANGES

D. Description of Changes

D.1 Add resistor-capacitor filters on CP28 to eliminate high frequency noise on 1-MHz and 2-MHz clock going to enhancements.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-OL-EGS

OPERATIONS SUPPORT SYSTEMS
COMMON
SMAS 5A/B AND RTS 5A
CONTROL CIRCUIT

CHANGES

D. Description of Changes

D.1 A new circuit pack (CP52) was generated as an afterdate standard to replace CP1. CP52 has a more stable crystal clock and also incorporates some class A wiring changes made on drawing issue 10A.

D.2 Pullup resistors were connected to CP16, pin 205, and pin 213 to provide noise immunity on previously open leads.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9231-01-B08

# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/B AND RTS 5A
# CONTROL CIRCUIT

## CHANGES

### D. Description of Changes

D.1 IC14 of CP18 was changed from 74LS365N to MM80C97N to eliminate oscillations seen on some units.

D.2 Generic 2 prom information was added to CP2( ).

D.3 IC1, 2, 3, and 4 of CP18 were changed from 74LS365N to 74LS366N to eliminate oscillations seen on some units.

D.4 CP1 was modified to provide separate $\overline{\text{MEMW2}}$ pulse to supply all RTP. This change was required due to slow risetime of original $\overline{\text{MEMW}}$ pulse causing intermittent operation in control circuit maintenance tests.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-OL-EGS

# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/B AND RTS 5A
# CONTROL CIRCUIT

## CHANGES

### D. Description of Changes

D.1 Note 302 of sheet D2 was changed so that the spare information about the PROM circuit packs does not relate to any particular generic.

D.2 Note 4 was added to sheet J25A to indicate that program documentation is contained in PG-350970.

D.3 Note 7 of Table 1 was added to sheet D2. This note indicates that CP25 and CP26 are used to test the RTS 5A frame and are not required for normal operation.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-LO-JRC

OPERATIONS SUPPORT SYSTEMS
COMMON
SMAS 5A/B AND RTS 5A
CONTROL CIRCUIT

CHANGES

D. Description of Changes

D.1 The printed circuit path going to pin 10 of circuit pack (CP) 8 was cut.

D.2 In CP37, the designations of integrated circuits (IC) 15 and IC 16 were changed from LF 356 to 613K to improve the high frequency response of the 50K-bit filter.

D.3 In CP37, the resistance values for R9 through R19 and R23 were changed to improve the inband shape of the 50K-bit filter.

D.4 In CP37, resistor R20 was eliminated to improve the inband shape of the 50K-bit filter.

D.5 In CP37, the resistor codes of R10, R12, R13, R16, and R19 were changed to make the inband response of the 50K-bit filter more accurate.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 4131-LO-JSI

# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/B & RTS 5A
# CONTROL CIRCUIT

## CHANGES

### B. Changes in Apparatus (Components)

B.2 Added

Circuit pack CP46, "12 Kbyte ROM", has been added to this system.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-LO-EGS

# OPERATIONS SUPPORT SYSTEMS
# COMMON
# SMAS 5A/B AND RTS 5A
# CONTROL CIRCUIT

## SECTION I - GENERAL DESCRIPTION

### 1. PURPOSE OF CIRCUIT

1.01 The RTS 5A control circuit (controller) is a microprocessor circuit used in conjunction with a near-end computer (PC1A), 52A test positions, remote test ports (RTPs), and a Switched Maintenance Access System (SMAS) to test telephone circuits.

### 2. GENERAL DESCRIPTION OF OPERATION

2.01 Operation starts when a 52A test position (52A) is used to access a telephone circuit. The information from the 52A is passed to the PC1A, and the PC1A establishes a link to the far-end controller. The link can be over a private line or DDD circuit. If the link is over the DDD network, the PC1A calls the controller, both hang up, and the controller then calls back the PC1A. This security arrangement is necessary to prevent unauthorized access. Once this link is established, the controller accesses the desired circuit via an available RTP and SMAS access point, and then connects the desired circuit via the RTP back to the 52A over a separate DDD test status verify line. This allows the accessing craft to determine if the circuit is idle before beginning circuit testing.

2.02 At this point, commands may be entered into the TP 52A for circuit testing, and these commands are decoded and sent to the RTS 5A by the PC1A. The testing commands include supervision and termination, signal generation and measurement, and signaling. The signal generation and measurement hardware and software of the controller includes tone generation and the measurement of ac or dc current and voltage, resistance, capacitance, level, frequency, and noise. The controller also has the ability to send test tones, MF, TT, and dial pulsing.

## SECTION II - DETAILED DESCRIPTION

### 1. CPU - FS1

1.01 The central processing unit (CPU) is an 8080A microprocessor system that controls the RTS 5A and SMAS 5A or 5B systems. CPU operation is initialized by momentarily grounding input RESET, which causes address leads A0 through A15 to become logic zero. This address code will cause the CPU to take data out of memory (PROM) on leads DB0 through DB7 and the operational program begins execution.

1.02 The microprocessor device requires additional peripheral devices to produce a complete microcomputer. The clock device (chip) is an 18-MHz crystal oscillator that provides 2-MHz signals of the proper amplitude and duration for the CPU.

1.03 An address buffer (ADD BUS) and data bus buffer (D BUF) provide the necessary drive required for the rest of the system.

1.04 The system controller (SYS CONT) takes signals from the CPU chip and derives control bus signals MEMR, MEMW, I/OR, I/OW, and INTA. These signals are used to clock address and data signals into the proper ICs.

1.05 The 1-kilobyte RAM is a 1024 by 8 bit read-write memory used by the CPU for temporary storage. This block of memory is enabled by grounding ERA1.

### 2. PROM - FS2

2.01 Three PROM circuit packs (CPs) are available in SMAS 5B (two packs for early SMAS 5A and early SMAS 5A/RTS 5A) with a total memory capacity of 36,864 bytes of storage. Each CP is enabled using the proper PR(N)E lead, some address combination on leads A0 through A13, and MEMR. When this condition occurs, data is fetched on leads DB0 through DB7.

### 3. TIMING CHAIN, INPUT PORT L - FS3

3.01 This circuit is used for various timing functions and is also an input port for signals going from the controller peripherals to the CPU.

3.02 Data present on leads DICL0 through DICL7 or timing information from the 24-bit register will be gated into the CPU on leads DIP0 through DIP7 when LTPE and PSD are grounded.

3.03 The #2 (TTL) input to the 24-bit synchronous binary counter is a 2-MHz squarewave that is used to count down to an 8-second squarewave. Timing signals between these two extremes are generated and used by the system for timing and interrupts. These interrupts, 1MSINT, 256MSINT, and 8SECINT, can be enabled or disabled.

### 4. PC CALLBACK, OPTION-EQUIPAGE SCAN, 1/16 TO DECODER - FS4

4.01 This circuit includes the DIP switches that contain primary and secondary PC1A callback numbers. When a DDD data link is used for RTS 5A, the PC1A telephone

number must be stored on DIP rocker switches. Storing this information is explained on sheet J128 of SD-1P107-01.

4.02 Two 1/8 decoders are used on this circuit to produce a 1/16 decoder. Address bits A8 through A11 are decoded to 16 leads, IO0 through IO15.

4.03 The local test port (LTP) equipage is checked using CP12A, which detects the CP7s that are inserted into the controller. When a CP7 is in position, it applies a ground to the input of CP12 on leads G(N)P, and these are read by the CPU.

5. DATA SET I/O, INPUT PORT R - FS5

5.01 This circuit is used to interface the CPU to the data set(s) and to provide another data bus input port between peripheral controller functions and the CPU. It is also used to provide programmable DIP switch information to the CPU.

5.02 There are three DIP switches on CP11; they are used to hold the RTS identity number, to provide a dial pulse TOUCH-TONEr option for PC1A callback, and to determine if the maintenance connector network is equipped with more than 400 maintenance connectors. Switch operation is covered on sheet J11B and in Section 666-615-100.

5.03 The RTPE input port on CP11 is a data bus input port that is used to transfer data set inputs, DIP switch settings, or DICR0 through 7 signals into the CPU (DIP0 through 7). The input port is enabled by RTPE and PS0, which are decoded address bits.

5.04 Three data set configurations are provided in RTS 5A: private line (PL) only, DDD only, and PL with DDD backup. If PL only or DDD only is used, the data set position is the DS1 position. If PL with DDD is used, the DDD data set (202S) position is the DS1 position, and the PL data set position is the DS2 position.

5.05 The CPU is informed of data set activity by an interrupt occurring on DSR (pin 11). When this interrupt occurs, the CPU reads data from the data set on lead SB (pin 25). When it is time for the CPU to send data, the data is sent to the data set on lead BA (pin 26).

6. PRIORITY INTERRUPT, 1/8 OUTPUT DECODER, MEMORY FIELD DECODER - FS6

6.01 The purpose of the priority interrupt and input port is to provide a priority structure for interrupts coming from the controller peripherals to the CPU. The lowest level priority is assigned to 8SECINT (pin 23) while the highest priority is assigned to RST0 (pin 213). Data set interrupt DSR (pin 212) is the second highest priority.

6.02 The memory field enable uses address bits A12 through A15 and decodes them into device enables. The decoded outputs enable the memory field of PROM, RAM, and the I/O devices that are accessed using memory read and write control pulses.

6.03 The 1/8 decoder uses MEMW, PS0, and address bits A5 through A7 to develop signals 00 through 07. The eight output leads are used to select output devices in the controller peripherals.

6.04 The 60-second missing pulse detector (MPD), failure flip-flop (FF), and alarm generator provide a sanity check on the system and an automatic reset mechanism if sanity is lost. After the CPU has been initialized by pushing the reset button on CP16, the CPU continuously pulses the 60-second MPD to keep the failure FF reset. If the CPU stops pulsing the 60-second MPD, the failure FF is set, causing a RESET (pin 214), and this will automatically reinitialize the system.

7. DOC SUPPLY, MF, TT, TONE SUPPLY, PORT SELECT - FS7

7.01 CP14 provides multifrequency (MF) and TOUCH-TONE (TT) pulses for RTS 5A. Data (DOC0 through 7) and decoded address from the CPU determine which frequency and for what duration they are transmitted. The gated tones are sent to CP15 and to the RTPs or to controller subscriber lines via the MF/TT summing and pulsing circuits.

7.02 Five continuous oscillators are available on CP15. They are 2.96-volt rms sinewaves at the frequencies indicated.

7.03 The 1/16 port select encoding takes address bits A0 through A4 and EIO to produce PS0 through PS15. Port select 0 (PS0) is used to address controller latches exclusively and PS(N) (N>0) are used in LTP operation.

7.04 The RTS controller data buffer derives DOC0 through 7 from DOP (0 through 7) to provide more drive capability for controller peripherals.

8. VOLTS, AMPS, RESISTANCE, CAPACITANCE, A/D - FS8

8.01 Voltage, current, resistance, and capacitance are measured using CP5 or CP6 in conjunction with an analog-to-digital (A/D) converter, CP3, and the CPU. A measurement is made by connecting the circuit to the input of an appropriate transducer and converting the parameter being measured to a dc voltage. The CPU applies this dc voltage to the input of CP3, and the A/D converter transforms [8 volts] into 8-bit binary. The CPU also determines the sign (+ or -) of the input to the A/D converter.

8.02 A dc voltage is measured by applying the unknown voltage to the input of CP5 between RM (+) and TM (-). Positive voltages on RM (+) with respect to TM (-) will produce positive readings within the CPU. When the CPU is asked to make a dc voltage measurement, it first closes contacts DCV, HI, and DCV, connecting the input lines to CP5, and connecting the output of CP5 to the A/D bus (8VFS).

8.03 One-hundred milliseconds after the connection is made, the CPU-A/D processing begins. CP3 converts input signals to binary by comparing the output of a digital-to-analog (D/A) integrated circuit (IC) with the 8VFS input and uses the CPU to load the D/A IC. Outputs of the positive comparator (DICL0) and negative comparator (DICL1) are monitored by the CPU.

8.04 At the beginning of A/D processing, a dc voltage is on input 8VFS and the A/D latch contains all zeros, written by the processor. The output of the D/A is 0 volts dc and if the input is positive, DICL0 = logic 1. If the input is negative, DICL1 = logic 1, and by this means the CPU determines the polarity of the input signal. Next, the CPU loads DOC7 = 1 into the A/D latch, the analog output of the D/A IC becomes $\frac{128}{255}$ x 8 volts, and the comparator outputs are checked. After the CPU has processed all eight input data bits DOC(N) in a similar manner, it will have the binary equivalent of the analog input stored in memory. Measurement of dc voltage starts out with the meter in its high range, 224 volts full scale referenced to the input of CP5. If the input signal is less than 56 volts, the CPU will change CP5 to the LO range and now 56 volts at the input to CP5 corresponds to 8 volts full scale at the input to the A/D converter.

8.05 AC voltage is measured on CP5 by closing relays ACV, HI, ACV, and AC. The CPU will wait 1 second after closing the ac voltage relays to give the ac/dc converter time to settle. Then A/D conversion is done in a manner identical to the dc voltage measurement. The HI range on ac volts is 200 volts full scale and the LO range is 50 volts full scale. These appear as 8 volts full scale at the input to the A/D converter.

8.06 Direct current is measured by closing relays AMP, HI, and DCA to allow measurement of ±224 milliamperes. The LO range is 56 milliamperes. Current is measured by inserting a shunt into the circuit in question and amplifying the voltage developed across that shunt.

8.07 Alternating current is measured using the same shunt, amplifying the voltage, and then converting it to dc. The HI ac range is 200 milliamperes and the LO range is 50 milliamperes. A 1-second settling time is used before A/D processing starts to allow the ac/dc converter to stabilize.

8.08 CP5 also contains a ranging and function latch. The CPU loads data into the function latch to close the appropriate relays on CP5 and choose the desired function. The range latch is shared by four circuit packs, CP5, CP6, CP10, and CP13, and changes range on these circuits when the A/D function determines that the input to the A/D circuit is out of range.

8.09 The R-C transducer, CP6, is used to measure resistance and capacitance. Resistance is measured by closing the R relays and applying a known current source across the unknown resistor connected between input RM (+) and MG. The voltage developed across the unknown resistor is passed to the A/D circuit via the voltage follower and converted to binary.

8.10 The 5-range current source can apply 40, 4, 0.4, 0.04, or 0.004 milliamperes to the unknown resistor RX. If RX equals 200 ohms and 40 milliamperes is applied, the input to the A/D will be 8 volts. This is the lowest resistance range. A complete resistance measurement starts by closing the R relays and not applying any current source. The CPU measures any dc voltage present on RX and stores it. A 40-milliampere current is applied to RX and after 50 milliseconds, the CPU does an A/D conversion. If the resistance is above 200 ohms, the A/D will read greater than 8 volts and then apply a 4-milliampere current source. If the A/D input voltage is less than 8VFS, the CPU computes the resistance, which includes subtracting out any initial offset it had measured. For resistances higher than 200 ohms, ranging will continue until the A/D input is less than 8VFS and then the resistance will be computed. The five resistance ranges are 0.2, 2, 20, 200, and 2000 kilohms.

8.11 Capacitance is measured by connecting unknown capacitor CX between RM (+) and MG of CP6 and then closing the C relays. CX is charged by the +8 volts from the voltage reference and then after 250 milliseconds the voltage reference is removed and CX is discharged into the input of an operational amplifier (op amp). If CX is equal to the capacitor CF in the feedback path of the op amp, the voltage on 8VFS will be -8 volts. For CX less than CF, CX = CF x (voltage on 8VFS lead) divided 8. The capacitance measurement actually has two ranges, 5.026 MFD and 0.706 MFD full scale. A measurement starts with the meter set on 5.026 MFD full scale and ranges down if the CPU detects a value less than 0.706 MFD.

## 9. LEVEL, FREQ, NOISE TRANSDUCERS - PS9

9.01 Level and frequency are measured by applying the unknown sinewave to the TTMS and RTMS inputs of CP10. When the level is measured, the output of CP10 is applied to the A/D input bus (8VFS) and converted to binary by the CPU. Frequency measurements are transferred to the CPU via the data bus DICL (0 through 7).

9.02 A level measurement is started by the CPU closing the L relays and setting the range by closing the make contact of relay R1. This sets the input to +10 dBm full scale (levels referred to the input of the remote test port). If the level is below -5 dBm, the CPU will sense this and change to range 2. If the input level was within range 1, a dc voltage would be passed from the ac/dc converter to the A/D converter and stored in memory. While the CPU is determining the proper range setting, it will stay within each range for 100 milliseconds. When the proper range has been determined, the CPU will wait 1 additional second in the final range for complete

stabilization of the ac/dc converter.

9.03 Frequency is measured by using the level measurement circuitry to bring the signal to the proper amplitude and then counting the number of cycles within a specified time period.

9.04 After the level of the input signal has been adjusted by the range circuitry, the CPU will turn on the 4-digit BCD counter by loading the appropriate data bit DOC(N) into the level and frequency latch. The counter is turned off after 1 second and the overflow bit on output DICL2 is sampled by the CPU. If the overflow bit equals 1, it means there have been more than 9999 counts per second (9999 Hz) and the counter outputs should be ignored. If an overflow occurs, a frequency measurement is made again using a gate time of 0.1 second instead of 1.0 second. The overflow bit is rechecked, and if equal to zero, the count is taken on leads DICL0 through DICL7 by the CPU. A maximum frequency of 99.99 kHz can be measured. CP13 allows noise measurement using C notch, program, 15-kHz low-pass, and 3-kHz low-pass weighting networks. It will measure levels from 0 through 60 dBrn (levels referred to the input of the remote test port).

9.05 The CPU makes a noise measurement by loading data into the function latch on leads DOC0 through DOC7. This data closes input relay NIN and the output relay that connects the SFVS A/D bus. The CPU also selects which weighting function is to be used and closes the appropriate relay. Initially, the range is set to 0 dB gain and the noise is converted to dc by the ac/dc converter. Ranging is done by starting with the least gain and sampling the input at the end of 100 milliseconds. If the signal is below range, the CPU will range downward by adding 15 dB of gain. This is done until the signal is within range and then the CPU waits 1 additional second for complete settling of the ac/dc converter. The CPU converts this reading to binary and then stores it.

10. OUTPULSING AND METER ACCESS - FS10

10.01 When it is desired to outpulse TT in order to link up with the PC, the TT signal is pulsed into pin 101, through the amplifier-transformer, and then through contacts DTENT and DTENR, which are closed during the entire process. If a PC link is to be set up using dial pulsing, contacts DTENT and DTENTR are used to break the loop.

10.02 The broadband detector has two functions: it can be used to detect dial tone from RTPS and the data link subscriber line, and it can be used to detect 2600 Hz by switching in the 2600 bandpass filter (BPF).

10.03 The second major function of CP17 is to configure meter leads STV( ) combining from the RTPS and connect them properly to RM (+), CO GRD, and TM (-). RM (+) and TM (-) are metallic inputs to the RTS 5A multimeter.

11. LTP-RTS INT, RTS-SMAS INT - FS11

11.01 This drawing has two major functions. CP8 option M or CP44 options T, N, and V are used to read relay or switch closures coming from SMAS relays or the LTP panel. In SMAS 5B operation the fifth digit is used and this is read by the CPU on input leads 5-26 through 5-29.

11.02 CP9 option M or CP45 options T, N, and V are used by the controller to drive relays for SMAS operation. The CPU loads the appropriate addressable latch from the data bus, using decoded address, and closes mercury relay contacts on CP9 or CP45. These contacts are used to drive wire spring relays.

12. LTP-RTS I/O - FS12

12.01 This drawing describes the LTP panel/RTS 5A interface. One CP7 is required per LTP panel and a maximum of nine LTP panels can be used if option M is not used.

12.02 Operation of the LTP is adequately described in SD-1P106-01 and will not be repeated here. When a CP7 is inserted into a connector, it applies a ground to CP7 pin 6 which is sensed by the CPU. After sensing this ground, the CPU will now continuously scan the CP7 by pulsing PSN pin 28 coincidently with CA6 pin 27. This is done so that unequipped CP7 positions are not scanned which could provide erroneous operation.

12.03 The inputs from the LTP panel, bid (ABA, ABRA, ABB, ABRB) and release (RBA, RBRA, RBB, RBRB) are integrated to remove bounce and scanned into the DIP(N) bus to the CPU. When the CPU senses a closure of the bid key on the A or B side of the LTP panel, it will write the appropriate data into an addressable latch via leads OA0 to OA3 (pins 19, 209, 20, 201). The latched data will momentarily close PSA, PSRA or PSB, PSRB, respectively, to operate the select relay and start the access sequence. The complete access procedure is discussed in SD-1P106-01.

13. RTS/SMAS INTERFACE - FS13

13.01 Sheets 813 and 814 supply the GTG, GTB, and TMB information to drive the SMAS 5 equipment. GTG and GTB leads represent the hundreds and thousands digits information of an SMAS number. For LTP panel operation using an RTS 5A system, GTG( ) and GTB( ) information comes from SD-1P106-01, is cut through by RTS 5A using ENL, and then goes out to SD-1P106-01.

13.02 When an RTP is used and the SMAS number comes from the PC, relays GA, GB, GC, GD, BA, BB, BC, and BD determine the value of GTG( ) and GTB( ). Relay ENR is then used to cut through battery and ground.

14. RTS-SMAS 5A OPERATION WITH ONE OR TWO RTPs - FS14

14.01 This circuit allows operation of an RTS 5A controller with one or two RTPs and no LTPs. Controller mounting plate J1P033AE is used as a mounting point for relays RTP 01 and RTP 02. Control signals LG(N) come from the RTPs and are used to drive relays RTP(N). Closures on these relays go back to the RTPs and provide control signals ENAB-( ) and ENABR-( ). This mode of operation eliminates the stage 1 distribution network on SD-1P106-01.

15. CONNECTOR GROUP CONTROL INTERFACE - FS155

15.01 This drawing is used when SMAS 5B connector group access (option T) is desired. When a connector group is to be accessed either by an LTP or an RTP, the controller simultaneously applies data signals to inputs DOC0 through DOC3 and decoded address signals to inputs 07 and IO14. These logic signals are used to drive mercury relays on CP43 that provide metallic closures for leads DRO to SGR going to the connector group network controller (SD-99560-01 Control and Connector Circuit).

15.02 Control signals coming from the RTP, LG1, and CCM, and from the cont and conn circuit, FD and BSY, are read into the CPU on leads DICR0 through DICR3.

16. 4-KBYTE RAM AND DDS CLOCK TERMINATOR - FS16

16.01 CP18, the 4-kbyte RAM, contains two functions. The 4096 bytes of read-write memory are used as a temporary scratch pad memory when RTS 5A test enhancements are equipped (option Q).

16.02 Two inverters are used to invert logic signals A11 pin 213 and A12 pin 215 to A11 pin 210 and A12 pin 214. These output signals are required to drive PROM board CP2C.

16.03 CP37 is used to provide two functions. When circuit noise has to be measured using a broadband 50-kHz filter, the accessed circuit is connected to TTMS pin 10 and RTMS pin 3. The output of this filter FI5 pin 7 is sent to CP13 and a noise measurement is made.

16.04 The second function of CP37 is to provide a Digital Data System (DDS) clock termination. Two timing supplies L( )X and Y (A and B) are run from the office timing supply to CP37. They are equivalent sources so one or the other is switched into use by CP37. Clock signals BITCKI and BYTCKI are generated from the input timing signal and sent to the test enhancement circuit. The input timing supply is a 64-kb bipolar signal, BITCKI is a 64-kb logic signal, and BYTCKI is an 8-kb clock signal.

17. FAR-END MAINTENANCE CAPABILITY - FS17

17.01 CP25 and CP26 provide circuitry that can be used to troubleshoot RTS 5A controller problems at the frame. The maintenance test BSP for RTS 5A, Section 666-615-500, has a full explanation of the fault location scheme and lists which circuit packs are most likely producing the fault.

17.02 On the front of CP25 is a plug (P1), a test pushbutton (TST), a disable switch (DS), and a breakpoint switch (BP). On the front of CP26 is a jack (J1), two digit thumbwheel switches, and a 3-digit LED display.

17.03 If the maintenance disable switch (DS) is set toward the arrow on the faceplate and the system reset (on the front of CP16) is pushed, the system will be in the RTS 5A operational mode. If DS is set away from the arrow and reset is pushed, the system will be in the maintenance mode and ready for testing at the frame. In the maintenance mode, the system cannot be used to access circuits.

17.04 When the system is in the maintenance mode, BP is set away from the arrow, thumbwheel switches are set to 00, and TST is pushed, the LEDs will display 888. This indicates that all elements of the display are working and the program on CP25 is operational. The maintenance BSP is now used to do all other tests.

17.05 If a teletypewriter (TTY) is inserted in J1 and reset is pushed, the TTY can now be used with an executive program stored on CP25.

17.06 The breakpoint (BP) switch should always be pushed away from the arrow on the faceplate when not being used. The BP switch is used in software debugging to stop the system program at any given point.

17.07 Plug P1 on CP25 is also used for software debugging. A Hewlett-Packard (HP) 1600A logic state analyzer can be connected to P1 and the addresses of the program being used are displayed on the HP CRT. This is used for complex problems and would normally not be used in routine maintenance.

18. CONTROLLER I/O SYSTEM BUFFER - FS18

18.01 The controller uses CP28 to supply all necessary logic signals from the CPU to the enhancements. In the controller, all I/O devices are controlled by memory read or memory write pulses, but the enhancement address and data signals are clocked with IOR and IOW. The outputs of CP28 are supplied to the enhancement modules on twisted pairs of the JNC cable.

18.02 CP28 is also used to supply a path from all enhancements that use the A/D converter to CP3, the A/D converter. AIN pin 101 is a lead from SD-1P112-01 to the input of a low-pass filter. Any noise carried on the dc signal that is to be converted will be shunted to ground at the low-pass filter so that a noise-free signal will be present on the output, pin 104 (8VFS).

19. HUNDREDS- AND THOUSANDS-SCANNERS - FS19

19.01 CP47 is required for connector group access option T. When a connector group is accessed by an LTP or RTP, five decimal digits must be loaded into the controller. When the access is from an LTP panel, CP47 is used to read the hundreds and thousands digits, GTG( ) and GTB( ).

19.02 GTG( ) are closures to ground supplied by the LTP that are combined by a 1/10 to BCD conversion. The BCD number is read into the CPU on leads DICR0 through DICR3.

19.03 GTB( ) are 1/10 closures to -48 volts supplied by the LTP; they are combined and read into the CPU on DICR4 through DICR7.

19.04 The CPU is also used to load input data DOC0 through DOC3 into latches to provide metal closures for control of SEL, TPB, and ALM1 during connector group access operation.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltage range:

| | |
|---|---|
| +5 volts | +4.75 to +5.25V |
| -5 volts | -4.75 to -5.25V |
| +12 volts | +11.4 to +12.6V |
| -12 volts | -11.4 to -12.6V |
| -48 volts | -42.75 to -52.5V |

1.02 Temperature range: +40 to +125oF.

2. FUNCTIONAL DESIGNATIONS

2.01

| DESIGNATION | MEANING |
|---|---|
| WTRQT | Wait Request |
| EIO | Enable Input-Output |
| DIP | Data Input From Ports |
| DB | Bidirectional Data Bus |
| DOP | Data Output to Ports |
| A0 | Address Lead Zero |
| DOC | Data Out to Controller |
| PS | Port Select |
| LTPE | Local Test Port Enable |
| 8 SEC INT | 8-Second Interrupt |
| DIC | Data Input From Controller |
| SL | Subscriber Loop |
| PL | Private Line |
| MG | Meter Ground |
| PR1E | Enable PROM 1 |
| ERA1 | Enable RAM 1 |
| RST | Restart |
| RTPE | Remote Test Port Enable |
| MF | Multifrequency |
| TT | TOUCH-TONE |
| 8VFS | 8 Volts Full Scale |

3. FUNCTIONS

3.01 Provides circuitry for controlling the establishment of a secure DDD data link between the near-end computer and the controller.

3.02 Provides circuitry for controlling the establishment of talk and test status verify circuits between RTPs and near-end test positions.

3.03 Provides circuitry for configuring an RTP to supervise an accessed circuit.

3.04 Provides circuitry to allow an LTP to access a circuit when used with an RTS 5A control circuit.

3.05 Provides circuitry to allow the controller to apply tones and make ac and dc measurements on an accessed circuit.

3.06 Provides circuitry to allow the controller to configure enhancements for complex testing of accessed circuits.

3.07 Provides circuitry to allow troubleshooting of the controller at the frame.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) Local Test Port and Distribution Circuit - SD-1P106-01

(b) Remote Test Port Circuit - SD-1P108-01

(c) Test Enhancement Circuit - SD-1P112-01

(d) Jack Key and Lamp Circuit - SD-99645-01

(e) Control and Connector Circuit - SD-99560

(f) RTS 5A Frame Circuit - SD-1P109-01

5. MAINTENANCE TESTING REQUIREMENTS

5.01 Circuit pack testing is covered in K-79358.

5.02 System testing is covered by Western Electric Test Procedures.

5.03 This circuit shall be capable of performing in accordance with the requirements of 3. FUNCTIONS.

6. ALARM INFORMATION

6.01 Power, fusing, and alarms for the RTS 5A control circuit are covered on the RTS 5A frame circuit, SD-1P109-01.

SECTION IV - REASONS FOR REISSUE

CHANGES

D. Description of Changes

D.1 Pin numbering of IC10 and IC12 on CP44 was changed.

D.2 IC7 of CP45 was changed from 41GU to 41AU.

D.3 Pin numbering on IC7 and IC8 of CP45 was changed.

D.4 Resistor code of R12 CP47 was changed.

D.5 CP18 moved from App Fig 12 to App Fig 8.

D.6 Changed pin numbering of IC8 and IC9 on CP28.

D.7 IC4 of CP3 changed from 621A to 502FR on a line-out basis.

D.8 IC3, IC4, IC8 of CP25 changed to KS-21831 L5 or S0C97.

D.9 Wiring of IC1,2,5,6,7,9 of CP25 changed.

D.10 IC20 of CP25 changed to 41N.

D.11 Add R17 and change wiring of IC9 on CP44.

D.12 CP12B and CP17 move from App Fig 4 to App Fig 3.

D.13 Change Enhancement module clear from RESET to CLA.

D.14 Correct SCFPL on DS2 from pin 6 to pin 12 on plug P4EIA.

D.15 Moved CP11 from App Fig 4 to App Fig 3.

D.16 Changed wiring of IC13 pin 6.

F. Changes in Description of Operation

F.1 Section II, paragraph 12.02 was rewritten to provide more information.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 9232-LO-EGS