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OPERATIONS SUPPORT SYSTEMS
COMMON
RTS5A
REMOTE TEST PORT

CHANGES

B. Changes in Apparatus (Components)

B.1	Superseded	Superseded by
	All 446AH Diodes, CPS7	808DB Diodes, CPS7

B.2 Added

Diode DS1 (LED), 541G Diode, CPS18, Option X

Resistor R27, KS-20616 L1A, CPS18, Option X

D. Description of Changes

D.1 Circuit descriptions are added on J sheets for all circuit packs.

D.2 In FS2 and CAD5, MEMW leads are changed to MEMW2 leads.

D.3 In FS3 and CAD5, MEMR leads are changed to TRPRG leads.

D.4 In CPS6, the DI1 lead terminal 29 is corrected to 22.

D.5 In FS12, Note 1 is added.

D.6 The reference to SMAS 3( ) is deleted in FS3 and FS4, Notes 106 and 303.

D.7 In CPS18, the symbol for 41FP ICs is corrected.

D.8 Block diagrams 2, 3, and 4 are added.

D.9 In FS5, the symbol for CP5 is corrected.

D.10 In FS4, an editorial correction is made in the symbol for CP17.

D.11 In CPS12, drafting corrections are made.

D.12 In CPS18, an inconsistent external lead designation is corrected.

D.13 In CPS14, wiring option Y is introduced as standard with option Z rated Mfr Disc.

D.14 In CPS15, wiring option Y is introduced as standard with option Z rated Mfr Disc.

D.15 In CPS18, wiring option Y is introduced as standard with option Z rated Mfr Disc.

D.16 In CPS12, AMPLZ pin 10 is corrected to pin 7.

D.17 In CPS18, apparatus option X is introduced as standard.

D.18 Circuit packs 2, 11, 12, and 15 are rated Mfr Disc.

D.19 The ringing voltage fuses referenced in circuit note 101 are changed to be consistent with the fusing provided on SD-1P109-01.

F. Changes in CD Section III

F.1 Delete 4.01 (b).

F.2 Add 4.01 (c) as follows:

53A test position, SD-1P166-01.

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DEPT 9232-FBD-EGS

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RTS5A
REMOTE TEST PORT

CHANGES

B. Changes in Apparatus (Components)

B.1 Removed	Replaced By
Circuit Pack CP11, ED-1P456-( ), Fig 1	Circuit Pack CP20, ED-1P628-( ), Fig 1
Circuit Pack CP12( ), ED-1P476-( ), Fig 1	Circuit Pack CP20, ED-1P629-( ), Fig 1

D. Description of Changes

D.1 Functional schematic 10 is altered to show the wiring changes for the replacement of CPs (circuit packs) 11 and 12 with CPs 20 and 21.

F. Changes in CD Section II

F.1 In paragraphs 10.04 and 10.05 change CP12( ) to CP21( ).

F.2 In paragraph 10.06, change CP12A to CP21A and CP12B to CP21B.

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OPERATIONS SUPPORT SYSTEMS
COMMON
RTS 5A
REMOTE TEST PORT

CHANGES

B. Changes in Apparatus (Components)

B.1 Superseded	Superseded By
All Relay, 345A Relay CPS 1	All Relay, 345B Relay, CPS 1
All Relay, 345A Relay, CPS 5	All Relay, 345B Relay, CPS 5
All Relay, 345A Relay, CPS 6	All Relay, 345B Relay, CPS 6
All Relay, 345A Relay, CPS 7	All Relay, 345B Relay CPS 7
All Relay, 345A Relay, CPS 10	All Relay, 345B Relay, CPS 10
All Relay, 345A Relay, CPS 13	All Relay, 345B Relay, CPS 13
All Relay, 345A Relay, CPS 16	All Relay, 345B Relay, CPS 16
All Relay, 345A Relay, CPS 18	All Relay, 345B Relay, CPS 18
All Relay, 345A Relay, CPS 19	All Relay, 345B Relay, CPS 19
IC 12, 13, 15, 16, 18 IC, KS21634 L4 IC, CPS 12	IC 12, 13, 15, 16, 18 IC, KS21634 L10 IC, CPS 12

D. Description of Changes

D.1 Notes 108, 203, and 204 are modified. Note 207 is added.

D.2 Miscellaneous drafting corrections are made.

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DEPT 4131-FBD-EGS

OPERATIONS SUPPORT SYSTEMS
COMMON
RTS 5A
REMOTE TEST PORT

CHANGES

A. Changed and Added Functions

A.1 The use of option X permits connection to SMAS 5B.

A.2 The use of option V permits the use of option 3 (and 4) for operation with SMAS 5() enhancements.

B. Changes in Apparatus

B.1

Superseded	Superseded By
CP2 Circuit Pack, App Fig 1, option Y	CP17 Circuit Pack, App Fig 1, option X
CP15 Circuit Pack, App Fig 1, option Y	CP18 Circuit Pack App Fig 1, option X

B.2 Added

App Fig. 3, option 3

App Fig. 4, option 4

D. Description of Changes

D.1 For description of operation see Issue 2A of this circuit description.

D.2 Standard option X added for SMAS5B with option Y added as Mfr Disc.

D.3 Standard option V added for enhancements with option W added as Mfr Disc.

D.4 CPS J17 sheets, CPS J18 sheets, and CPS J19 sheets added.

D.5 Circuit Notes 106 and 107 added.

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OPERATIONS SUPPORT SYSTEMS
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RTS 5A
REMOTE TEST PORT

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The purpose of this circuit is, under microprocessor control, to enable the testing of 2- and 4-wire telephone and digital circuits that are accessed via a Switched Maintenance Access System (SMAS) whose circuit control characteristics are comparable to those of SMAS No. 5( ). Appropriate dc supervisory conditions may be applied to accessed circuits as well as many of the standard voiceband test and signaling tones. In addition, both ac and dc measurements are enabled. The tone sources and actual measurement capability are derived from a connecting circuit. Appropriate controllable internal level adjustments are available to translate from standard internal levels to various accessed circuit transmission level points (TLPs).

2. GENERAL DESCRIPTION OF OPERATION

2.01 This circuit is controlled by an external microprocessor via a 5-bit port select, a 1-bit enable, an 11-bit address, and an 8-bit data signal. These signals are used to select the proper port and operate or release the desired latches within the port.

2.02 Local control is restricted to a PWR key for the internal -48 to +12V, +5V power converter and a STATUS key that controls the balance of the -48 V and ground used in the port as well as a brute force latch clear.

SECTION II - DETAILED DESCRIPTION

1. POWER DISTRIBUTION, FS 1

1.01 All remote test port (RTP) power is taken through FS 1. Included in the FS is a -48 to +5V dc-to-dc converter and two locking keys. The keys are PWR with a PWR OFF lamp and STATUS with an OUT SRV lamp.

1.02 The PWR key contacts are sequenced in that make-contact 3, 4 close, then make-contact 1, 2 close when the PWR key is operated. This ensures proper turn-on sequence for the PWR UNIT dc-to-dc converter.

1.03 The STATUS key controls the -48 V and ground used in the balance of the RTP and also causes an RTP to be logically hard cleared when in the OUT SERV (off) position (see FS 3).

1.04 Both the PWR and STATUS keys shall be in the off state (outer position, lamps on) any time any RTP circuit packs are to be either withdrawn or inserted or if system fuses are to be inserted. This avoids two problem areas: 1) hits on the logic buses causing random latch operations; and 2) illegal contact sequence damage in an RTP caused by mechanical momentary activation of the 345( ) relays resulting from the mechanical shock of insertion.

1.05 The STATUS key should never be in the operated condition (OUT SRV lamp extinguished) with the PWR key not operated (PWR OFF lamp on). This is an illegal state and should be avoided.

2. ENABLE AND DATA CIRCUIT, FS 2

2.01 This FS handles three primary functions: 1) data signal buffering; 2) enable A generation; and 3) enable B generation.

2.02 The data signal leads, DOP 0-7 (data output from the external microprocessor), are buffered on CP 14, split into an A and B set (ie, DIOA [data input to circuit packs] and DIOB), and distributed to the various circuit packs requiring them. Circuit packs using only addressable latches get only leads DIO( )-3( ). Leads DIO( )-2( ) are within latch address signals and lead DI3( ) is a data signal to be latched at that address. Leads DI4( )-7( ) are used in addition to DIO( )-3( ) when parallel (nonaddressable) latches need to be loaded. There is no logical difference between the A and B sets. The two sets are used simply to control driver loading.

2.03 It should be noted that the data leads, DIO( )-7( ) are not gated in the RTP and have signals present full time, even in an in-service but inactive RTP. These signals, however, are ineffectual except when a given latch within the RTP is enabled by simultaneous lows on one enable A and one enable B which enable only one latch.

2.04 The ENB0-7 (enable B) signal leads are active lows and are decoded from address signals A0-4, A5-7, and the active low remote test port enable (RTPE) signal from the external microprocessor. The A0-4 signals are used to identify a particular port. Identification is by a bit match to the setting of switch S1 on CP 14 which in turn causes an active low on internal lead ME thus enabling both ENA( ) and ENB( ) active low outputs. If within an RTP system, more than one switch S1 is set to the same coding, a certain degree of confusion will result.* The A5-7 signals (3-line binary) are decoded to 1 out of 8 decimal. The decoding is enabled by the active low of the RTPE lead and the internal active low ME signal as previously noted.

2.05 The ENA0-15 (enable A) signal leads are active lows and are decoded from address signals A8-11, the active low memory write (MEMW) signal (and the active low ME signal noted in paragraph 2.04) from the external microprocessor. The decoding is 4-line binary to 1 out of 16 decimal and is enabled by a low signal on the MEMW lead.

2.06 In summary, the DIO( )-7( ) are in continuous operation; the ENA0-15 leads are decoded under control of the port identity and the active low of MEMW signal; and the ENB0-7 leads are decoded under control of the port identity and the active low of the RTPE signal.

2.07 Only one ENA0-15 signal and only one ENB0-7 signal should be simultaneously low within a given port. This coincidence is used to identify and enable a given latch or function within the RTP and to cause the valid information contained within the DIO( )-7( ) signals to be placed in the given latch(es). If, for any reason, extraneous lows are present (resulting from RTP malfunction or other causes), the degeneration of the addressing scheme will cause more than one latch to be simultaneously enabled, causing unusual results.

2.08 Note that signals may be present on ENA1-15 leads and/or ENB1-8 leads and, since time coincidence does not occur within a given RTP, no latches are set.

3. SPECIAL ENABLE, PORT CLEAR, AND MISCELLANEOUS CONTROL CIRCUIT, FS 3

3.01 This FS includes the control portion of circuit pack CP 15 or CP 18 that performs three separate functions.

3.02 The first function is the decoding of special enables and the common RTP clear. The special enables are simply decoded active lows from the active lows of certain ENA and ENB signals and are used for circuit packs that do not have decoding hardware. The common RTP clear is derived from the active lows of ENA5 and ENB7. When both these signals are low, both PCLRA and PCLRB are pulled low and all (but one) latches in an RTP are cleared. Note also that PCLRA and PCLRB signal leads are pulled low when the STATUS key is in the released (out) state.

3.03 The clock function is basically a 4-state, 4-to-1 divider with a high output on the clock pulse start (CP S) lead for state 0 and a high output on the clock pulse finish (CP F) lead for state 2. The

* Port 0 or binary 00000 is typically the identity of the microprocessor itself and is therefore not normally used to identify an RTP.

output is low for states 1 and 3. These signals are used to control EMB or EBM relay transfer functions that are structured from two make-contacts. For example, when a latch bit controlling an EBM relay function is loaded, the CP S signal causes the closed contact to open and the CP F signal causes the open contact to close. The relay characteristics and original timing signal (1-millisecond period) are such that an open interval results achieving the desired EBM characteristic.

3.04 The third function involves an addressable latch which controls various relay functions as shown. In order of system use, the remote test port equipment (RTPEQ) contact is used by the external microprocessor to determine if the RTP is equipped (at least insofar as CP 14 and CP 15 or 18), powered, and not in the out-of-service state via the STATUS key. The line gate (LG) contact for LG2 lead is used as an end mark or similar function for the associated SMAS during the initial call setup or the initial access attempt. The other two LG contacts are used as steering contacts to connect external signals to the external microprocessor. Only one LG function at a time should be active in any system. The cut through (CT) function is used with SMAS 5B to activate the connector group function and then to control the CT function. The HOLD function is used either as a forward acting control signal to establish and then hold the connection as in SMAS 5( ) or to hold an established connection as in SMAS 3( ). The CM1 and CM2 leads are for operational control of maintenance connector circuits which are reached via the associated SMAS. This circuit allows the application of +24 V, ground, or -48 V on each lead. If conflicting information is set (ie, 481 and 241 bits), all relay contacts involved will be open, thus giving an open-circuited output.

3.05 Note that the addressable latch is not cleared from the common port clear. This enables the microprocessor to clear the bulk of RTP hardware using the common clear but yet leaves an established connection up since the hold bit is not affected unless specifically addressed. The STATUS key, however, will clear this latch as well as any other latches when it is operated.

4. MAPPING, TURNOVER, AND FROGGING CIRCUIT, FS 4

4.01 The mapping portion of this FS is the configuration mapping circuit, CP 2 or CP 17. The basic function is to enable the signal and transmission leads from various maintenance connectors or connector groups to be mapped or translated into a rational 3-pair (equipment/facility directions for A, B and E&M or C pairs) format. The change from CP 2 (option Y) to CP 17 (option X) eliminates unused mapping states and introduces appropriate new states for SMAS 5B.

4.02 Two additional functions are supported by the configuration mapping circuit. These are loop test (LT) and split drop (SD) [or its equivalent, split equipment in SMAS No. 5( )].

4.03 The LT function is used to override, but not change, the mapping memory or latch bits. The LT bit, when set high, causes a remapping that complements the action within any maintenance connector when the connector is placed into an LT mode. When the LT bit is set low, the original configuration is restored.

4.04 The split drop prime (SDP) function is used to establish a mapping environment which may than be modified by the SD function when an accessed type 1 or type 2 maintenance connector is split to the drop (equipment) side (SD is set high) or split to the line (facility) side (SD is set low). This function eliminates the otherwise necessary operation of resetting the A0, B0, A1, B1 bits as a type 1 or 2 maintenance connector is changed from the split line (facility) to the split drop (equipment state) and the converse.

4.05 The turnover and frogging circuit CP 3, will interchange or turn over tip and ring leads of any given pair (one or more pairs) and/or interchange or frog the A facility (AF) pair with the B facility (BF) pair and/or interchange or frog the A equipment (AE) pair with the B equipment (BE) pair.

5. METER ENTRY AND E&M SIGNALING CIRCUIT, FS 5

5.01 This FS covers the application of three circuit packs: the meter entry circuit, CP 4; the long term meter and digital entry circuit, CP 19 (option 3); and the E&M signaling, entry and supervision entry circuit, CP 5.

5.02 The (short-term) meter entry circuit, CP 4, is for direct metallic connection to an accessed pair on a one-pair-at-a-time basis. Upon entry, both wires of a pair are opened and all four resulting leads are connected to a common metering bus to the RTS 5A control circuit. The control circuit will, in turn, administer the leads and provide metering for series current measurements, open or closed circuit voltage measurements, resistance measurements, etc. Since such metering is common to a system, it is normally done on a snapshot basis.

5.03 In addition to the metering entry function, CP 4 also contains two shorting functions. These are the AS and BS relays. The shorts can be used in conjunction with the LT function of the maintenance connectors to measure the wire resistance between the maintenance connector accessed by the RTP and the RTP.

5.04 The long-term meter and digital entry circuit, CP 19 (option 3) is similar in concept to CP 4 except that it is

connected to a different bus. Note that the A( )M, B( )M, E( )M latch bits on both CP 4 and CP 19 cause identical results.

5.05 In addition, CP 19 has latch bits digital A pair (DA) and digital B pair (DB). One of these bits, but not both simultaneously, will cause the establishment of equipment and facility output pairs for either the A pairs (DA) or the B pairs (DB). A third pair can be established by activation of the BFM or BEM bit if the DA is set or AFM or AEM if DB is set.

5.06 The E&M signaling, entry and supervision entry circuit, CP 5, has the primary function of generating E&M signaling states. In addition, the facility supervision (FS P) and equipment supervision (ESP) functions may be activated to connect the E&M leads to dc supervisory circuitry when the E&M leads are used for other than E&M signaling. Additional connections to external state sensing circuits are available via the ETRP and MTRP functions. These functions, when set, are arranged to connect the state sensing circuits to the leads that are not being locally signaled on. In other words, if a ground is being locally sent on the E equipment (EE) lead (ECLS and EEE bits set), the ETRP bit will cause the RTSE lead to be connected to the E facility (EF) level.

6. CROSSPOINT CIRCUIT, FS 6

6.01 This FS covers the eight 1x4 latched crosspoint circuit pack, CP 1A, and part of the signaling inductor and resistance circuit circuit pack, CP 8.

6.02 The crosspoints are used to allow either the AF or AE pair to be connected to either of the first two dc supervisory control ckt circuit packs (see FS 8) via associated CP 8 signaling inductors. In the same manner, the BF and BE pairs may be connected to either of the second two dc supervisory control ckt circuit packs via associated CP 8 signaling inductors.

6.03 Connections are also provided from the E&M signaling portion of FS 5 to the connections to the second and fourth dc supervisory control ckt. These connections are used if, for example, the E&M pair actually carries a 2-wire tip and ring pair.

6.04 Additional crosspoints are available for transmission. These crosspoints allow transmission connections to be made for any two of the AF( ), AE( ), BF( ), or BE( ) pairs to either of the ( )A or ( )B pairs.

7. SECONDARY MONITOR ENTRY AND TERMINATION CIRCUIT, FS 7

7.01 The two circuit packs covered by this FS provide four different functions: high-impedance secondary monitoring; burglar alarm control; circuit transmission termination with through-path control; and transmission crosspoints. The first two functions are on the secondary monitoring circuit, CP 16, and the last two on the termination circuit, CP 6.

7.02 The high-impedance secondary monitoring function of CP 16 is controlled by setting one bit (other than RCV1 or RCV2) plus either RCV1 or RCV2 in one latch. No bits are set in the other latch.

7.03 The burglar alarm operation of CP 16 is accomplished in a somewhat different fashion. A bit pair such as AF and AE is set in one latch. This shorts AFT to AET and AFT to AFR. The shorts may then be selectively opened by setting, in the other latch, the BAOT or BAOR bits. Ground may also be selectively applied by setting either the BAGTF, BAGTE, BAGRF, or BAGRE bits.

7.04 The termination function of CP 6 is single-bit controlled and applies 732 ohms with a 2μfd series capacitor. The through-path is also single-bit controlled on the A and B pairs but is arranged for single-lead control (total of two bits) on the E&M pair.

7.05 CP 6 also includes transmission crosspoints for use on the E&M leads for the situation where, for example, the E&M pair is actually a 2-wire tip and ring pair.

8. DC SIGNALING CIRCUIT, FS 8

8.01 The dc signaling circuit, as shown in FS 8, consists of four CP 7s and part of one CP 8. The CP 7s are independent of each other, except for SX operation, and use separate sections of the associated CP 8. It should be noted that CP 7 uses some defensive logic (for abnormal bit combinations that are potentially destructive) which is not shown in the CP 7 symbol. For example, if both TG and T48 latch bits are set, the TG and T48 relay contacts will be open.

8.02 For SX operation, CP 7A and CP 7C may be used as a set and/or CP 7B and CP 7D may be used as a set. Within a set, either circuit pack may be used as the primary signal control board. This is accomplished by setting the simplex control (SXC) latch bit on the board to be used for primary control and the SX latch bit on both boards to establish the basic SX configuration.

8.03 Ringing voltages are selected external to these circuit packs and placed on the tip and ring pair on pins 211 and 216. After selection, ringing is applied to a specific pair by external logic control of the RNG( ) lead to the appropriate circuit pack. This in turn will directly operate the RNG relay functions.

8.04 External connections to a common bus (DCS pair) are provided for possible external sensing of incoming reverse battery or similar signals.

8.05 It should be noted that -72 volts is neither required nor furnished in some offices. There are no internal RTP options to reflect this variation.

9. COMPENSATION AND MATCHING CIRCUIT, FS 9

9.01 This FS and circuit pack CP 11 of FS 10 are the vehicles through which the transmission paths to a maintenance connector are set to a constant resistance which is then padded to a constant loss and then compensated for by fixed gain. This results in a matched 0 loss connection between the RTP and a maintenance connector.

9.02 At the time of initial entry to a maintenance connector, the external microprocessor uses the RTP measurement capability to measure the resistance of the wires that may be used for transmission between the RTP and a maintenance connector. The results of this measurement are then used to compute the resistance of each wire. Then, when either the first or second half of CP 9 is connected to a maintenance connector in the split mode via the associated crosspoints, the buildout resistance on CP 9 is set such that the resistance of each wire plus the buildout resistance is 82 $\pm$ 4 ohms. Next, looking at the schematic for CP 10, option Y, 35.7-ohm fixed resistors are found at the 600-ohm taps with 5.5 ohms of coil resistance. This is effectively 41.2 ohms of resistance and we now have 123.2 ohms total per wire. Going through the transformer (1-to-1 turns ratio for the 600-ohm taps) we find 6.6 ohms of coil resistance per side which increases our total of 129.8 ohms. Next, looking at the effective termination on CP 11, the wires are terminated in 171 ohms each side or 129.8 ohms plus 171 ohms each side for a grand total of 601.6 ohms at the maintenance connector when the 600-ohm transformer taps are used. Comparable results can be found for the 150-, 900-, and 1200-ohm taps. Either transformer option will give essentially the same results. It should be specifically recognized that the only place in this portion of the RTP that has a true impedance match is at a maintenance connector.

9.03 A little number pushing would show that the above resistance and transformer also make up a voltage divider where the division depends on the impedance and gives the same voltage for a given power level (in other words, a constant loss structure). This loss is compensated for by the design of the RTP amplifier structure.

9.04 The remaining items in this FS are the 2-wire network (2WN) function, the SP function, and the amplifier, all shown on CP 9.

9.05 The 2WN function is intended for future use and has no present application.

9.06 The split (SP) function is used in conjunction with the splitting functions in a maintenance connector and serves to disconnect and bypass the monitor amplifier when the maintenance connector is split.

9.07 The monitor amplifier makes up the loss of the monitor transformer used in maintenance connectors.

10. AMPLIFIER, PAD, AND CROSSPOINT CIRCUIT, FS 10

10.01 The circuit symbology for this FS is reasonably straightforward and self-explanatory. However, several sections require further explanation.

10.02 The send (SND) latch data is used to operate the gain steps in the associated send amplifier. When the latch bits are all lows, the variable portion of the gain is 0 dB; when the latch bits are all high, the variable portion of the gain is 63 dB. Note that the gain step is 1 dB.

10.03 The receive (RCV) latch data is used to operate the gain steps in the associated receive amplifiers. When the latch bits are all lows, the variable portion of the gain is 0 dB. With all highs, the variable portion of the gain is 37.5 dB. Note that the RCV2 bit should be read as 2.5 which, in decibels, is the actual gain step.

10.04 The -5 transmission level point (TLP) and 0 TLP references on the left of CP 12( ) are the design value of the TLP of the system. Note that the impedance is 600 ohms.

10.05 The TLP values given on the right side of CP 12( ) show the displacement (voltage relative to a 600-ohm circuit) in decibels of the signal from the actual level of the accessed circuit.

10.06 It should be noted that the listen amplifier on CP 12A is used while the one on CP 12B is not used. Further, the listen amplifier includes a 0 dBm0 limiter or clipper. Any signal from this amplifier will be clipped at the peak level of a 0 dB 0 600-ohm sinewave, in order to protect any connecting subscriber line (see FS 11 and 12) from overload.

11. SIGNAL CONNECTION CIRCUIT, FS 11

11.01 This FS consists of two circuit packs, the eight 1x4 latched crosspoints, CP 1B, and the tone amplifier part of the tone amplifier and miscellaneous control circuit, CP 15/18.

11.02 The crosspoint circuit pack, CP 1B, is used to interconnect various signal paths as required. Connections can be established between the send amplifiers in FS 10 and various tone sources, multifrequency or touch tone (MFTT) dialing or RCVT subscriber line, between the receive amplifiers in FS 10 and a transmission measuring set (TMS) on the TTMS lead, or a single-frequency dial tone (SFDT) detector. The listen amplifier in FS 10 may be connected to the SFDT subscriber line. The subscriber lines may be also connected to the SFDT detector and, in turn, to the MFTT source for call origination. (Dial pulse calls are dialed on CP13 shown in FS 12.) Additional connections are available to the enhancement steering circuit (FS 13) via option V.

11.03 The tone amplifiers on circuit pack CP15/18 are used to buffer the 3-volt RMS signals from the RTS 5A control circuit and to establish the proper levels internal to the RTP as shown in the FS. The tone amplifier connected to the SPTNA lead is spare and is not actively in use.

11.04 Transmission in this FS is on a 600-ohm load basis.

11.05 Option W wiring was not externally implemented. Therefore, it is not discussed.

12. DDD AND RINGING CIRCUIT, FS 12

12.01 The ringing control and telephone ckt circuit pack, CP 13, is the primary item in this FS. It contains one passive and two dynamic functions.

12.02 The passive function is the protection resistance lamps that are used for the CM1 and CM2 leads that are controlled on CP 15/18 in FS3. The lamps are located on CP 13 because of the high profile established by its other components.

12.03 One of the dynamic functions is the control of two originating-only 900-ohm subscriber lines. These lines are controlled by setting the line [LN( )] bit high, thus operating the LN( ) contact. The line may then be dialed, when required, by sequentially setting the dial pulse [DP( )] bit.

12.04 The other dynamic function is the selection and control of 20-Hz ringing. Three types of ringing signals can be connected to the RTP. Two are continuous ringing signals and one machine ring signal. The ringing signal can be applied via any CP 7( ) shown in FS 8.

12.05 To use ringing, a particular combination of the A and B latch bits is first set to identify a particular CP 7. Next, a particular combination of RTPA (ringing type A) and RTPB (ringing type B) latch bits is set and then the application of ringing via CP 7 is controlled by setting the ring (RNG) bit high or low, thus setting the RNG( ) lead to the selected CP 7 high or low. Note, however, that this is not true for the machine ring state (RTPA=RTPB=1). Under this condition, the selected RNG( ) lead will be continuously high until the ringing is tripped. Ring trip is detection of dc current flow followed by automatic clearing of the latch. Note that the machine ring signal is continuous -48 Vdc with superimposed 2 seconds on 4 seconds off 20 Hz. At the end of the desired (or maximum) ringing times, the latch should be cleared by the external microprocessor since no external ring trip signal is generated.

13. MISCELLANEOUS CIRCUITS, FS 13

13.01 This FS covers unused leads.

14. ENHANCEMENT STEERING CIRCUIT, FS 14

14.01 This FS may contain no circuit packs (and is therefore nonfunctional) or it may contain one, two, or three circuit packs depending upon the apparatus options chosen.

14.02 When functional, this FS provides the steering to externally provided enhancements (normally long-term or occasional use) functions. The steering is to selected module buses and the connections could occupy an entire bus or part of a bus. In most instances, it is anticipated that one RTP will be connected to only one module bus at a time.

2.03 Circuit Pack Relays

Circuit Pack 2

Designation	Meaning
EAE( )	E&M drop pair to A equipment pair
EAF( )	E&M line pair to A facility pair
EAF( )	E&M line pair to A facility pair
EBE( )	E&M drop pair to B equipment pair
EBF( )	E&M line pair to B facility pair
EEE( )	E&M drop pair to E&M equipment pair
EEF( )	E&M line pair to E&M facility pair
T1AE( )	T1&R1 pair to A equipment pair
T1AF( )	T1&R1 pair to A facility pair
T1BE( )	T1&R1 pair to B equipment pair
T1BF( )	T1&R1 pair to B facility pair
T1EE( )	T1&R1 pair to E&M equipment pair
T1EF( )	T1&R1 pair to E&M facility pair
TAE( )	T&R pair to A equipment pair
TAF( )	T&R pair to A facility pair
TBE( )	T&R pair to B equipment pair
TBF( )	T&R pair to B facility pair
TEE( )	T&R pair to E&M equipment pair
TEF( )	T&R pair to E&M facility pair

Circuit Pack 3

Designation	Meaning
FRE( )	Frog A&B equipment pairs
FRF( )	Frog A&B facility pairs
TOAE( )	Turn over A equipment pair
TOAF( )	Turn over A facility pair
TOBE( )	Turn over B equipment pair
TOBF( )	Turn over B facility pair
TOEE( )	Turn over E&M equipment pair
TOEF( )	Turn over E&M facility pair

Circuit Pack 4

Designation	Meaning
AEM( )	A equipment pair meter
AFM( )	A facility pair meter
AS	A equipment short
BEM( )	B equipment pair meter
BFM( )	B facility pair meter
BS	B equipment pair short
EEM( )	E&M equipment pair meter
EFM( )	E&M facility pair meter

Circuit Pack 5

Designation	Meaning
EBAT	E lead to battery
ECLS	E lead battery or ground closure enable
EEE	E lead to equipment enabled
EESP	E lead to equipment connected for supervision
EFE	E lead to facility enabled
EFSP	E lead to facility connected for supervision
ETF	E TROP connection to E facility
ETNF	E TROP connection to E not facility (equipment)
MBAT	M lead to battery

Designation	Meaning
MCLS	M lead battery or ground closure enabled
MEE	M lead to equipment enabled
MESP	M lead to equipment connected for supervision
MFE	M lead to facility enabled
MFSP	M lead to facility connected for supervision
MTF	M TROP connection to M facility
MTNF	M TROP connection to M not facility (equipment)
STRP	Strap E&M leads together

Circuit Pack 6

Designation	Meaning
AETE	A equipment pair terminated
AFTE	A facility pair terminated
ATH( )	A pairs connected through
BETE	B equipment pair terminated
BFTE	B facility pair terminated
BTH( )	B pair connected through
EETA( )	E&M equipment pair connected to transmission A pair
EETB( )	E&M equipment pair connected to transmission B pair
EETE	E&M equipment pair terminated
EFTA( )	E&M facility pair connected to transmission A pair
EFTB( )	E&M facility pair connected to transmission B pair
EFTE	E&M facility pair terminated
ETH	E leads connected through
MTH	M leads connected through

Circuit Pack 7

Designation	Meaning
3RL	Three ringer load
DP( )	Dial pulse
DX( )	DX signaling
DXRG	DX signaling ring ground
DXTB	DX signaling tip battery
DXTG	DX signaling tip ground
HS	High sleeve
LNT	Longitudinal noise test
LPH	Loop hold
LPP	Loop pulsing mode
LS	Low sleeve
R48	Ring -48 volts
R72	Ring -72 volts
RL( )	Resistance lamps
RNG	Ringing voltage
RV	Reverse
SX	Simplex signaling
SXC	Simplex signaling control
T48	Tip -48 volts
TG	Tip ground
TRP	TRP (test register and outpulsing)

Circuit Pack 9

Designation	Meaning
2WN( )	2-wire network
8( )	8-ohm compensation
16( )	16-ohm compensation

Designation	Meaning
32( )	32-ohm compensation
64( )	64-ohm compensation
SP( )	Split

Circuit Pack 10

Designation	Meaning
150( )	150-ohm impedance
600( )	600-ohm impedance
900( )	900-ohm impedance
1200( )	1200-ohm impedance

Circuit Pack 11

Designation	Meaning
2W( )	2-wire
RCV( )	Receive
SND( )	Send
TER( )	Terminate
TMS( )	Transmission Measuring Set

Circuit Pack 13

Designation	Meaning
LN( )	Line loop closure
RNGH( )	Ring high voltage
RNGL( )	Ring low voltage
RNGT( )	Ring trip

Circuit Pack 15

Designation	Meaning
241	+24 volts applied to CM1 lead
242	+24 volts applied to CM2 lead
481	-48 volts applied to CM1 lead
482	-48 volts applied to CM2 lead
HOLD	Hold
LG( )	Line gate
RTPEQ	Remote test port equipped

Circuit Pack 16

Designation	Meaning
AER	A pair equipment ring lead
AET	A pair equipment tip lead
AFR	A pair facility ring lead
AFT	A pair facility tip lead
BAGR	Burglar alarm ground ring
BAGT	Burglar alarm ground tip
BER	B pair equipment ring lead
BET	B pair equipment tip lead
BFR	B pair facility ring lead
BFT	B pair facility tip lead
EE	E&M pair equipment E lead
EF	E&M pair facility E lead
ME	E&M pair equipment M lead
MF	E&M pair facility M lead
RCV( )	Receive
RCV1	Receive rail 1
RCV2	Receive rail 2

Circuit Pack 17

Designation	Meaning
B4BE( )	B pairs (SMAS4) to B equipment pair
B4BF( )	B pairs (SMAS4) to B facility pair
B4EE( )	B pairs (SMAS4) to E&M equipment pair

Designation	Meaning
B4EF( )	B pairs (SMAS4) to E&M facility pair
EAE( )	E&M drop pair to A equipment pair
EAF( )	E&M line pair to A facility pair
EBE( )	E&M drop pair to B equipment pair
EBF( )	E&M line pair to B facility pair
EEE( )	E&M drop pair to E&M equipment pair
EEF( )	E&M line pair to E&M facility pair
T1AE( )	T1&R1 pair to A equipment pair
T1BE( )	T1&R1 pair to B equipment pair
T1BF( )	T1&R1 pair to B facility pair
T1EE( )	T1&R1 pair to E&M equipment pair
T1EF( )	T1&R1 pair to E&M facility pair
TAE( )	T&R pair to A equipment pair
TAF( )	T&R pair to A facility pair
TEE( )	T&R pair to E&M equipment pair
TEF( )	T&R pair to E&M facility pair

Circuit Pack 18

Designation	Meaning
241	+24 volts applied to CM1 lead
242	+24 volts applied to CM2 lead
481	-48 volts applied to CM1 lead
482	-48 volts applied to CM2 lead
HOLD	Hold
LG( )	Line gate
RTPEQ	Remote test port equipped

Circuit Pack 19

Designation	Meaning
AEM( )	A equipment pair meter
AFM( )	A facility pair meter
BEM( )	B equipment pair meter
BFM( )	B facility pair meter
DAB( )	Digital, A or B pair
DAEM( )	Digital, A equipment pair meter
DAFM( )	Digital, A facility pair meter
DBEM( )	Digital, B equipment pair meter
DBFM( )	Digital, B facility pair meter
EEM( )	E&M equipment pair meter
EFM( )	E&M facility pair meter

3. FUNCTIONS

3.01 Provides holding interface control and maintenance connector control for SMAS 3( ) and SMAS 5A/B.

3.02 Provides configuration mapping for all maintenance connector and connector group applications.

3.03 Provides pair frogging and turnover capability.

3.04 Provides ac and dc short-term meter connection capability.

3.05 Provides ac and dc long-term meter connection capability and long-term digital connection capability (option 3).

3.06 Provides E&M signaling capability.

3.07 Provides DX, loop, and SX signaling and supervisory capability.

3.08 Provides compromise terminations or through-paths for split circuits.

3.09 Provides burglar alarm functions.

3.10 Provides secondary monitoring capability.

3.11 Provides primary monitoring capability.

3.12 Provides resistance compensation to standardize accessed circuit transmission characteristics independent of accessed path length.

3.13 Provides impedance matching for 150-, 600-, 900-, and 1200-ohm circuits.

3.14 Provides program adjustable gain for both sending and receiving functions to match accessed circuit TLPs.

3.15 Provides resistance hybrid for 2-wire operation.

3.16 Provides for connection of 404, 1004, 2600, 2713, and 2804 tones as well as TOUCH-TONE® and multifrequency signaling.

3.17 Provides for connections to single-frequency and dial tone detectors.

3.18 Provides for connections to transmission measuring sets.

3.19 Provides for connections to two port associated subscriber lines for use of craftspersons for either talking or monitoring.

3.20 Provides for connections to enhancements (option 3 and additional option 4).

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a key sheet, the connecting information thereon is to be followed.

(a) RTS5A, RTS5A Frame Ckt SD-1P109-01

(b) SMAS5A/5B, RTS5A Control Ckt SD-1P107-01

(c) SMAS5A, Local Test Port and Distribution Ckt SD-1P106-01

(d) SMAS5B, Interface Ckt SD-99641-01

(e) SMAS3A, 3B, and 3C, Maintenance Concentrator and Control Ckt SD-99500-01

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are as specified in specification X-79366.

SECTION IV - REASONS FOR REISSUE

CHANGES

B. Changes in Apparatus (Components)

B.1

Removed	Replaced By
IC1 Integrated Ckt 93L34PC, CP 7	IC1 Integrated Ckt CP 7
R36 Resistor, KS-16311 L5D, 4420 ohms, CP 12	R36 Resistor, KS-16311 L5D, 7590 ohms, CP 13
R3 Resistor, KS-16311 L5D, 3050 ohms, CP 12	R3 Resistor, KS-16311 L5D, 3160 ohms, CP 12
R29 Resistor, KS-16311 L5D 10K ohms, CP 12	R29 Resistor, KS-16311 L5D, 11.1K ohms, CP 12
R30 Resistor, KS-16311 L5D, 23.4K ohms, CP 12	R30 Resistor, KS-16311 L5D, 53.6K ohms, CP 12

B.2 Added

C6 Capacitor, KS-19774 L2, 220 pF, CP 1

C7 Capacitor, KS-19774 L2, 47 pF, CP 1

C8 Capacitor, KS-19774 L2, 1000 pF, CP 1

C9 Capacitor, KS-19774 L2, 1000 pF, CP 1

R1 Resistor, KS-20616 L1A, 5.11K, CP 1

R2 Resistor, KS-20616 L1A, 5.11K, CP 1

C7 Capacitor, KS-19774 L2, 47 pF, CP 4

C8 Capacitor, KS-19774 L2, 200 pF, CP 4

R13 Resistor, KS-20616 L1A, 5.11K ohms CP 4

R14 Resistor, KS-20616 L1A, 5.11K ohms CP 4

C14 Capacitor, KS-20480 L1, 0.01 µF CP 7

C15 Capacitor, KS-20480 L1, 0.01 µF CP 7

CR1-8 Diodes, 446AF, CP 8

C20 Capacitor, KS-19774 L2, 0.01 µF CP 13

B.3

Superseded	Superseded By
CR1-8 Diodes, 446AF, CP 8	CR1-8 Diodes, 808DA, CP 8

D. Description of Changes

D.1 In FS 2 and FS 3, DOPO-7, AO-11, RTPE, and MEMW leads were paired with ground. A12-15 leads and two terminal strips were deleted. Old CAD 6 was deleted and CAD 7 and CAD 8 renumbered as CAD 6 and CAD 7. CAD 1, CAD 2, and CAD 5 were reworked.

D.2 In FS 1, STATUS key was rewired and CAD 3 and CAD 4 changed accordingly.

D.3 On sheet H1, CP 14 was relocated.

D.4 Title of CAD 5 was changed.

D.5 CAD 3 and CAD 4 were corrected.

D.6 In CAD 4 a lead was added to terminal 2.

D.7 In FS 1 and CAD 3 and CAD 4, a 10-gauge ground jumper was added.

D.8 Circuit Note 105 was added.

D.9 In FS 1 and CAD 3 and CAD 4 a B ground to X ground tie was added.

D.10 In FS 11, mults were added to SFDT, RCV1, and RCV2 leads.

D.11 In CAD 1, CAD 6, and CAD 7, ENAB1 and ENAB2 leads were modified.

D.12 In FS 8, SXC1, SXC2, SXC3, SXC4, SXNC1, SXNC2, SXNC3, SXNC4 leads were modified.

D.13 In FS 3, PCLRA and PCLRB lead destinations were modified.

D.14 In FS 8 and FS 12 and CAD 3 and CAD 4 ringing lead wiring was modified and Equipment Notes 205 and 206 added.

D.15 Certain leads were replaced with shielded singles per new Circuit Note 108 and Equipment Note 203.

D.16 In FS 1, a B ground was added to terminal 4 of J21( ) connector.

D.17 In FS 4, a DI7 lead was added to terminal 102 of J1( ) connector.

D.18 In FS 1, a B ground was added to terminal 203 of J9( ), J10( ), J11( ), and J12( ) connectors.

D.19 In FS 5, shielded pairs were substituted for twisted pairs used for STVMOT/R and STVMIT/R leads and Equipment Note 204 was added.

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