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ELECTRONIC SWITCHING SYSTEMS

NO. 2
ARRANGED WITH 2-WIRE FEATURES

CIRCUIT PACK SCHEMATICS

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This schematic drawing shows detailed circuit information for all circuit packs used in the No. 2 Electronic Switching System (ESS).

2. GENERAL DESCRIPTION OF OPERATION

2.01 The basic building block circuit of the No. 2 ESS is the high-speed transistor-resistor logic (HSTRL) gate. Approximately 20 codes of general purpose circuit packs, each containing variations and combinations of this basic gate, are interconnected throughout the system control unit to perform most of the logical and data-processing functions required.

2.02 In certain circuit areas where the use of general purpose logic packs would be either uneconomical or unsuitable (eg, in analog circuitry), special purpose circuit packs are provided. These packs are assigned code numbers between A431 and A917 and are designed to perform one or more specialized functions in a particular unit.

2.03 The operation and capabilities of the basic HSTRL gate in its various forms are described in detail in Section II. Input-output information and brief descriptions of operation for the gate combinations used on general purpose circuit packs and for the circuits on special purpose packs are contained on the associated B and J sheets of this drawing.

SECTION II - DETAILED DESCRIPTION

1. TRL GATE OPERATION

1.01 A 2-input HSTRL gate is shown schematically on sheet J401 at position 2A. The inputs, terminals 2 and 3, receive digital signals whose value may be either a nominal GRD (less than +0.27 volt) or +E (greater than +2.15 volts). The value at the output, terminal 4, may also be either GRD or +E but is a function of the input conditions. The transistor saturates when one or both of the inputs is at +E. When saturated, the collector-emitter (CE) junction is a near short circuit, and the output voltage at terminal 4 is approximately at GRD. When both inputs are at GRD, the transistor is cut off, the CE junction is effectively an open circuit, and the output is at +E.

1.02 The 4-input TRL gate, shown on sheet J405 at position 2A, is similar to the 2-input gate, except that, because of base current limitations and other circuit considerations, a dual transistor is used. Functionally, the circuits are identical: when one or more inputs are at +E, the output is at GRD; when all inputs are at GRD, the output is at +E.

1.03 As described previously, the signals at the inputs and outputs of the TRL gate are permitted to assume only two different values: +E (actually, any voltage greater than +2.15 volts) and GRD (any voltage less than +0.27 volt). These signals may be used to represent any set of Boolean variables, such as true or

false, open or closed, good or bad, on-hook or off-hook.

1.04 If a logical 1 is assigned to the +E voltage condition and a logical 0 to the GRD condition, the output of the TRL gate assumes the 1 state if, and only if, all inputs are at the 0 state as shown in Table A. Letting A and B represent the inputs of a 2-input gate, the Boolean expression for the output is the NOR logic relationship: $(A + B)' = A' B'$.

TABLE A

TRUTH TABLE FOR TRL NOR GATE

INPUTS		
A	B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

1.05 Any Boolean equation can be expressed using only the AND, OR, and NOT logic functions. The output of a 1-input TRL gate, an inverter, is always opposite in polarity to the input and, thus, can be used to perform the NOT operation. The OR function requires two NOR gates; one gate produces the inverted OR, and the other acts as an inverter to produce the normal output. The AND operation is achieved with the NOR gate when complement inputs are used. These complements are obtained from the outputs of inverters, when necessary. Therefore, any Boolean expression used in the design of a digital system can be implemented using only the TRL NOR gate configuration.

1.06 The symbol for the standard HSTRL NOR gate is described on sheet D1, Information Note 301.

2. INPUT-OUTPUT INFORMATION

2.01 Associated with each circuit pack schematic drawing, the input-output information presents data related to the operating characteristics of the circuitry on that circuit pack. Certain terms and expressions commonly used in describing these characteristics are defined in 2.02 through 2.06.

2.02 The fan-in of a logic stage is the number of independent inputs to that stage.

2.03 The fanout of a logic stage is the number of other stages driven by the logic stage.

2.04 Signal level refers to the two ranges of voltages which are considered either TRL ground level or TRL off-ground level. The span of voltages shown for the off-ground output signal level assumes 5-percent resistor tolerances and a power supply of 5.4 to 7.2 volts at the circuit pack terminals. The ground signal level voltage is determined by transistor characteristics controlled in manufacture. At 80°C in a worst-case TRL circuit, the transistors specified have a V at saturation of less than 270 mV.

2.05 Propagation delay is defined as the elapsed time between an amplitude point on the input signal and the corresponding point on the output signal. Unless otherwise stated, it is assumed that the half-amplitude points are being measured. Turnon delay applies to a ground-going output signal; turnoff delay applies to a +E going output signal. The delays given are for worst-case circuit configurations at nominal resistance and power supply voltage values; they are only for the basic gates and do not include increased delay times due to wiring and parasitic effects.

2.06 The loading of a circuit pack terminal is equal to the number of equivalent TRL logic stage inputs connected to that terminal.

3. FAN-IN EXPANSION

3.01 Circuit considerations require that the fan-in per transistor base be limited to two. Fan-in may be expanded by paralleling collectors and providing only one common collector resistor for the combination. The maximum fan-in which can be obtained is limited by the degrading effect of the added capacitance of the paralleled collectors on the speed of the gate. Where speed is not critical, a fan-in of 40 is possible.

3.02 Sheet J418 illustrates how collectors may be paralleled to increase fan-in. The gate shown at position 2B is known as an unpowered gate, since the collector is brought directly out to thin-film gate terminal 10 and the collector resistor and connection to +6 volts are omitted. This collector connects to the powered collector of the gate at position 5A, with the combination forming an 8-input gate. The common collector lead is brought out on circuit pack terminal 13 so that fan-in may be increased further, if required, by the connection of other unpowered gates, such as those shown on sheet J408. The letter U in the logic symbol is used to designate the unpowered gate.

4. FANOUT EXPANSION

4.01 The maximum fanout of the standard HSTRL gate is three. For larger fanout, medium- and high-power TRL gates are provided. Medium-power (PM) and high-power (PH) modifiers are added in the logic symbols to identify these gate circuits.

4.02 The configuration of the 2-input PM TRL gate is shown on sheet J402 at position 2B. An HSTRL stage controls an emitter-follower (EF) which provides sufficient current to drive up to ten TRL stages. The EF transistor saturates when a +E voltage is applied to its base. The values of the two EF resistors have been selected so that the voltage at gate terminal 2, under these conditions, is regulated within the limits for +E. When the EF is cut off by the application of a GRD signal to its base input, the output is kept within TRL GRD limits by the low impedance of the emitter-resistor, which acts as a reverse-current sink for the input circuits of the driven gates.

4.03 Since the EF acts only as a current amplifier and does not invert the signal, the logical operation of the PM TRL gate is identical to that of the standard TRL gate as indicated by the symbol shown on sheet J402. Fan-in expansion is accomplished by connecting one or more unpowered TRL stages to the input gate collector. By convention, this connection is also shown entering the side of the logic symbol as shown on sheet J409.

4.04 The configuration of the 4-input PH TRL gate is shown on sheet J407 at position 1A. This circuit is capable of driving up to 44 TRL loads. The necessary current is obtained from a clamped EF with output at thin-film gate terminal 2. The emitter-resistor in the follower circuit is replaced by a dual transistor which acts as a clamp to maintain the proper TRL GRD output level. The output at +E is regulated by the EF through its collector resistor, with the clamp being turned off in this state. The TRL-compatible input stage is followed by two inverters which supply the currents needed to drive the EF and the clamp and provide a net logical inversion equal to that of the standard TRL gate.

4.05 As in the PM gate, the test point connection is made to the base of the EF. Fan-in to the PH gate is expanded by connecting unpowered TRL stages to thin-film gate terminals 3 and 12 and is indicated by a lead connecting to the side of the symbol, as shown on sheet J419.

5. FLIP-FLOPS

5.01 A TRL flip-flop consists of two TRL gates interconnected so that the output of each gate is cross-connected to an input of the other. In this configuration, the gates form a bi-stable logic device capable of maintaining either of two possible states, and thus can be used to perform counting, shift register, and memory functions.

5.02 For purposes of circuit analysis, assume that all inputs on gate A1, sheet J411, are at GRD, except gate terminal 7 which is at +E. The upper transistor conducts, forcing its output at terminal 4 to GRD. Since all inputs to the lower transistor are at GRD level, this gate is nonconducting, and its output, terminal 10, is at +E. Thus, the outputs of the two gates forming the flip-flop are at opposite levels. Since terminal 10, at E+, cross-connects to the upper gate input, terminal 5, the flip-flop will remain locked in the same state even after the original +E signal at terminal 7 is removed. If, however, a +E signal is applied to terminal 8, terminal 10 goes to GRD, terminal 4 goes to +E (assuming +E at terminal 7 has been removed), and the flip-flop is set in the opposite state.

5.03 The logic symbol for a flip-flop is a rectangular box with the letters FF, as shown on sheets J411 to J414. The modifiers PM and PH are also shown, when required. Either side of the flip-flop may be used as a set or clear side, depending upon circuit requirements. It should be noted that each output lead on the flip-flop symbol is shown associated with the input leads of the opposite side. The symbol differs from the schematic in this fashion since, for logical clarity, it is customary to show the one output opposite the set inputs and vice versa.

6. BINARY COUNTERS/SHIFT REGISTERS

6.01 The schematic for the binary counter/shift register circuit is shown on sheets J415 and J416. Two gates with TRL-compatible inputs are interconnected to form a bi-stable logical element similar to the flip-flop described earlier. Capacitors are employed across the cross-coupling resistors to increase the speed of operation. The diodes and associated steering capacitors connecting thin-film gate terminal 11 act as a steering circuit to direct an incoming ground-going signal to the base of the conducting transistor. Thus, each time a ground-going signal is applied to the trigger (T) lead the circuit will switch to the opposite state. EFs provide PM fanout at TRL levels. The resistors connecting gate terminals 13 and 9 allow the same basic circuit to be connected and act as a binary counter as shown on sheet J415 or as a shift register as shown on sheet J416.

6.02 The symbols for the binary counter and shift register are rectangular boxes with the letters BC and SR, respectively, as shown on sheets J415 and J416.

Either side may be used as a set or clear side, and each output lead is associated with the input leads of the opposite side as described in 5.03.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 These circuit packs provide plug-in logic and analog circuitry for use in the No. 2 ESS.

4. CONNECTING CIRCUITS

4.01 None

5. MANUFACTURING TESTING REQUIREMENTS

5.01 None required.

6. TAKING EQUIPMENT OUT OF SERVICE

6.01 Power must be turned off while circuit packs are being removed or replaced in the equipment.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 Added circuit packs A565, 566, 1129, 1156, 1224, 1225, 1226, and 1235.

D.2 Incorporated changes to reduce circuit pack cost. These changes are reflected on a line-out basis in the circuit pack schematic stock list.

D.3 Reissued circuit pack schematics for the following circuit packs to reflect the changes described in D.2.

A425	A551
A443A	A554
A458	A563
A481B	A794D
A491A&B	A805
A507A&B	

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