OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 APP FIG 4

Removed	Replaced By
J Pack Circuit, PICB INTER, MC2P004A2B, AM (TN629B)	J Pack Circuit, PICB INTER, MC2P004A3B, AH (TN629B)

B.2 APP FIG 5

Removed	Replaced By
J Pack Circuit, PMUINT1, MCP010B2 (SM251)	J Pack Circuit, PMUINT1, MC2P010B3 (SM251)
J Pack Circuit, PMUMEN1, MC2P00A2 (SM274)	J Pack Circuit, PMUMEN1, MC2P010A3 (SM274)

B.3 APP FIG 6

Removed	Replaced By
K Pack Circuit, PMUINT (), MC2P010B2 (SM251)	K Pack Circuit, PMUINT (), MC2P010B3 (SM251)
J Pack Circuit, PMUMEN (), MC2P010A2 (SM274)	J Pack Circuit, PMUMEN (), MC2P010A3 (SM274)

D. Description of Changes

D.1 The following changes are made to provide new DCTU firmware.

D.2 Fs 3, PICB INTER, MC2P004A3B was MC2P004A2B. Also updated "POWER DATA" table.

D.3 FS 5, PMUINT 1 and PMUINT (), MC2P010B3 was MC2P010B2.

D.4 Note 207, MC2P004A3B was MC2P004A1B.

D.5 Note 302 and 303 updated.

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OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 APP FIG 2, FS 17
Added
982M, Resistor Module, 104385059

B.2 APP FIG 5

Removed	Replaced By
[4] Port 1, Option J CLEI CODE LMPQ17A	[4] Port 1, Option J CLEI CODE LMPQ17B

B.3 APP FIG 6
Added
[4] Port 9 () Option J. LMPQ17B, SM248B (A&M only)

Removed	Replaced By
[-] Port ()	[4] Port Option K

D. Description of Changes

D.1 The following changes are made to make the DCTU meet original design intent.

D.2 Designation Mnemonic Index updated.
MTBT (0-2) (0-3) and MTBR (0-2) (0-3) changed FS 16 to CAD 9, 10, 11. Also added RMT and RMR.

D.3 FS 16, leads 049, 149, 048, 148, 047, 147, 046, 146, 046, 146 changed designations and notation reference "FS 17 via (CAD 25)" for leads on "PORT PMUØ" and "FS17 via (CAD 26, 27) for leads on "PORT PMU ()". PMUØ was PMU1. Also update TABLE C.

D.4 FS 17 added.

D.5 CADs 9, 10, and 11 added pin numbers and references to FS 17, and sheet note 2.

D.6 CADs 25, 26, and 27 added.

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B. Changes in Apparatus

B.1 APP FIG 4

Superseded	Superseded By
(K) PICB INTER, Pack Circuit, LMMQ048, (A&M only) MC2P004A1B (TN629B)	(J) PICB INTER, Pack Circuit LMMQ04C, MC2P0042B (TN629B)

B.2 APP FIG 5

Superseded	Superseded By
(K) PMUINT1, Pack Circuit LMMQ20CAXX MC2P002B1 (SM251)	(S) PMUINT1, Pack Circuit LMMQ20E, MC2P002B2 (SM251)
(K) PMUEM1, Pack Circuit LMMQ12C, (A&M only) MC2P002B1 (SM251)	(S) PMUEM1, Pack Circuit LMMQ21B, MC2P002A2 (SM274)

Added

(J) R4, Resistor, KS-20616,L1A, 1000 ohm

B.3 APP FIG 6

Superseded	Superseded By
(K) PMUINT(), Pack Circuit LMMQ20CAXX MC2P002B1 (SM251)	(J) PMUINT(), Pack Circuit LMMQ20E, MC2P002B2 (SM251)

(K) PMUMEM(), Pack Circuit
LMMQ21A
MC2P010A1 (SM274)

(J) PMUMEM(), Pack Circuit
LMMQ21B
MC2P010A2 (SM274)

Added

(J) R(), Resistor, KS-20616, L1A, 1000 ohm

D. Description of Changes

D.1 All changes are made to provide DCTU users with an option in which requests for DCTU testing can be made directly from an ARSB office to a 5ESS office over a Data Link. This option will only apply to DCTUs under generic 5E2(1) (or Higher) software. The Generic software must be installed before hardware or the hardware can be installed later.

D.2 FS 3, FS 5, FS 9, FS 13, FS 16, APP FIGs 4, 5 and 6, added options J and K.

D.3 Note 303 updated.

D.4 Note 312 Added.

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OPERATION SUPPORT SYSTEMS
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CIRCUIT

B. Changes in Apparatus

B.1 APP FIG 4

Removed	Replaced By
SWU1, Pack Circuit LMPQ5B, SN423	SWU1, Pack Circuit LMPQ05CAXX, SN423

B.2 APP FIG 5

Removed	Replaced By
PMUINT1, Pack Circuit LMMQ12D MC2P002B1 (SM251)	PMUINT1, Pack Circuit LMMQ20CAXX MC2P010B1 (SM251)

B.3 APP FIG 6

Removed	Replaced By
PMUINT(), Pack Circuit LMMQ12D MC2P002B1 (SM251)	PMUINT(), Pack Circuit LMMQ20CAXX MC2P010B1 (SM251)

B.4 APP FIG 7

Removed	Replaced By
SWU2, Pack Circuit, LMPQ05B, SN423	SWU2, Pack Circuit, LMPQ05CAXX, SN423

B.5 APP FIG 8

Removed	Replaced By
SWU3, Pack Circuit LMPQ05B, SN423	SWU3, Pack Circuit LMPQ05CAXX, SN423

D. Description of Changes

D.1 Changes in B.1 through B.5 are to update circuit pack information.

D.2 FS 13 add -48 and B-GRD leads. Drawing correction

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D. Description of Changes

D.1 CAD1, changed lead from E6 to 5ESS Grd window (QUIET GRD) from 14 GA to 16 GA. To conform with 5ESS standardization.

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D. Description of Change

D.1 Note 306 applies to this class AC change, not drawing issue 7B.

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B. Changes in Apparatus

B.1 APP FIG 5

Removed	Replaced By
PMUCTL1, Pack Circuit LMMQ08A MC2P002C1(SM250)	PMUCTL1, Pack Circuit LMMQ08BA, MC2P002C1(SM250)

B.2 APP FIG 6

Removed	Replaced By
PMUCTL(), Pack Circuit LMQ08A, MC2P002C1(SM250)	PMUCTL1, Pack Circuit LMQ08BA MC2P002C1(SM250)

D. Description of Changes

D.1 APP FIG 5 and 6 changed to show new codes for SM250.

D.2 Notes 207 and 208 added to provide information for installers.

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OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

B. Changes in Apparatus

B.1 APP FIG 1

Superseded	Superseded By
(N) +5.1A, Pack Circuit PWPQ21A, 495A	(M) +5.1A, Pack Circuit PWPQ54CA, 495FB
(N) +12, Pack Circuit PWQ20E, 494E	(M) +12, Pack Circuit PWPQ53YA, 494MA
(N) +150, Pack Circuit PWPC21D, 495D	(M) +150, Pack Circuit PWPQ53YA, 494MA

B.2 APP FIG 8

Superseded	Superseded By
(N) 5.1B, Pack Circuit PWPQ22A, 496A	(M) 5.1B, Pack Circuit PWPQ54CA, 495FB

D. Description of Changes

D.1 Added option M and N. Power units 495A, 496A, 494E are scheduled to be Manufacture Discontinued by 1/84. This change permits AT&T-T to replace these power units with Generic III versions.

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D. Description of Changes

D.1 Note 306 to provide information for mounting apparatus for installation of a DCTU in a 6 Foot 5ESS* Single Bay Frame.

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*Mark of AT&T

OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

B. Changes in Apparatus

B.1 APP FIG 1

Added

Stop Codes to Circuit Packs +5.1A, +12, +15, -12, and -150.

B.2 APP FIG 4

Added

Stop Codes to Circuit Packs DCTUCTL, PICB INTER(2) and SWUL.

Removed	Replaced By
DCTUCTL, Pack Circuit, Eqpt Loc 004-010 LMPQ05A, SM422	DCTUCTL, Pack Circuit, Eqpt Loc 004-010 LMPQ15A, SM422
PICB INTER, Pack Circuit, Eqpt Loc 004-018 MC2P004A1, TN629	PICB INTER, Pack Circuit Eqpt Loc 004-018 MC2P004A1B, TN629B

B.3 APP FIG 5

Removed	Replaced By
CAN1, Pack Circuit, Eqpt Loc 004-146 LMPQ03Y, SM264	CAN1, Pack Circuit, Eqpt Loc 004-146 LMPQ23Y, SM264
FILTR1, Pack Circuit, Eqpt Loc 004-050 LMPQ03T, SM259	FILTR1, Pack Circuit, Eqpt Loc 004-050 LMPQ13T, SM259B
PMUINT1, Pack Circuit, Eqpt Loc 004-018 LMMQ02B, MC2P002B1 (SM251)	PMUINT1, Pack Circuit, Eqpt Loc 004-018 LMMQ20B, MC2P010B1 (SM251)

B.3 Cont APP FIG 5

Removed	Replaced By
PMUMEM1, Pack Circuit Eqpt Loc 004-026 LMMQ02A, MC2002A1 (SM274)	PMEMEM1, Pack Circuit Eqpt Loc 004-026 LMMQ21A, MC2P010A1 (Sm274)
[2]SIG COM1, Pack Circuit Eqpt Loc 004-058,004-070 LMP03S, SM258	[2]SIG COM1, Pack Circuit Eqpt Loc 004-058,004-070 LMPQ13T, SM258B
[2]SOAMP1, Pack Circuit Eqpt Loc 004-130,004-138 LMPQ03X, SM263	[2]SOAMP1, Pack Circuit Eqpt Loc 004-130,004-138 LMPQ24X, SM263

B.4 APP FIG 6

Removed	Replaced By
CAN(), Pack Circuit, Eqpt Loc 004-146 LMPQ03Y, SM264	CAN(), Pack Circuit Eqpt Loc 004-146 LMPQ23Y, SM264
FLTR(), Pack Circuit Eqpt Loc 004-050 LMPQ03T, SM259	FLTR, Pack Circuit Eqpt Loc 004-050 LMPQ13T, SM259B
PMUINT(), Pack'Circuit, Eqpt Loc 004-018 LMMQ02B, MC2PQ02B1 (SM251)	PMUINT(), Pack Circuit Eqpt Loc 004-026 LMMQ20B, MC2P010B1 (SM251)
PMUMEM(), Pack Circuit, Eqpt Loc 004-026 LMMQ02A, MC2PQ02A1 (SM274)	PMUMEM(), Pack Circuit, Eqpt Loc 004-026 LMMQ20A, MC2P010A1 (SM274)
[2]SIG COM() Pack Circuit, Eqpt Loc 004-058, 004-070 LMPQ03S, SM258	[2]SIG COM() Pack Circuit, Eqpt Loc 004-058, 004-070 LMPQ13S, SM258B
[2]SOAMP1 Pack Circuit, Eqpt Loc 004-130, 004-138 LMPQ03X, SM263	[2]SOAMP1 Pack Circuit, Eqpt Loc 004-130, 004-138 LMPQ24X, SM263

B.5 APP FIG 7
Added
Stop Code to Circuit Pack SWU2.

B.6 APP FIG 8
Added
Stop Code to Circuit Pack +5.1B

B.7 APP FIG 9
Added
Stop Code to Circuit Pack SWU3.

D. Description of Changes

D.1 FS 3, APP FIG 4, replaced PICB INTER(TN629) with PICB INTER(TN629B).

D.2 FS 5, APP FIG 5 and 6, PMUINT1 SM251 and PMUINT() SM251 chang code MC2P002B1 to MC2P010B1. Also PMUMEM1(SM274) and PMUMEN()(274) changed code from MC2P002A1 to MC2P010A1.

D.3 FS 10, APP FIG 5 and 6, replaced SIGCON1 SM258 and SIG COM() s with SIG COM1 SM258B and SIG COM() SM258B.

D.4 FS 11, APP FIG 5 and 6, replaced FLTR1 SM259 and FLTR() SM259 FLTR1 SM259B and FLTR() SM259B.

D.5 Added Note 304.

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OPERATIONS SUPPORT SYSTEM COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

CHANGES

B. Changes in Apparatus (Components)

B.1 Superseded	Superseded By
RTERM1 CIRCUIT PACK SM262	RTERM1 CIRCUIT PACK SM262, OPTION R
RTERM1 CIRCUIT PACK SM262	RTERM1 CIRCUIT PACK SM262B, OPTION Q

D.1 Description of Changes

D.1 APP FIG 5 and 6, information note 303, and FS 13 are modified to reflect the addition of options R and Q.

D.2 Information note 305 is added to note the MFR DISC status of SM262 and the addition of SM262B.

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OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

CHANGES

B. Changes in Apparatus (Components)

B.1 Superseded	Superseded By
PICB INTER CIRCUIT PACK, MC2P004A1(TN629)	PICB INTER CIRCUIT PACK MC2P004A1(TN629), OPTION X
PICB INTER CIRCUIT PACK, MC2P004A1(TN629)	PICB INTER CIRCUIT PACK MC2P004A1B(TN629B), OPTION Y

D. Description of Changes

D.1 In APP FIG 4, information note 303, and FS 3, TN629 is shown as option X and TN629B is shown as option Y to correct drawing.

D.2 Information note 304 is added to note the MFR DISC status of TN629 and the addition of TN629B.

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Directly Connected Test Unit (DCTU) is a microprocessor based system. Its main function is to provide a unified testing system for a number of users in a No. 5 ESS central office (class 5 digital switching system). These users include:

(a) Automated Repair Service Bureau (ARSB)

(b) Switching Control Center (SCC)

(c) No. 5 ESS Trunk and Line Work Station (TLWS)

2. GENERAL DESCRIPTION OF OPERATION

2.01 The DCTU in a No. 5 ESS office provides a dc and sub-audio ac precision measurement capability for the integrated testing of loops and trunks. The DCTU is controlled over a Peripheral Interface Control Bus (PICB) link of the No. 5 ESS Interface Module (IM). The No. 5 ESS Metallic Service Unit (MSU) provides a metallic path from the DCTU to the facility being tested and is controlled by the IM. Access and test messages are transmitted from the ARSB and the SCC to the DCTU by means of separate 2.4K baud data links that are terminated at the No. 5 ESS. Loop and trunk testing is performed by the DCTU's Precision Measurement Unit (PMU). The DCTU consists of the following subunits:

(a) DCTU Controller Circuit

(b) PICB Interface Circuit

(c) one, two, or three PMUs

(d) one, two, or three Equipment Access Networks (EANs)

(e) two to twelve port units

(f) five or six power units

2.02 The DCTU Controller (FS 2) processes test requests, selects a PMU, and sets up a metallic connection via an EAN to the port assigned by the No. 5 ESS Module Controller Unit (MCU). Test requests are then sent to a PMU over an IEEE-488 Bus (GPIB) which connects the DCTU Controller to any PMU. Upon completion of the test (or tests), the metallic path is released and the results are passed to the MCU.

2.03 The PICB Interface (FS 3) enables the DCTU Controller to communicate with the No. 5 ESS, and thus, any of the previously mentioned users. In addition to providing for communication over the PICB, this circuit also enables ports or EANs, and receives alarms or hazardous potential information. Communication between MCU and DCTU is via a serial duplex 2.048 Mbit data link.

2.04 Physical memory of the system can be divided into two sections, the PMU controller and the DCTU controller. The PMU controller section (FS 5) is made up of

a BELLMAC®-8 microprocessor circuit pack, an interface circuit pack, and a bank-switching memory circuit pack. This section can provide up to 104 Kbytes of ROM and RAM. The DCTU controller section is made up of a microprocessor circuit (FS 2) and an interface circuit (FS 3). This section provides up to 240 Kbytes of ROM and RAM. Data communication between these sections is through the GPIB.

®Trademark of Western Electric.

2.05 Through a matrix of relays, EANs (FS 4) enable connection of any port to any PMU. In a 100K line office, up to three PMUs are required to handle the testing traffic and twelve ports are needed for trunk termination.

2.06 Port units (FS 16) provide the interface between the Metallic Test Bus (MTB) and a PMU. It contains circuitry for detecting hazardous potential and communicating information to the controller. The port can also monitor tip-ring for a short to ground and provide the controller with an interrupt. Tracing tones, generated by the controller, are coupled into the tested lines by this circuit.

2.07 Power for the DCTU is supplied from the -48 volt office battery. This voltage is brought into the No. 5 ESS Fuse Panel. From this panel, the -48 voltage is connected into the DCTU control shelf power units (FS 1). These power units are fused dc-to-dc converters which yield positive voltages of 5, 12, 70, and 150, and negative voltages of 12 and 150 volts.

LOOP TESTING

2.08 Actual loop testing is performed by the PMU. The PMU is designed as general purpose hardware not dedicated to any specific test. Specific test functions are performed in the digital signal processing part of the PMU. Test sequences are altered or added by firmware changes, not hardware changes. Test voltages are generated digitally by a microprocessor-controlled digital signal generator (FS 6) and amplified to a usable level by the source amplifiers (FS 14). The PMU can provide signals up to 135V peak at 125 mA from 0 to 3 kHz.

2.09 A loop is measured by applying a voltage from the power amplifiers and measuring the current that flows. The tip and ring of the loop under test are routed through the Core Access Network (FS 15). Loop current flow is measured by the magnetic current sensor circuitry (FS 12) which converts the current to a voltage. The resulting voltage is passed through the Filter Circuit (FS 11) which implements a low-pass filtering function. If the measured voltage is an ac signal, it is then synchronously demodulated from signals provided by the Line Reference Module (FS 7). The result is converted to a digital signal by the Analog-to-Digital Converter (FS 9). This signal is then digitally filtered by the Digital Signal Processor (FS 5). Formatting of data for the Digital Signal Processor is performed by the Measurement Controller (FS 8). The output of the digital filter, usually a current value, is transmitted to the PMU Controller, which formats the results for transmission through the GPIB to the DCTU Controller. The DCTU Controller sends the results back to No. 5 ESS over the PICB data link.

SECTION II - DETAILED DESCRIPTION

1. DCTU CONTROL AND PICB INTERFACE (FS 2, FS 3)

1.01 The DCTU controller circuit pack (FS 2) (SN422) is a single board microcomputer comprising a BELLMAC-8 central processing unit, random access memory (RAM), a programmable interval timer, a programmable interrupt controller, a general purpose interface bus adapter (GPIB), and a long-term tone circuit. Through the BELLMAC-8, the DCTU has an eight-bit data bus and a sixteen-bit address bus which can access up to 64 Kbytes of memory. SN422 uses 16K of this memory space for RAM (12K) and peripherals (4K).

1.02 The PICB interface circuit pack (FS 3) (TN629B) provides the necessary hardware for communicating over a peripheral interface control bus (PICB) to a No.5 ESS interface module and also contains circuitry for floating point processing. This circuit pack has a memory capacity of 208 Kbytes of EPROM and 20 Kbytes of RAM. The address space not used by the DCTU controller is dedicated to decoding the PICB circuitry, the port enables (PTE), and the alarm (ALM) and hazardous potential (HP) signal inputs.

1.03 The switching unit circuit pack (FS4) (SN423), a component of the equipment access network (EAN), comprises a 4x4 matrix made up of LR1 and 353A type relays. Each SN423 provides for connecting three PMUs and one auxiliary pair to four port units (SM248). The auxiliary pair is used during resistive fault sectionalization testing. Three SN423 circuit packs form an equipment access network for the DCTU and provide for PMU and auxiliary connection to twelve ports.

1.04 The port unit (FS16) (SM248) allows the DCTU access to No.5 ESS metallic test bus (MTB) trunks, and provides tip, ring, and sleeve connection, hazardous potential detection, and lighting protection. SM248 can also detect short circuits and can provide long term tone (applied longitudinally or metallically) for pair identification and binder group identification.

2. PRECISION MEASUREMENT UNIT

The precision measurement unit (PMU) consists of three major parts, a control section, a signal generation section, and a measurement section. The control section is microprocessor based and provides supervision for the other two sections. PMU measurements are made by applying a combination of ac and dc test signals through the signal generation section and measuring the resulting loop current through the measurement section. AC signals may be measured broadband (up to 3 KHz) or at single frequencies.

CONTROL

The PMU is controlled through the implementation of controller, memory, and interface circuit packs (FS5). These circuits control external testing, internal diagnostics, administration, and GPIB communication functions. Included in these functions are memory dumping, reset administration, table checking, self calibration, and sanity.

2.01 The PMU controller (SM250), a general purpose processor, provides overall control of the PMU and in addition provides:

(a) Downloading of the proper filter program to the digital signal processor.

(b) Setting up (after downloading) of the DSP to receive data from the measurement controller.

(c) Control of the output of the DSP data.

(d) Selection of the proper channels and applied signals throughout the signal conditioning and digital boards.

(e) Return calculation and formatting of test/result data to the DCTU controller (SM422) via the GPIB bus.

(f) Control of sampling rates and other parameters intrinsically associated with the measurement controller.

(g) Measurement of ac and dc signals.

(h) Selection of the appropriate ac frequencies and ac and dc voltage levels.

2.02 The PMU interface circuit (SM251) provides the digital signal processing for the PMU, PMU reset functions, and PMU memory. Memory capacity for this circuit is 16K of EPROM and 4K of RAM. With the exception of the master reset (0xF800) all system resets are implemented by setting bits at address 0xE400. The various DSP programs are downloaded by using dual-port RAM that can be accessed by both the PMU controller and the digital signal processor. The 16-bit dual-port RAM allows the PMU to store many DSP programs as tables in ROM and then download to the dual-port RAM the proper program for each test. The PMU controller thus has both read and write functions available into the lower and upper 8-bit sections, allowing each section to be written independently. The DSP then uses the RAM as ROM memory.

2.03 The memory board (SM278) supplies the PMU controller with 64 Kbytes of read only memory (ROM). This memory is divided into banks that are dynamically mapped into the processors address space. To achieve this dynamic mapping, the circuit pack contains the hardware to implement a bank switching scheme.

SIGNAL GENERATION

A. Generators

The programmable signal generator (FS6), generates all ac signals that are applied to a loop for testing and also provides for loop signaling. The sinusoidal signals generated are between 1 Hz and 3200 Hz in 1 Hz increments with amplitudes that are fully programmable. Through the use of multiplying D/A converters (MDAC) and a gain range circuit, these signals can range in amplitude from 0 volts to 0.717 volts RMS in 0.0028 volt steps and from 0.719 to 5.377 volts RMS in 0.0225 volt steps. All information necessary for the generation of these signals is transferred to the PSG microprocessor over the PMU's tri-state data bus. In addition to these test signals the PSG also provides for certain timing, addressing, and decoding signals used by the line reference module circuit (SM254).

2.04 The line reference module (FS7), a microprocessor based circuit pack, provides a pair of ac reference signals for the synchronous detection of ac signals in the Tip/Ring measurement channels of the PMU. Since separate measurement channels are used, one for tip and one for ring, two line reference modules (LRM) are needed for each PMU. The ac reference signals consist of quadrature sine and cosine functions with output amplitude fixed at 9 volts peak, and frequency selectable between 1 Hz and 3200 Hz in 1 Hz increments. All information necessary for the microprocessor to generate sinusoidal signals is transferred to it via the PMU's tri-state data bus. The LRM circuit also generates any dc level from 0 volts to 0.9648 volts in 0.035156 volt steps using a MDAC. Positive or negative 9 volt reference for this MDAC is selected through a relay.

B. Power Amplifiers

The source amplifier circuit board (FS14) is an analog amplifier consisting of a preamplifier, a power amplifier, an overload protection circuit, and associated logic circuitry for relay control. This circuit pack is used to energize the tip and ring conductors as required by the trunk or loop circuit tests. Each PMU contains two source amplifier circuit packs; one each for tip and ring measurement channels.

2.05 The preamplifier stage receives signals from the FSG source board (SM253) then provides selection of ac or dc input signals, gain adjustments, and a low impedance source for driving the power amplifier stage. This power amplifier stage consists of a non-inverting high gain amplifier, transistors, relays, and RC components. A relay configures the power amplifier from either the tip or ring source preamplifiers. Distinguishing between tip and ring channels is accomplished by backplane wiring differentiations.

C. Termination

Two separate circuit boards provide the tip and ring terminations (FS13) necessary for loop testing.

2.06 The tip termination unit (TTU) circuit pack (SM261) is composed of two circuits. The first circuit is a set of resistors and capacitors which provide suitable terminations for electrical tests on subscriber loops. The second is a sanity amplifier which can be used as a movable voltage probe by actuating appropriate relay contacts.

2.07 The ring termination unit (RTU) circuit pack, SM262B, is composed of three circuits. The first circuit, like the TTU R-C networks, provides termination for electrical tests. The second is a constant current sink which is used to draw and break dial tone. The third supplies dc voltage in series with the central office battery voltage. This extra voltage increases the resistance range over which dial tone can be drawn.

MEASUREMENT

Measurement in the PMU is done using filtering, signal conditioning, signal conversion, and data conversion of loop current magnetically sensed through the ferrite cores.

A. Tip/Ring Filtering

Bandlimiting and anti-aliasing functions are implemented through analog active filters. The main filtering process is done using the digital signal processor (DSP), a VLSI component.

2.08 The core-access network circuit pack (FS15) (SM264) provides the facilities for switching various conductors of two distinct loop pairs (S0 Tip/S0 Ring and S1 Tip/S1 Ring) to the two magnetic current sensor channels on circuit pack SM260. Provisions are also available for applying various sanity and diagnostic terminations to the two current sensor channels.

2.09 The current sensor circuit pack (FS12) senses and measures loop current by converting currents detected on the tip and ring side of the loop under test to linearly proportional voltages. Two 2-core transformers are used to sense the loop conductor current. A loop current is passed through a transformer and due to opposite winding polarities causes opposite reactions in each core thereby creating a voltage differential. This differential is read by an operational amplifier which produces the corresponding output voltage.

2.10 After the tip and/or ring signals are conditioned and formatted they are input to the DSP (part of SM251). The DSP is a 40-bit HMOS signal processor. In conjunction with programs downloaded into the dual-port RAM and address/data multiplexing logic the DSP performs the final signal processing for the PMU. The result of this signal processing is the measured loop current.

B. Signal Conditioning

Reference signals, generated by SM254, are used by the circuitry discussed in this section for conditioning of the loop signals.

2.11 The filter unit (FS11) restricts the bandwidth of the PMU current measurement section to voice band, dc to 3200 Hz. This function reduces out of band noise energy and provides anti-aliasing for the PMU digital filter 8 KHz sampling rate. These 6th order low pass filters are made up of three second order sections. The filters have a flatband corner frequency at 3200 Hz and are 20 db down at 4 KHz. SM259B also contains 60 Hz notch filters that may be switched in or out depending on the test being run and the presence of excessive power line noise coupling into the loop under test.

2.12 The signal conditioner circuit pack (FS10) isolates a signal of interest with respect to frequency. If the desired signal is dc, the conditioning is simply additional low pass filtering. If the signal is ac then it is translated to dc by multiplying it with reference signals generated by the line reference module (FS7) and then low pass filtered for conditioning. A broadband signal may be passed for subsequent noise power measurements. Auxilliary circuits include programmable gain amplifiers for boosting weak signals and latching saturation detectors which cause alarms if voltages exceed the defined linear range of the analog circuits.

C. Data Formatting and Conversion

This section describes the measurement controllers (FS8) and data converter (FS9) circuit packs which provide analog to digital conversion and twelve bit to twenty bit formatting.

2.13 Circuit packs SM255 and SM256 perform the function of sequencing and controlling the operations of the PMU circuitry associated with loop current measurement. Assertion of the B_U_CLKB signal by the PMU controller (SM250) causes the SM255 and SM256 to cycle through a series of states to acquire voltages from the analog boards, convert the analog signal into a digital representation (A/D),

normalize this representation into a standard twenty bit format, and transmit the result to the digital signal processor on SM251. Circuit pack SM255 contains the state generator for sequencing the measurements. Timing signals are input to SM256 indicating when certain operations are to take place.

2.14 The data converter circuit pack (FS9) converts analog signals into a digital stream. The two input analog signals are constrained to 8.00 volts in magnitude. These signals are each buffered and connected to a two-to-one analog multiplexer. Sample and hold functions can be applied to these signals through software control (SM255). Either signal may be switched to the output of the multiplexer and then fed into the programmable gain amplifier (controlled by SM256). The purpose of the programmable gain amplifier is to maximize the voltage applied to the A/D converter without overloading the converter input buffer. Maximizing the A/D converter input increases the number of significant bits in the converter digital output.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Environmental Limits

(a) Temperature

(1) Operating temperature (long term): 40°F to 100°F

(2) Operating temperature (short term): 35°F to 120°F

(b) Humidity

(1) Humidity (long term): 20 to 55 percent

(2) Humidity (short term): 20 to 80 percent

(c) Maximum Testable Circuit

Maximum Testable Metallic Test Bus plus Loop: 3000 ohms or 100 Kft.

(d) System Current Requirements

(1) Typical: 15 amperes

(2) Maximum: 20 amperes

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 None.

4. CONNECTING CIRCUITS

4.01 Connecting information is contained in the following documents.

(a) Electronic Switching Systems No. 5 — Module Controller Unit Circuit — SD-5D040-01

(b) Electronic Switching Systems No. 5 — Fuse Panel Circuit — SD-5D034-01

(c) Electronic Switching Systems No. 5 — Metallic Service Unit Circuit — SD-5D033-01

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are covered in X-79805. Burn-in requirements are covered in X-79848.

SECTION IV - REASONS FOR REISSUE

Changes

B. Changes in Apparatus (Components)

B.1 Added

R1 resistor,
KS20616L1A, 3480 Ω
APP FIGs 5 and 6

D. Description of Changes

D.1 The following is to provide correct backplane information.

(a) A hardwire strap from control shelf EQL 004-010, 021 and EQL 004-010, 120 to EQL 004-018, 021 and EQL 004-018, 120 is added.

(b) Hardware connections are removed from 004-010,006 and 004-010,106 and added to 004-026,006 and 004-026,106.

(c) Resistors are added to backplane pins 004-034,106 and 004-042,006.

(d) APP FIG 5 and 6 are modified.

(e) A hardwire strap is added between control shelf EQL 004-010, 148 to EQL 004-018, 148.

D.2 The following changes reflect the addition of options X and Y, which allow the use of TN629B. TN629 is manufacture discontinued.

(a) Information Note 303 is modified.

(b) Information Note 304 is added.

(c) APP FIG 4 is modified.

(d) FS 3 is modified.