COMMON SYSTEMS
T1 LINE MONITOR

CHANGES

B. Changes in Apparatus

B.1 Superseded	Superseded by
2 - Lamps DS1, DS2 - CPS 1, RM-795831 MPS-132564 (Drake Mfg.)	2 - Diodes CR13, CR14 - CPS 1, 534A

D. Description of Changes

D.1 In CPS 1, lamps DS1 and DS2 have become difficult to obtain. This change permits substitution of the 534A light-emitting diode (LED) with mounting holders for the lamp. Use of the diode instead of the incandescent lamp requires changing the values of the series resistors, R33 through R36, from 1 kilohm to 1.8 kilohms on a line-out basis. Reference to Note 107 was added.

D.2 Circuit Note 107 was added.

D.3 A record of changes table was added.

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CHANGES

D. Description of Changes

D.1 Circuit Note 102 was revised to clarify application.

D.2 In FS1, lead designation information was revised to clarify interconnection with other circuits.

D.3 In FS1 (and APP Fig. 1), the value of resistors R11, R12, R14, and R15 (all KS-16645, List 1) was changed from 1200 ohms to 820 ohms.

D.4 In CPS1, the values of resistors R8 and R10 were changed from 470 ohms to 680 ohms, and R37 and R38 were changed from 47 kilohms to 68 kilohms (all codes remain KS-13490, List 1).

D.5 In CPS1, the code of transistors Q1 and Q2 was changed from 66J to 66F.

D.6 In note 4 of CPS1, the value of 1500 ohms was added to the table, and the value of 15000 ohms was removed from the table.

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D. Description of Changes

D.1 In CPS 2, Sheet Note 3 was added.

D.2 In CPS 2, new values of R11, C1, C2, and C3 were optionally specified, per Note 3, resulting in a new plug-in unit designated VIOLATION RATE ALARM-R2.

D.3 Equipment Note 202 was revised.

D.4 In FS 1, CP 2 was changed to show R1 OR R2.

F. Changes in Description of Operation

F.1 In SECTION II, Part 6, add paragraph 6.04 as follows:

"6.04 The violation rate alarm R1 version triggers at a violation rate of about one per million and responds to severe failures in about 1.3 seconds. The R2 version triggers at a rate of about one per hundred thousand and responds to severe failures in about 0.3 seconds."

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CHANGES

D. Description of Changes

D.01 In CPS 1 and TSB, interconnection information was corrected or added to agree with the manufacturing information.

D.02 In FS 1, terminal designations were added to agree with the manufacturing information.

D.03 In FS 1 and CPS 1, the standard values of components were changed to agree with the manufacturing information.

D.04 In FS 1, APP FIG. 1, CPS 1, and CPS 2, drawing corrections to make schematics and apparatus lists agree with each other and with the manufacturing information were made.

D.05 In FS 1, control and display designations were changed to agree with standards and with the manufacturing information.

D.06 In CPS 1, Sheet Note 4 was changed to add a new resistor value to the selection table.

D.07 In FS 1, schematic references were removed from the signal transfer connections.

D.08 In FS 1, drawing corrections on the transfer representations and designations were made.

D.09 In FS 1, connecting information and reference to Notes 104, 105, and 106 were added.

D.10 Circuit Notes 103, 104, 105, and 106 were added.

D.11 Information Fig. 101 was revised.

D.12 Information Fig. 102 was added.

F. Changes in Description of Operation

F.1 In SECTION II, Part 6, paragraph 6.01, the first sentence of paragraph 6.01 should end as follows:

"...stretched (35 millisecond) pulses which are amplified by Q6 and are provided (in differentiated form) at the COUNT jacks J1 and J2."

F.2 Paragraph 6.02 and 6.03 were added as follows:

"6.02 The inhibit circuit (Q7) receives a positive transition when the detector relay (K2) is released. This produces a negative pulse which temporarily blocks the triggering of the pulser circuit, and also drains some voltage from the accumulation capacitor C1. These actions prevent immediate retriggering of the threshold circuit when it releases.

"6.03 Transfer contacts on the control relay (K3) put a voltage charge from pin 13 on capacitors C2 and C3, and when the control relay operates, these capacitors with their charge are transferred to pin 20 to temporarily sustain the trigger input voltage of the threshold circuit."

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COMMON SYSTEMS
T1 LINE MONITOR

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The T1 line monitor is a unit which detects pulse format violations on a working T1 line. The monitor circuit is bridged across the working line with high impedance tap resistors and detects both bipolar violations and occurrences of 16 consecutive zeros on the T1 line. The monitor can be wired to a specified T1 line or be shared by several lines, using patching jacks to provide the input connection. The monitor has lamps to indicate the occurrence of bipolar and pulse absence violations. It also has provisions for triggering relay circuits if the violation rate exceeds a predetermined value. The relays can actuate external alarms and controls, and there are lamps on the monitor which indicate the state of the relay circuits.

SECTION II - DETAILED DESCRIPTION

1. T1 LINE MONITOR UNIT - GENERAL

1.01 The input signal goes through a jack J1 which provides an alternate input into the violation detector circuit pack. The detected line pulse violations go to the violation rate alarm circuit pack which processes the violations to detect line troubles. Indication of trouble is sent back through the violation detector pack to operate a detector relay K2 and lamp DS4.

1.02 The detector relay will operate a control relay K3 and lamp DS3 if they are enabled by connecting terminals 53 and 54 together. The control relay can be set to stay operated until manually released by switch S2. A switch relay K4 is slaved to the control relay, and it is arranged to transfer a transmission path from the regular to a standby input. An alarm relay K1, which is normally operated, will be released by a line failure operating the detector relay or by a power failure. Alarm outputs are provided when the alarm relay is released, but the alarms can be cut off by a manual switch S1 which operates the alarm relay. A lamp DS2 indicates that the alarm cutoff switch has been operated.

1.03 Most of the electronic circuits operate across a +4.2 volt potential derived from the -48 volt office power. This low voltage is maintained between -48 volts and -43 volts by using shunt varistor regulation (RV1-6). Inductor L1 and capacitors C1, C2, and C3 provide filtering for rejecting high frequency interference in the power circuits. Maximum current drain is approximately 500 mA, and the unit is protected by a 70A fuse rated at 1-1/3 amperes.

2. INPUT CIRCUIT (ON VIOLATION DETECTOR PACK - PART OF CP 1)

2.01 The input amplifier of the T1 line monitor consists of two saturated, inverting amplifiers, one amplifier for each side of the winding of a transformer. The output of each amplifier (representing either all the positive or all the negative pulses on the bipolar line) is fed to a 400-ns monopulser which responds to only the leading edge of the incoming pulse. The 400-ns pulse is then fed to and processed by the bipolar monitor and absence monitor.

2.02 The input of the circuit is coupled to the tapping line through a type 2560AL, 1:1 transformer T1. To match the impedance of the length of tapping cable, the secondary is terminated in two 50-ohm resistors R7 and R9 and is then ac coupled into the base of the amplifying transistors Q1 and Q2. Since the voltage developed on these lines is less than VBE of the transistors, the bases are biased at 0.6 volt through 100D varistors RV1 and RV2. These varistors provide temperature compensation for the circuit as the drop across them tracks with VBE.

2.03 If the pulse at the base of Q1 (Q2) is positive, the transistor turns on and is driven into saturation. Since a positive pulse on one side of the secondary appears as a negative pulse on the other (and vice-versa), and since the transistors only respond to positive pulses, the amplifiers also provide polarity separation. The output of the amplifier represents the inversion of all the positive (negative) pulses of the bipolar input.

2.04 The stream of amplified pulses is then fed through Q3 (Q4) to the inverting gate G1 (G2). Base bias for Q1 and Q2 is obtained from the voltage on C5 and C4. This voltage is provided by current through R6 and R5, depending on the average output level, and it is also provided through CR4 or CR3 during signal input pulses. The common collector stage Q3 (Q4) provides sufficient level shifting to insure that the amplifier output drops below the RTL level threshold. The output of the inverter G1 (G2) is a stream of positive pulses representing the positive (negative) bipolar pulses on the T1 line. This pulse stream is fed to a 400-ns monopulser made up of three RTL NOR gates. Gates G3 and G4 (G6 and G5) are connected as a set-clear flip-flop. The monopulser input can be thought of as the clear lead, and the output as the ZERO lead. The ZERO output of the flip-flop is inverted and coupled to an integrating capacitor C2 (C3) and to the set lead of the flip-flop. It is this connection that provides the single stable state of the circuit, and the capacitor determines the pulse width.

2.05 Assume the flip-flop is in the set state initially, and at some time T1 after zero, a pulse arrives at the clear input. The flip-flop is driven into the clear state, and the inverted ONE output is integrated across C2 (C3). When the integration reaches the logic threshold, gate G4 (G5) is driven low. When the input pulse ends, the flip-flop returns to the set state. If the pulse is long enough to set the flip-flop (30 ns) the monopulser output is unaffected by the width of the incoming pulse.

3. BIPOLAR CIRCUIT (ON VIOLATION DETECTOR PACK - PART OF CP 1)

3.01 The bipolar circuit detects bipolar violations by comparing the polarity of the existing pulse with that of the pulse immediately preceding it. The circuit outputs a 400-ns positive-going pulse if a bipolar violation occurs. The output of the circuit is inhibited by a +3 volt level on the inhibit (INH) lead, and the logic is initialized after the inhibit level falls such that, regardless of polarity of the first pulse registered, the circuit is not enabled until the second pulse is on the line.

3.02 The two pulse streams from the input amplifier are fed to the set and clear inputs, respectively, of flip-flop B1 and also into gate G9, whose output drives the toggle lead of flip-flop B2. The ONE output of B1 drives the set lead of B2, and the ZERO output drives the clear lead. The two outputs of B2 drive NOR gate G13 and provide an error condition when both ONE and ZERO of B2 are zero.

3.03 If a pulse comes in and sets flip-flop B1, by the nature of the circuitry, the ZERO output of B2 is forced to zero, however, B2 will not set unless the toggle lead is coincidentally high. The same is true for a pulse of the "opposite" polarity which will clear flip-flop B1 and thus hold ONE of B2 at zero. Assume the flip-flops are both cleared initially, and at time T1, a pulse appears on the set lead of B2 (representing a positive pulse on the bipolar input). The leading edge of the pulse causes B2 to toggle to the set state before the first flip-flop B1 is set. Since at no time were ONE and ZERO of B2 both zero, no error pulse was generated. Now assume at time T2 that a pulse (representing a negative pulse on the bipolar input) arrives on the clear lead of B1. Again, the leading edge of the pulse toggles B2 before B1 is set and no violation pulse is generated. Assume a third pulse arriving also appears on the clear lead of B1 (representing a negative pulse and, therefore, a bipolar violation). The leading edge of the pulse will toggle B2 but will leave B1 in the clear state. B2 will attempt to toggle to the set state, however, the ZERO output (which is high in the clear state) of B1 holds ONE of B2 at zero, which constitutes an error situation. Gate G13 will go high and stay high until flip-flop B2 returns to the clear state after the falling edge of the incoming pulse.

3.04 The inhibit operation is initiated by the flip-flop B3 going to the set state, forcing the expander gate G14 to zero (forcing G13 to zero). B3 is not cleared until the inhibit line falls and the trailing edge of a T1 pulse appears at the input. Flip-flop B3 is cleared by the output of a monopulser which is triggered by the trailing edge of a T1 pulse. The monopulser is composed of gates G10, G11, and G12, and operation is the same as the monopulsers in the input amplifier.

4. ABSENCE CIRCUIT (ON VIOLATION DETECTOR PACK - PART OF CP 1)

4.01 The absence circuit is a resettable five-stage binary counter driven by a 1.544-MHz clock which outputs a 400-ns pulse if there is a string of 16 or more consecutive zeros on the input line. The counter is reset by a pulse on the line, a presence violation pulse, or the inhibit level, +3 volts.

4.02 The two input pulse streams are gated together by gates G15 and G17 which all set inputs of the five-stage counter, the inhibit flip-flop B9, and one input of gate G22. The output of gate G15 also drives a 200-ns monopulser whose output is, in turn, gated with the clock pulse in G21. The monopulser output insures the resetting of the counter immediately after the end of the incoming pulse. The output of gate G21 is gated with the output of gate G17 by gate G22, and the output of that gate is inverted to drive the clock input of the counter.

4.03 The counter is composed of flip-flops B4 through B8 cascaded to form a five-stage binary counter the last stage of which, together with the output of the inhibit flip-flop B9, controls gate G24. If the output of G24 goes to a ONE, a 400-ns monopulser made up of gates G25, G26, and G27 fires.

4.04 If a pulse is present on the line being monitored, a presence violation pulse is generated, or the inhibit lead goes to +3 volts, the set input and, consequently, the toggle input of all stages is forced high. Under this condition, all flip-flops B4 through B9 are set. When the violation pulse, line pulse, or inhibit line drops, the 200-ns monostable toggles the first stage of the counter to the clear state, and each stage after that toggles the next stage to the clear state. When the ONE output of B8 goes high (indicating the counter is reset), it clears the output inhibit flip-flop B9 to allow gate G24 to respond to the counter output.

4.05 The counter now follows the internal 1.544-MHz clock and registers 16 clock pulses. On the 16th clock pulse, an error pulse is generated and resets the counter as above. The worst case exists when the leading edge of the clock pulse coincides with the leading edge of the 200-ns monostable. Since the monostable output forces the counter unconditionally to reset, this clock pulse is ignored, and the count to 16 does not begin until the leading edge of the next clock pulse. Under this condition, the presence detector may allow a string of 16 consecutive zeros; it will not at any time, however, produce an error pulse for a stream of 15 zeros.

4.06 If there is no line present, or if the line has no pulses present on it at all, the presence violation rate immediately rises to its maximum 90,824 Hz.

4.07 The 400-ns violation pulses from the presence detector and the bipolar detector are gated together by gates G28 and G29 to give positive-going 400-ns totalized violations.

5. MISCELLANEOUS CIRCUITS (ON VIOLATION DETECTOR PACK - PART OF CP 1)

5.01 The violation lamps DS1 and DS2 are turned on by a 100-ms pulse which is the output of pulse stretchers Q6,7 and Q8,11 that respond to the 400-ns violation pulses.

5.02 The clock circuit is a crystal controlled Colpitts oscillator which drives an inverting amplifier. The output of Q10 is a 4-volt 200-ns pulse at 1.544 MHz. This signal is sufficient to drive the RTL logic. The output is fed to gates G21 and G30. The output of gate G30 is brought out to pin 2 as a test point and for use in external devices.

5.03 The relay driver circuit is normally off and is turned on by a positive voltage at its input (terminal 15). When Q5 is turned on, it provides current to the detector relay circuit of the monitor through the collector (terminal 9).

6. VIOLATION RATE ALARM PACK - CP 2

6.01 The 400-ns positive pulses (from the violation detector pack) representing T1 line violations trigger the pulser circuit (Q1, Q2), producing stretched (30 us) pulses which are amplified by Q6. These pulses go through R11 and CR3 and are accumulated as a positive voltage on C1. When this input voltage exceeds a certain threshold (voltage across R10 plus the base-emitter voltages of Q3 and Q4), it triggers the threshold circuit (Q3, Q4, Q5) on, turning off Q5 and producing a positive voltage at the output.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The supply voltage is nominally -48 volts but may vary from -42 to -53 volts.

1.02 The input signal is a sequence of negative and positive pulses from a T1 line which occur at a maximum rate of 1,544,000 per second. Average width of the pulses should not exceed 400 ns, and the pulse height should be between 0.1 volt and 0.35 volt.

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 The monitor is connected to a working T1 line and detects bipolar violations and sequences of 16 time slots without a pulse.

3.02 The monitor accumulates violations over a short-term period and activates an alarm if the violation rate is excessive.

3.03 The monitor can switch to an alternate line if violations trigger an alarm and the alternate line is functioning properly.

4. CONNECTING CIRCUITS

4.01 Digital Transmission Facilities Patch and Cross-connect Interconnection Circuits - SD-99503-01

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are specified in X-78613.

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