7

ELECTRONIC SWITCHING SYSTEMS

NO. 3

PERIPHERAL CONTROL
CIRCUIT

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The peripheral control circuit (PCC) performs the interfacing function between the high-speed central control (CC) and the relatively low-speed peripheral equipment. The PCC is the buffer circuit that receives orders from the CC, executes these orders, and returns appropriate responses to the CC.

1.02 Two PCCs are provided on each control frame. One PCC functions under control of CC 0 while the duplicate functions under control of CC 1.

1.03 Four special circuits are incorporated into the PCC. The frame input/output controller (FIOC) is the interface between the high-speed serial I/O channel of the CC and the rest of the circuits that make up the PCC. The peripheral pulse distributor (PPD) generates the low-speed serial messages to the peripheral decoders, which control

relays in the peripheral equipment. The network controller (NC) generates the signals that control the crosspoints in the network fabric. The scan controller (SC) reads out the state of ferrods that indicate requests for service, supervisory states, alarms, and other data required by the CC.

2. GENERAL DESCRIPTION OF OPERATION

FRAME I/O CONTROLLER

2.01 The FIOC is the interface between the four high-speed serial subchannels from the CC and the rest of the PCC. This relationship is shown in Information Note 304. Four coaxial cables, one for each subchannel, carry information from the CC to the FIOC. A fifth cable, not associated with any particular subchannel, carries the reply back to the CC. Each subchannel is associated with a particular circuit within the PCC. Messages on subchannels A and D are directed to the SC (low half and high half, respectively). Messages on subchannel B are directed to the PPD, and messages on subchannel C are directed to the NC.

PERIPHERAL PULSE DISTRIBUTOR

2.02 The 6.7-volt 0.45-USEC pulses that drive the peripheral decoders are generated by the PPD. The PPD receives address and control information from the FIOC. It selects one of 256 outputs and drives the selected output with a positive or negative pulse according to the input received (see Information Note 305). Each message from the FIOC results in a single pulse on one of the PPD outputs. Seven such pulses make up a complete message to the peripheral decoder. The PPD sends reply data back to the FIOC. This consists solely of checking and maintenance information, thus allowing the CC to verify proper operation of the circuit.

2.03 The PPD and the duplicate PPD in the mate PCC function independently and are paralleled only at the outputs. This prevents faults in one PPD from affecting the operation of the duplicate. In offices having more than seven network frames, the PPD in the second control frame provides another set of 256 outputs.

NETWORK CONTROLLER

2.04 The NC works with the remreed pulser circuit and network access circuits to control the crosspoints of the network fabric. The output of the NC consists of control signals to the pulser and a large number of selection signals that are required to steer the pulser output through a particular combination of control windings in the network switches. Input messages to the NC are received from the FIOC. Two messages are used to define the operation to be performed. After the operation is completed, a third message directs the NC to return the contents of internal registers that contain the results of checks made during the course of the operation. Additional messages from the FIOC are used to set up various maintenance states in the NC.

2.05 The NC and the duplicate NC in the mate PCC function independently except for enabling logic, which allows each NC to control the internal power of both NCs. The outputs from the duplicated NCs are logically combined in the access circuits and network switches.

2.06 The NC in the first control frame controls the network fabric on the first seven network frames and the associated third-stage switches, which are located on the control frame. In offices having more than seven network frames, the additional frames are controlled by the NC on the second control frame. In this case the control of the third stage is split with each NC controlling half of the third-stage switches.

SCAN CONTROLLER

2.07 The SC generates interrogate pulses for rows of ferrods and detects the responses. The SC receives address information from the FIOC, selects one of 256 rows, and drives the selected row with a bipolar interrogate pulse. The responses from the 16 ferrods in the accessed row are detected and returned to the FIOC. The rows of ferrods are divided into eight blocks of 32 rows called logical scanners. Each logical scanner is served by a detector circuit pack in the SC. Information Note 314 shows the overall SC organization.

2.08 Two subchannels from the CC are used to access the SC. Logical scanners 0 through 3 are accessed over the first subchannel, and logical scanners 4 through 7 are accessed over the second.

2.09 The SC and the duplicate SC in the mate PCC function independently with two exceptions. The enabling logic is interconnected to allow each SC to inhibit or enable the operation of both SCs. Also, certain maintenance orders involve simultaneous access in both SCs.

2.10 The SC in the first control frame accesses the master scanner (logical scanner 0) and the logical scanners in network frames 1 through 7. In offices having more than seven network frames, the logical scanners in the additional frames are accessed by the SC on the second control frame.

SECTION II - DETAILED DESCRIPTION

1. FRAME I/O CONTROLLER

1.01 The FIOC consists of three functional blocks: a receiver-transmitter that communicates over the serial subchannels, a sequencer that controls the overall operation of the FIOC, and a register that converts the serial message to parallel form and converts the parallel reply data to serial form. Incoming messages are placed in parallel form on a data bus within the PCC. One of four enable leads (GCTL0 through GCTL3), depending on the subchannel in use, is then activated. The enabled circuit (SC, PPD, or NC) then performs a function based on the data received, presents reply data to the FIOC over a set of leads that is unique to each circuit, and informs the FIOC that the data is ready by activating the associated reply enable lead (RDGCT0 through RDGCT3). The FIOC loads the data from the proper set of reply leads and transmits the reply message to the CC over the reply cable. Clocking for all FIOC functions is derived from the subchannel from the CC, which continues sending a string of zeros until the complete reply is received in the CC.

RECEIVER - TRANSMITTER - FS 1

1.02 The receiver recovers the data and timing from the four serial subchannels from the CC. It provides the serial data input and clock to the shift register, the state clock and control signals to the sequencer, and a clock signal to the PPD and NC. The receiver also provides the timing signals used by the transmitter.

1.03 The transmitter gets an enable signal from the sequencer and data from the shift register via the sequencer and combines these with timing signals from the receiver to generate a reply to the CC.

SEQUENCER - FS 2

1.04 The sequencer provides the control signals for the internal operation of the FIOC and the enable signals for the other circuits of the PCC. Operation of the sequencer is described in Information Note 304.

REGISTER - FS 3

1.05 The register circuit packs contain the shift register, a set of latches for holding the received message, and a data selector for loading reply data into the shift register. The register is partitioned onto two circuit packs with each pack handling eight data bits and the associated parity bit (the three shift register bits that hold the start code are located in the sequencer). Each register pack provides nine outputs (eight data bits and one parity bit) to the data bus that goes to the other circuits of the PCC. A separate set of reply data leads is provided for each circuit with the sequencer controlling which set is selected (diagnostic orders can also load status information from the mate FIOC). The register circuit packs provide parity checking on the received message and parity generation for the reply.

2. PERIPHERAL PULSE DISTRIBUTOR

2.01 The PPD consists of several functional blocks as shown in Information Note 306. The PPD matrix consists of 256 transformers arranged in a 16-by-16 matrix with each transformer providing one of the 256 outputs. The matrix is accessed by horizontal and vertical translators and drivers, which receive data from the FIOC and signals from the PPD control and timing block.

CONTROL AND TRANSLATION - FS 4

2.02 The PPD control governs the sequence of operations according to the timing sequence shown in Information Note 307. Upon receipt of an enable signal from the FIOC, the control first enables the vertical translator. The vertical translator sends two signals to the vertical driver selected by the 1-out-of-32 decoder. One signal turns on the driver while the other removes the ground termination from the selected vertical. After a delay to allow transient currents to subside, the sequencer strobes the current sense outputs from the level control (FS 5) into an internal register. No current should be flowing in the matrix at this time. The horizontal translator is then enabled, turning on one of the horizontal drivers and beginning the output pulse. At the end of the horizontal selection interval, the current detectors are examined again, and the horizontal selection is turned off, thus ending the ouput pulse. The vertical translator is then turned off, and the reply enable lead to the FIOC is activated.

2.03 The reply from the PPD consists of checking information as shown in Information Note 307. The six bits of the timing counter, checks on the vertical and horizontal selection, and the results of the two examinations of the current detectors are returned.

DRIVERS - FS 5

2.04 The level-control circuit pack is the source of the drive current for the PPD matrix. The current flow is from lead SENS of the level-control board, through the selected vertical driver, through the transformer matrix, and back through the selected horizontal driver to the COM lead of the level-control board. The

level-control board monitors, via three threshold detectors, the current being drawn from the SENS lead and provides these indications (marginal, intermediate, and normal level) to the PPD control. In normal operation the COM lead has a low impedance to ground via the level-control board, but diagnostic orders can add resistance to this path to reduce the current to the marginal level.

2.05 Each of the 33 vertical drivers consists of two parts. One provides a low-impedance path from the SENS lead to the selected vertical, and the other provides a resistive ground termination that is normally turned on for the nonselected verticals and turned off for the selected vertical. This permits detection of shorted diodes and other faults in the matrix that would show as leakage between two verticals. One of the 33 vertical drivers, the false vertical, bypasses the matrix to permit exercise of the rest of the access circuitry without generating output pulses.

2.06 The horizontal drivers provide a low-impedance path from the selected horizontal to the COM lead of the level-control board. Horizontals are terminated with a high impedance to +24 volts to keep the stray capacitance on the horizontal multiples charged when not selected.

MATRIX - FS 6

2.07 The PPD matrix consists of a 16-by-16 array of transformers. A particular transformer is selected by providing a ground on the proper matrix horizontal and a positive voltage on one of the two verticals of the transformer. Which one of these two verticals is selected depends on the polarity desired for the output pulse. Two diodes associated with each transformer block sneak paths through the matrix. The matrix is partitioned with 16 transformers on each circuit pack. Each vertical multiple is entirely within a circuit pack while the horizontal multiple picks up one transformer from each circuit pack used.

3. NETWORK CONTROLLER - FS 7 THROUGH FS 16

3.01 The functional block diagram of the network control is shown in Information Note 308. There are seven major circuit functions and each will be discussed in this description of how the network control handles one network order.

3.02 All the data required to execute one network order is contained in two 21-bit words. Nineteen bits of each word are used by the network control and are received via the frame input-output circuit over a parallel bus. Five bits (PH, 13, 12, 11, and ST2) of word 1 (see Information Note 313) contain information that indicates the type of order to be executed by the network control. These five bits are registered and decoded on the FA1001 circuit pack. There are six basic network orders that are used to control the fabric (see Information Note 313). They are:

(a) A - Close Stage I and II

(b) RLS2 - Open Stage I and II

(c) 3 OPR - Close Third Stage

(d) 3RLS - Open Third Stage

(e) HD - High and Dry

(f) FCG - False Cross and Ground

3.03 The remaining orders, out of a total of 16 possible, are used for maintenance or power enabling. Not all 16 are used at present.

3.04 The two highest order bits (14 and 15) indicate to the controller which word is being received. These bits are registered and used for control by the FA1001 control circuit pack.

3.05 The remaining 12 bits contain part of the data needed by the controller to execute the order indicated by the order field. The remaining data is contained in word 2 and will be explained later. The lower half of word 1 (bits 0 through 7 and PL) contains the concentrator group and input level binary fields. The input switch group field is given by bits 8, 9, and 10. These data are registered and decoded by circuit packs FA998, FA999, and FA1000 as indicated in Information Note 308.

3.06 These circuit packs perform the three major functions of registering, decoding, and driving. The register circuits store the data from the frame input-output circuit in binary form under control of FA1001. The decoder circuits decode each of the binary fields, with parity, into 1-out-of-N outputs. Both of these functions are accomplished using low-level 1A logic. The driver circuits follow the 1-of-N low-level logic outputs. (See Information Note 311 for a typical driver circuit.) These circuits perform the function of raising the low-level logic signals to the higher voltage and current levels required to drive the gate circuit of the PNPN devices that are used in all the access circuits and network switches. In addition, these circuits provide the means whereby the currents supplied to the gates of the PNPN devices can be monitored by discrete circuitry contained on FC219, which are called group check circuits. These circuits will be discussed later.

3.07 As already discussed, the driver output of the decoder/driver circuit packs controls the gates of PNPN devices that in turn control the actual pulse path.

3.08 The remaining data for one network order is contained in word 2. Bits 0 through 7 contain the output level and output switch fields. The input switch number is contained in bits 8, 9, and 10. These data fields are gated into the various decoder/driver circuit packs under control of FA1001.

3.09 Once both words 1 and 2 have been received without error, the controller activates the group check circuits and voltage supplies. When this happens, gate voltages are applied to all the PNPNs that are required to select the desired pulse path. See Information Note 309 for a typical concentrator-group pulse-path selection, and Information Note 310 for the third-stage pulse path. The required nodes for the various access circuits and switch groups are also turned on at this time. A time delay of about 1.5 ms is initiated at the same time that all the voltages are applied. During this time delay the gate current in each of the selected PNPNs reaches a normal steady state value of about 23 mA.

3.10 If all of the currents are normal, each of the eight group-check circuits on FC219 senses this fact and the outputs will be low. At the end of the time delay, these outputs are gated into the upper eight bits of the transmit register on FA1001.

3.11 The control logic checks that all group checks are good and if so a start signal to the remreed pulser circuit is activated. The pulser then generates a current waveform as indicated in Information Note 312 through the PNPNs selected. When the current level of the pulser reaches the 1-ampere level, the voltage sources and the group-check circuits are turned off. The selected path remains held via PNPNs until the current drops to 0.0-ampere. The current generated operates the remreed crosspoints and they in turn remain operated after the current goes to 0.0 ampere, thus establishing a path. If the current from the pulser reaches the normal maximum value, a POK signal is sent from the pulser and registered on FA1001. The network control remains in a fixed state with the transmit register containing group-check information and the lower eight bits containing progress marks (see Information Note 313) until interrogated later.

3.12 When the network controller receives word 3, all of the contents of the transmit register on FA1001 are sent back to the central control via the frame input-output circuit. Word 3 also signals the network controller to go to the cleared state in preparation for further orders.

4. SCAN CONTROLLER

4.01 A block diagram of the scan controller is given in Information Note 314. The interrogate matrix is a 16-by-16 array of transformers, each of which provides a bipolar interrogate current pulse to a row of ferrods. The drivers for the matrix horizontals are contained on the matrix circuit packs themselves, while a separate block of interrogate drivers is used for the verticals. The control and timing section provides signals to the selected drivers at the proper times. The responses from the interrogated ferrods are received by the detectors and returned to the FIOC.

CONTROL AND TIMING - FS 17

4.02 The scan-control circuit pack receives address information and an order code from the FIOC. The address is decoded into a 1-out-of-16 horizontal selection and a 1-out-of-8 vertical selection. The FIOC also activates one of two enable leads. Which of the two leads is activated depends on which half of the scanner is to be accessed. Upon receipt of an enable, the control pack causes the timing pack to initiate the sequence shown in Information Note 314. The timing pack signals the interrogate drivers to select a negative and then a positive vertical in succession and then signals the FIOC to accept response pulses from the detectors. The leading edges of the LCT and RDGCT pulses define a window during which the response will be accepted by the FIOC for transmission to the CC.

INTERROGATE MATRIX - FS 18

4.03 The interogate matrix consists of a 16-by-16 array of transformers built up from 16 circuit packs, each containing a 4-by-4 array. The first four circuit packs also provide the horizontal drivers for the entire matrix and an indication to the interrogate drivers as to how many horizontals have been selected. A particular transformer is selected by activating a horizontal driver to supply +24 volts to the selected horizontal. The two vertical drivers associated with the desired transformer are then activated in sequence, thus supplying ground first to one and then to the other of the two oppositely poled primary windings and consequently generating a negative output pulse followed by a positive output pulse.

INTERROGATE DRIVERS - FS 19

4.04 The interrogate drivers provide the ground for the matrix verticals for selection and pulse timing. Each circuit pack receives four outputs from the

vertical decoder and two signals from the timing circuit pack. These are logically combined to generate four positive vertical outputs and four negative vertical outputs. The eight vertical decoder outputs multiple to two pairs of driver packs with the final selection being determined by one of two pairs of timing signals. Which pair of timing signals is used depends on which half of the scanner is being accessed.

4.05 The four interrogate driver packs are interconnected both with each other and with the first four matrix packs in order to provide 1-out-of-N checks, which are passed back to the scanner control pack. Only the checking circuits on the first driver pack are used.

DETECTORS - FS 20

4.06 The scanner detectors receive the readout current from columns of ferrods and return a logic-level signal to the FIOC. Each circuit pack receives the readout signals from the 16 columns of one logical scanner and returns 16 bits to the FIOC. The outputs from the first four detector packs are multipled to one FIOC port while the last four packs feed the other FIOC port. Of the 16 bits in each group, four (bits 2 through 5) do not go directly to the FIOC but are routed instead through the scanner control pack and then to the FIOC. On certain orders (see Information Note 315), these bits are replaced by other status information from the control pack.

4.07 Each detector pack also has a connection from the scanner test board. The test board can inject a current into the 16 readout loops of each detector pack to verify the continuity of the readout loop. This should result in a logical zero on all 16 outputs of the detector pack under test.

5. +3 VOLT AND +24 VOLT POWER DISTRIBUTION - FS 21

5.01 The +3 volt and +24 volt power for the PCC, along with the associated ground, are distributed through multilayer printed-wire backplanes (MLPWBs). The MLPWBs that provide +3 volts and +24 volts to the NC, SC, and PPD are split into an upper- and lower-half plane so that each voltage is present at the COAX terminating field in each circuit pack position. The MLPWB that carries the +3 volts to the ceramic packs is fed by the two +3 volt power converters with each converter powering half of the circuit pack positions.

+3 VOLT POWER CONVERTERS

5.02 The +3 volt power for the unit is supplied by two dc-to-dc converters operating from -48 volts with +24 volt control circuitry. A reference voltage is provided by the +12 volt reference board and is reduced to +3 volts by a voltage divider on the +3 volt reference and filter board. The power converters are turned on and off by the presence or absence of +24 volts on the +24VST leads, which are under control of the frame circuit. Other leads to the frame circuit provide power alarms and alarm test capability.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Switchboard cable for leads (0 through 7) SC(A/B) (0 through 15) and leads SDR (00 through 07) (00 through 31) (P/N) may not exceed 25 feet.

1.02 Switchboard cable for leads D(P/N) (000 through 255) may not exceed 450 feet.

1.03 Leads which connect to the mate PCC may not exceed 3 feet and must be wired as specified in the control frame circuit (SD-3H902-01).

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packs

Designation	Meaning
CGD	NC Concentrator Group Decoder
CLR	NC Control Logic and Register
CTL	PPD Control
GC	NC Guard Control
GKD	NC Group Check Detectors
HD(0/1)	PPD Horizontal Driver
HDS(L/H)	NC High and Dry Select (Low/High)
IGGS(A/B/C)	NC Input Gate Group Select
IGS(L/H)	NC Input Group Selector (Low/High)
ILM	NC Input Level and MISC Decoder
INS	NC Input Node Select
LCB	PPD Level Control Board
LVD	NC Level Decoder
MP(00-15)	PPD Matrix Pack
OGGS(A/B)	NC Output Gate Group Select
OGS	NC Output Group Select
ONSA	NC Output Node Select
PDLC	NC PWR & Dummy Load Control
PEN	NC Power Enable Control
RCVX	FIOC Receiver-Transmitter
REGHIGH	FIOC Shift Register (high half)
REGLOW	FIOC Shift Register (low half)
RL2HD	NC Release 2 and High and Dry Decoder
SCDET(0-7)	SC Detectors
SCNCTL	SC Control
SCNTMR	SC Timer
SCNTST	SC Test
SEQCTL	FIOC Sequence Control
SICD(0-3)	SC Interrogate Current Driver
SWD	NC Switch Decoder
S3GS	NC Stage 3 Group Select
TCPK	NC Timing Control

Designation	Meaning
VD(0-2)	PPD Vertical Drivers
VXLTR	PPD Vertical Translator
12REF	+12 V Reference
16VS	NC 16-V Source
3CON(0/1)	+3 V Power Converter
3REF	+3 V Reference and Filter

3. FUNCTIONS

3.01 Provides means to communicate with the CC via four 6.67-MHz serial subchannels.

3.02 Provides means to generate low-speed serial messages on any of 256 outputs suitable for the operation of peripheral decoders on peripheral frames.

3.03 Provides means to work with the electronic remreed pulser circuit to control the crosspoints of the network fabric on up to eight network frames and the associated third-stage switches.

3.04 Provides means to read out the states of up to eight blocks of 512 ferrods in peripheral circuits and return this data to the CC.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) 3A Central Control Circuit - SD-1C900-01.

(b) Electronic Remreed Pulser Circuit - SD-1C913-01.

(c) 15A Remreed Grid Circuit - SD-3H120-01.

(d) 15B Remreed Grid Circuit - SD-3H121-01.

(e) First and Second Stage Access Circuit - SD-3H122-01.

(f) 15C Remreed Grid Circuit - SD-3H130-01.

(g) Third Stage Access Circuit - SD-3H131-01.

(h) Master Scanner Matrix Circuit - SD-3H140-01.

(i) Distribute Point Circuit - SD-3H150-01.

(j) Junctor and Junctor Control Circuit - SD-3H200-01.

(k) Peripheral Test Circuit - SD-3H520-01.

(l) Network Frame Circuit - SD-3H901-01.

(m) Control Frame Circuit - SD-3H902-01.

(n) Scanner, Peripheral Pulse Distributor, and Peripheral Decoder Assignment Rules - SD-3H912-01.

5. MANUFACTURING TESTING REQUIREMENTS

Intermediate Requirements

5.01 None.

End Requirements

5.02 This circuit should be tested to verify that it is wired in accordance with the schematic and wiring drawings, that the requirements of the circuit requirements table are met, and that the circuit is capable of performing all functions stated in this circuit description.

5.03 Functional tests for this circuit are performed as part of the test of the Control Frame Circuit - SD-3H902-01 and are specified in the X-79037 specification.

6. TAKING EQUIPMENT OUT OF SERVICE

6.01 This circuit may be taken out of service by pressing the associated REQ key on the control frame control panel. If the unit is already out of service, pressing the REQ key will cause diagnostics to be run on the unit. If the diagnostic passes, the unit is restored to service. The NC, SC, or PPD may be individually removed from or restored to service by means of appropriate TTY messages.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 Provided complete CD information.

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