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ELECTRONIC SWITCHING SYSTEMS

NO. 3

MULTIFREQUENCY RECIVER
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This circuit receives voice-frequency signals in the multifrequency (MF) code, recognizes the frequencies present, and informs the processor of these frequencies via scan points. These signals are the directory number of a customer to which a distant office is calling. In addition, this circuit checks the continuity of loop trunks and transmits a battery-reversal start-pulsing signal (wink) to the MF transmitter of the distance office. This circuit also provides a high degree of protection against false operation by voice-frequency components contained in speech or noise picked up by an operator transmitter and/or coupled into the transmission facility as crosstalk.

2. GENERAL DESCRIPTION OF OPERATION

2.01 When a call is from a distant office, the local office must be sent the called number so that it can complete the call. An MF receiver is the circuit that receives the called number in the form of tone signals from the distant office. After the calling customer has dialed the called number and the distant office has determined that the call is to another office, an idle MF transmitter will be seized and connected to the appropriate trunk circuit. The trunk circuit will then send a seizure (start) signal to the local office. The local office will connect an idle MF receiver to the trunk circuit via a network path through a bypassed junctor. To verify the connection, the processor will scan the continuity scan point of the MF receiver. When the MF receiver is ready to receive digits, the MF receiver sends a wink (reverse battery) signal to the distant MF transmitter. The MF transmitter will detect the wink signal and the distant office will cause the MF transmitter to start sending the digits in the form of tone signals conforming to the 2-out-of-6 code. The MF receiver will detect and decode the signals into the frequency components.

2.02 Several timers are used to verify that the signals detected are true digits. When the signal input exceeds a minimum value, a timer is started. Once the MF

receiver decodes the signal into at least two frequency components, a second timer is started. When both timers time out, the signal-present scan point is operated. The processor will then scan the frequency scan points to determine the digit sent and check that only two of the six frequencies are present. If the signal input does not exceed the minimum valve or goes away before the timer times out, the timer will be reset and no signal-present indication is given. If only one frequency is present, the second timer will not be started and no signal-present indication will be given when the first timer times out. To prevent double registration of a digit, a third timer is started when the signal input is removed. The third timer will hold the signal-present scan point operated for a period of time to prevent noise from causing a second signal-present indication to be given on the same digit. After all digits have been received, the processor idles the MF receiver and releases it.

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.01 MF signaling uses one group of six frequencies in the speech band (700, 900, 1100, 1300, 1500, and 1700 Hz). A valid MF signal consists of exactly two of these six frequencies. This signaling code is known as the 2-out-of-6 code. There are only 15 valid combinations, which can be used as digits or other signals.

1.02 When a call is from a distant office, the distant office will locate and connect an idle MF transmitter to the appropriate trunk circuit. This connection will then cause the trunk circuit to send a seizure (start) signal to the local office.

1.03 The local office will locate and connect an idle MF-receiver circuit to the trunk circuit via a network path through a bypassed junctor. The MF receiver will send a start-pulsing signal (wink) to the MF transmitter when it is connected to the trunk. When the MF transmitter detects the wink signal, the distant office will operate the MF-transmitter tone-select relays and begin sending the digits.

1.04 The MF receiver will receive the signals from the distant office and decode the individual frequencies. The receiver will time the input signal and the frequency combinations to verify that a digit has been received (not noise or speech). When the input signal persists for a minimum time, with at least two frequency components, the signal-present scan point is operated. The operation of the signal-present scan point will cause the processor to scan the frequency scan points. The processor then determines that two out of the six frequencies (2-out-of-6

code) are present and that the frequency combination is a valid combination. If either test fails, the processor aborts the call. To prevent double registration of a digit (noise interference), another timer is started when the input signal is removed. This timer will hold the signal-present scan point operated for a period of time to prevent causing the processor to rescan the frequency scan points for the same digit. The processor will monitor the signal-present scan point for each successive operate and release (to initiate a frequency scan) until all digits are received.

2. SIGNALING CODE

2.01 The relationship between digits and other signals and the MF-signaling frequencies in the 2-out-of-6 signaling code is shown in Table A.

TABLE A

MF 2-OUT-OF-6 CODE

FREQUENCY HERTZ	SIGNIFICANCE
700, 900	1
700, 1100	2/CC
700, 1300	4
700, 1500	7
700, 1700	R/ST3P
900, 1100	3
900, 1300	5
900, 1500	8
900, 1700	STP
1100, 1300	6
1100, 1500	9
1100, 1700	KP/CR
1300, 1500	0
1300, 1700	ST2P
1500, 1700	ST

Note: CC = Coin Collect

CR = Coin Return

R = Rering or Ringback

KP = Keypulse

ST = Start [=1 + Coin for TSP(s)], [normal trunk start]

STP = Start [=0 + Coin for TSP(s)]

STP = Start [=1 + Noncoin for TSP(s)]

STP = Start [=0 + Noncoin for TSP(s)]

3. CONTROL OF CIRCUIT

3.01 The MF receiver has one state relay (A), which is controlled by the distributor circuit. The processor determines the state required and, via the peripheral decoder circuit, operates the relay.

3.02 Relay A, driven by -48 V, has a 1000-ohm resistor, with one of the break contacts in parallel with it, in series with the coil to initially provide rapid operate. This arrangement also limits the maximum current through the distribute point when the relay is operated. To limit the transient voltage spike when the relay is released and to dissipate the relay-coil energy when released, a diode is connected from the distribute point to -48 V with the anode of the diode to -48 V.

3.03 A representation of the MF-receiver states is:

$$\bar{A} \qquad A$$

$$00 \qquad 01$$

Wink   Digits

3.04 When the MF receiver is in the idle or wink state, the A relay is released and -48 V and ground are connected to the tip and ring respectively (reverse battery). Operating the A relay connects -48 V and ground to the ring and tip respectively.

3.05 This is a typical state sequence of this circuit. See BSP 233-151-105 for more details.

Operation	State Sequence
Receive Digits	000, Send Wink
	001, Receive Digits
	000, Idle

4. CIRCUIT OPERATION

4.01 An MF-receiver circuit is comprised of 11 circuit packs, input transmission circuitry, and a voltage-divider power supply (R1 through R5). Because all operating potentials are proportional to the battery voltage, all potential changes are as well. Thus, overall battery variations have little effect on receiver performance. Filter capacitors (C1 through C6 on circuit pack A1024) smooth the output voltage of the voltage divider. The power-off (PWR OFF) key removes battery from the circuit to permit circuit pack removal and testing. A resistor (R3 on circuit pack A1024) limits the current in the PWR OFF indicator lamp. The remainder of the circuit components will be discussed in the order in which the signal passes through them.

4.02 The input transmission components are L, T, C5, C6, C7, and C8. Inductor L connects the continuity scan point (SC0), which supplies battery and ground, to the network via the tip-ring reversing contacts of relay A. Transformer T has a very lower capacitance between the primary and secondary windings, which provides a high degree of protection from longitudinal lightning surges to the circuit. Capacitors C5, C6, C7, and C8 provide protection against metallic surges. C5 and C6 also provide dc blocking in the transformer primary. The input transmission circuitry, when terminated into the variolosser circuit (P/O circuit pack A260), presents a very high return loss to the network.

4.03 The variolosser circuit (P/O circuit pack A260) provides a controlled loss to the input signal and passes the signal to the AGC amplifier (P/O circuit pack A261). A dc control current from the AGC will change the shunt impedance (and thus the gain) of the variolosser circuit. This feedback control assures an almost constant steady-state ac signal at the variolosser output.

4.04 Any feedback loop requires a finite time to respond (and correct for) changes in the input level. This time is called the attack time of the AGC system. The attack time of the receiver is approximately 5 ms. If a high-level signal is received, the variolosser will pass an excessively-high input signal to the AGC amplifier until the feedback loop can reduce the variolosser gain.

4.05 After the receiver sends the wink signal (reverse battery), relay A is operated to place the circuit in the receive-digits state. Operating relay A connects ground and battery to tip and ring respectively, and also creates high-level voice-frequency transients, which appear as an input to the receiver. These transients could cause the variolosser circuit to be placed in a high-loss condition until the AGC system responds. This high-loss condition could persist long enough to prevent detection of the low-level keypulse (KP) signal from the distant office. To prevent this problem an inhibit amplifier (P/O circuit pack A262) stops the feedback control from operating for approximately 20 ms after relay A operates. The 20-ms delay is sufficient to allow for the battery-reversal transients to die out and no longer affect the operation of the receiver.

4.06 The AGC amplifier amplifies the signal from the variolosser and supplies the amplified signal to the signal driver (P/O circuit pack A261), the guard driver (P/O circuit pack A260), and the control rectifier of the variolosser, which generates the direct current to control the variolosser gain.

4.07 The guard driver provides a frequency-dependant dc bias to the MF-channel detectors (A152s) to prevent digit simulation (see 5.01 through 5.04). The guard filters (P/O circuit packs A262 and A263) short signaling frequencies out of the guard-driver input. All other voice frequencies are amplified and rectified to provide the dc guard bias.

4.08 The signal driver provides power gain to the signal so that the channel filters (circuit packs A264 and A265) can respond. These six filters are a parallel combination of series-resonant circuits. This configuration offers low impedance at signaling frequencies and requires that the signal driver provide high (ac) current.

4.09 The channel filters separate the signal into the frequency components, corresponding to the MF-signaling code, and apply the individual frequencies to the MF-channel detectors. The channel detectors (dc) will convert the frequencies applied to a direct current only if the guard bias does not exist. A direct current would operate the frequency scan points (SC2 through SC7). When two channel detectors operate, a valid signal is present.

4.10 The signal-present timer (circuit pack A266) is two separate timers ANDed together. The first timer is activated by the ac signal from the signal driver. If the input persists continuously for 20 ms, the timer will time out and activate one side of the AND gate. The second timer will be activated when at least two channel-detector outputs are operated. If the channel-detector outputs are operated continuously for 10 ms, the timer will time out and activate the other side of the AND gate. If the input to either timer is removed before the timer times out, the timer will be reset. When both inputs to the AND gate are activated, the AND gate will operate the scanner driver (P/O circuit pack A1024), which will operate the signal-present scan point (SC1). The operating of the signal-present scan point (SC1) will cause the processor to scan the frequency scan points (SC2 through SC7) and interpret the digit received. To prevent double registration of the same digit, bridge timing is used. When the input to the timers is removed after time-out, the timers will time for 20 ms before releasing the AND gate. The 20-ms delay will prevent noise from causing the signal-present scan

point to release and reoperate for the same digit.

5. PROTECTION AGAINST DIGIT SIMULATION BY GUARD ACTION AND SIGNAL-PRESENT TIMING

5.01 The MF receiver uses guard action to reduce digit simulation or the response of the receiver to signals that are not genuine MF pulses. The guard driver applies a dc bias to the channel detectors that varies in magnitude according to the frequency and amplitude of the received signal. With guard action, genuine MF pulses excite the guard driver only weakly and strongly excite the proper channel detectors. Thus, the receiver is able to respond. In contrast, most speech signals contain many frequency components that excite the guard driver more strongly than the channel detectors. Guard bias is generated to inhibit the response of the channel detectors and the receiver tends not to respond to signaling frequencies in the presence of other signals.

5.02 The AGC amplifier applies a signal to the guard driver. The MF guard filter effectively shorts the signaling frequencies out of the guard driver. Any voice-frequency signal not shorted out will be amplified and rectified to produce a dc-bias voltage. Since the MF-signaling frequencies are shorted out, the dc bias will only appear as a result of the presence of nonsignaling frequencies. This bias raises the threshold of the channel detectors and inhibits the recognition of signaling frequencies. Consequently, if a signal is to be recognized, frequencies in the 2-out-of-6 code must be present and other signals must be either absent or at a much lower level.

5.03 Because some digit simulating signals may contain momentary bursts of only signal frequencies, guard action as described may not be sufficent. However, in speech, pure digit-simulating frequencies are of very brief duration. By requiring at least two channel-detector outputs to remain active for 10 ms before digit recognition is possible, most speech-generated potential simulations will come and go without being recognized.

5.04 Another longer timing is provided for ac-signal levels approximately equal to or greater than the minimum expected MF signals. Lower levels cannot activate the timer at all. This timer requires that an ac signal be present for 20 ms before a digit can be recognized. Thus, guard action and two separate timing operations prevent digit simulations by voice-frequency energy.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The maximum external loop resistance is 6000 ohms. The minimum insulation resistance is 30,000 ohms. The battery limits are -42.75 V to -52.50 V.

2. FUNCTIONAL DESIGNATIONS

2.01 Associated Scanner Ferrods

Designation	Meaning
SC0	Continuity
SC1	Signal Present
SC2	700 Hz
SC3	900 Hz
SC4	1100 Hz
SC5	1300 Hz
SC6	1500 Hz
SC7	1700 Hz

2.02 Circuit Packs

Designation	Meaning
Chan Filter	Channel Filter
MF	Multifrequency
MF Chan Det	MF Channel Detector
MF Gd Dr	MF Guard Driver
MF Sig Dr	MF Signal Driver
MF Sp Timer	MF Signal Present Timer
MF VLSR	MF Variolosser

2.03 Circuit States

Designation	Meaning
Wink	Circuit Idle (Battery and Ground on tip and ring respectively).
Digits	Circuit ready to receive digits.

3. FUNCTIONS

3.01 Provides for reception of multifrequency signals from operator keysets or automatic sending equipment and converts the received signals into outputs suitable for detection by the scanner.

3.02 Provides proper response to MF pulses of 30-ms duration with 30-ms intervals between pulses.

3.03 Provides response to MF pulses with received level within the limits of -22 dBm and -2 dBm per tone. The receiver is able to respond properly in the presence of 6.0-dB twist (difference) between any two MF tones.

3.04 Provides dc output signals of at least 11 ms for each of the signaling frequencies, regardless of input-signal duration, when a valid signal is received.

3.05 Provides a signal-present output signal, which starts about 20 ms after a valid input signal is received and remains operated until about 20-ms after the input signal is terminated.

3.06 Provides tolerance for variation in the received signaling frequencies of ±1.5 percent ±10 Hz about the nominal MF-signaling frequencies.

3.07 Provides protection against false operation on speech or noise by:

(a) Guard action.

(b) Fast-acting detectors.

(c) A signal-validity check requiring the operation of two (or more) detectors for a timed interval before the signal-present output is delivered.

(d) A fast-cycling timer, which forces an input signal above a threshold level to persist uninterrupted for a required time interval before the signal-present output is delivered.

(e) Signal-present output holding to prevent recycling when noise causes short breakups in the input signals.

3.08 Provides means to prevent a reverse-battery start-pulsing transient from affecting the AGC feedback loop; the feedback loop is inhibited for a timed interval after operation of the A relay.

3.09 Provides for sending a wink (start-pulsing signal) to the distant office.

3.10 Provides a high return loss to the transmission facility.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) Master Scanner Circuit - SD-3H140-01.

(b) Distribute Point Circuit - SD-3H150-01.

(c) Universal Trunk Circuit - SD-3H220-01.

5. MANUFACTURING TESTING REQUIREMENTS

Intermediate Requirements

5.01 Before circuit packs are inserted in the unit, it should be verified that the unit is wired in accordance with the schematic and wiring drawings to prevent damage to the circuit packs.

End Requirements

5.02 This circuit should be tested to verify that it is wired in accordance with the schematic and wiring drawings, that requirements of the circuit requirements table are met, and that the circuit is capable of performing all functions stated in this circuit description.

6. ALARM INFORMATION

6.01 This circuit is fused individually with one fuse to the -48 V talk supply. If the fuse blows, it will cause an FA relay, in the frame that it is mounted on, to operate as alarm.

7. TAKING EQUIPMENT OUT OF SERVICE

7.01 Information on taking this circuit out of service can be found in BSP IM-3H000 and OM-3H000.

SECTION IV - REASONS FOR REISSUE

D. DESCRIPTION OF CHANGES

D.1 Provided complete CD information.

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