COMMON SYSTEMS
3B20D MODEL 2 & 3 PROCESSOR
SMALL COMPUTER SYSTEMS INTERFACE (SCSI)
NEW SHIP UNIT
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Main Store (MAS), IO, and Disk File Controller (DFC) circuits provide program and data storage for the 3B20D processor, mass storage for the 3B20D processor (in the main store subunit), basic input/output capability between the 3B20D processor and IO devices (in the IO subunit), and firmware control of a fixed media disk system (in the DFC subunit).

2. GENERAL DESCRIPTION OF OPERATION

MAIN STORE

2.01 The main store is physically partitioned into two units: a main unit (J3T029AA-1) and a growth unit (J1C147BC-1). The main unit contains the main store controller (MASC) and up to eight MAin Store memory Arrays (MASAs). The growth unit is connected to the main unit via a tape cable assembly and can consist of up to eight additional MASAs. The 3B20D main store growth increment is on a per MASA basis, in other words, each additional MASA increases the addressable memory by 1, 2, or 4 megabytes. The maximum address spectrum of the 3B20D is 16 megabytes without memory expansion, and 64 megabytes with the Very Large Main Memory (VLMM) feature.

A. Interface

2.02 The MASC interfaces to the MASAs and, via the MAin Store Update (MASU), to the Central Control (CC), Direct Memory Access Controller (DMAC), and the other processor. Communication between the two control units is through the MASU in each CU. The MASU controls all access to the MAS and, in the case of multiple store requests, determines which unit has the highest priority and allows access from that unit to the main store busses.

B. Features

2.03 The MASC contains the Hamming circuitry, data and address parity check circuits, a timing sequencer for system or refresh store cycles, the array addressing circuitry, and maintenance access circuitry.

2.04 Since the memory used in the 3B20D main store is dynamic, the stored information must be refreshed periodically. The main store controller determines the time and rate at which refresh operations occur. When possible, the controller makes the refresh operation transparent to the system by inserting it at the end of a system access.

2.05 The 3B20D main store performs error checking and correction. Hamming circuitry in the main store controller and Hamming coding of data in the memory arrays result in the correction of all single-bit errors; this circuitry also flags all double and detectable multi-bit errors. The state of the memory is continually checked during refresh cycles. Each refresh cycle selects a particular memory array, reads the data at the current refresh address, and checks this data for data parity errors. The memory arrays that were not selected are refreshed only. The entire memory is thus verified for good data every 134 seconds. In addition to the Hamming correction and refresh/data parity checking, the store performs various hardware checks on internal circuitry and bus communications. If the check circuit detects an error, the MAS returns four error signals to the system. Based on the type of error, the CC can attempt to remedy the error, or mask the error and continue to run. Additional data on the error source is retained in three registers in the store. These registers contain information as to which of the four error sources is applicable when the error occurred (refresh or system access), and the address that was being accessed at the time of the error.

C. Store Access

2.06 A store access is initiated when the STORE GO signal (SGOO) is received. Upon receiving this signal, the main store controller begins a timing sequence which accesses memory or performs the required maintenance operation. The command leads indicate whether the operation is a WRITE, READ, CLEAR, BYTE, HALFWORD, or MAINTENANCE operation. The store signals the CC that the store no longer requires the address, command, and data buses with the STORE COMPLETE (SCMOO) signal. This signal is issued by a timing sequencer in the main store controller to the MASU. The trailing edge of the SCMOO signal from the main store on read operations indicates to the CC that the data on the store data bus is valid.

INPUT/OUTPUT (IO)

A. Physical Description

2.07 The input/output subunit consists of four circuit pack slots. Two of these slots accept the single-board Direct Memory Access Controller (DMAC) (UN46), while the other two slots accept the Dual Serial CHannel (DSCH) circuit pack (UN9B). A minimum equipage would be one UN46 and one UN9B.

B. Interface

2.08 The DMAC interfaces with the central control unit via the Central Control Input/Output (CCIO) bus. In addition, each UN46 can interface with a maximum of two DSCH boards via the Direct memory access Input/Output (DIO) bus. Each DSCH can interface with a maximum of 16 devices through five pairs of dedicated wires. These wires connect between the DSCH and each device. The dual serial channel can also communicate directly with the central control via the CCIO bus. Each central control unit can interface with a maximum of two DMACs over the CCIO bus. The DMA also interfaces to the main store over the main store bus.

C. Features

2.09 The purpose of the direct memory access system is to transfer data to or from a peripheral device using its own data transfer control circuitry. This transfer can be a word transfer (32 bits and 4 parity bits) or a block transfer (16 words). Each device is set up by the CC in one of two modes: expanded or unexpanded. Unexpanded devices have access up to 128k bytes of main store memory; expanded devices can have up to 256 jobs, each of which has access to 128k bytes of memory.

2.10 The DSCH performs word and block data transfers between the DMA and the devices. The DSCH can also perform interprocessor communication operations (CHIP mode). Data communication to and from devices occurs over two pairs of data leads. The low order bits (0-15) are transmitted serially over the data low lead, and the high order bits (16-31) are transmitted over the data high lead.

SCSI DISK FILE CONTROLLER (DFC)

2.11 The SCSI-DFC interfaces to the 3B20D processor via the DMAC/DSCH. Each DFC supports two independent differential SCSI busses. Each SCSI bus can logically support seven disk drives. The 3B20D SCSI disk driver software supports a maximum of four disk drives per bus.

2.12 The 3B20D SCSI-DFC consists of a Duplex Dual Serial Bus Selector, or DDSBS (TN69B), which interfaces to the DSCH, a SCSI Host Adapter (UN294 and TN2116), a power supply (495FA), and a power switch (TN6B). The Host Adapter (HA) provides an interface to the DDSBS, an interface to two SCSI busses, and intelligent control logic.

2.13 The DDSBS communicates with the 3B20D via the dual serial bit stream of the DSCH. The DDSBS converts the serial data and commands from the DSCH to 36-bit parallel words. The DDSBS also communicates to the 3B20D processor through a service request line used to transmit setup, transfer, and interrupt requests to the 3B20D DMAC. The DDSBS communicates with the UN294 through a 36-bit bus for data, commands, status, and ten control and response signals used for handshaking during transfers.

2.14 The Bus Interface Circuit (BIC) on the UN294 provides the interface between the HA and the DDSBS. The BIC contains the registers and first-in-first-out memories (FIFOs) used to buffer commands, status, and data between the 3B20D and the HA.

2.15 The UN294 also contains the SCSI bus interface circuitry. Each SCSI bus is controlled by a SCSI Protocol Controller (SPC), which provides much of the low-level control of the SCSI bus protocol. Each differential SCSI bus consists of 50 signals that are brought out to the UN294 backplane. The disk drives on each bus connect to the backplane through a 50-conductor twisted-pair ribbon cable. SCSI bus termination is provided by resistor networks that plug into each end of the SCSI cable.

2.16 The HA control logic on the TN2116 provides the intelligent control necessary to process commands from the 3B20D and manage the two SCSI busses. It contains a CPU, a DMA controller which performs high-speed data transfers between the SCSI busses and HA RAM or BIC FIFOs, 256 kbytes of EPROM, 1 Mbyte of RAM, address decoding logic, interrupt control logic, and a serial port for debugging support.

2.17 The 495FA power unit supplies +5 volt power to each of the circuit packs within the DFC.

2.18 The TN6B power switch directs the sequencing of power within the DFC, and is controlled by the operator from pushbutton switches mounted at the faceplate of the pack. During power up/power down sequencing, the power switch provides an initialization signal that initializes the TN69B, UN294, and TN2116. In addition, the power switch automatically removes all power when +5 volt power is absent or when any fuse is blown.

SECTION II - DETAILED DESCRIPTION

1.01 More detailed circuit descriptions can be found in the individual circuit pack schematics.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 NOMINAL LIMITS
+5-volt power +5.00 volts $\pm$ 10 percent

2. CONNECTING CIRCUITS

2.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) Power Distribution Circuit SD-4C053-01.

(b) 3B20D Model 3 Processor System Circuit SD-4C122-02.

(c) Moving Head Disk Drive Interface KS-23484, list 11B and list 13.

(d) Circuit Packs and Power Converters per SD-3T004-01.

3. MANUFACTURING TESTING REQUIREMENTS

3.01 The manufacturing testing requirements are specified in the X-79516 3B20D Models 1, 2, and 3 test specification.

4. TAKING EQUIPMENT OUT OF SERVICE

4.01 This information is contained in the task-oriented practice for 3B20D Models 2 and 3 BSP 254-302-811.

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