COMMON SYSTEMS
3B21D COMPUTER
PROCESSOR CIRCUIT
UNIT

CONTENTS

1. GENERAL DESCRIPTION 1
1.1 PURPOSE OF CIRCUIT 1

2. GENERAL DESCRIPTION OF OPERATION 1
2.1 CONTROL UNIT 1
2.2 INPUT OUTPUT PROCESSOR 3
2.3 DISK FILE CONTROLLER 6
2.4 SCSI TERMINAL FIELDS (B.37 - B.38) 7
2.5 BUS TERMINATIONS 7

3. DETAILED DESCRIPTION 8

4. REFERENCE DATA 8
4.1 WORKING LIMITS 8

5. REASONS FOR REISSUE 2 8
5.1 Incorporate external wires into backplane 8
5.2 Ground Changes 8
5.3 Functional Changes 8

6. REASONS FOR REISSUE 3B 9
6.1 Functional Changes 9

7. ACRONYMS 9

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The basic unit contains all of the functionality required to support one of the two processing units that comprise a duplex 3B21D. The major units in the basic unit consist of: the control unit (CU), input/output processor (IOP), disk file controller (DFC), (small computer system interface [SCSI], peripheral units [SPUs]) and the port switch signal distribution (PSSD).

2. GENERAL DESCRIPTION OF OPERATION

2.1 CONTROL UNIT

2.1.1 CONTROL UNIT POWER (B.1-B.2)

Power control for the CU power group is provided by a TN1821 or TN1821B CU power switch (CUPS). This circuit pack controls two 410AA DC-to-DC power converters: power converter A (CONVA), and power converter B (CONVB). Converter A powers the major CU circuit packs and is always required. Converter B powers the two expansion slots (EX0 and EX1), and a second direct memory access (DMA) position. It is not required unless any of these three positions are equipped. The TN1821B supports Auto Restart, while the TN1821 does not. The Auto Restart function allows a power controller to restart automatically if -48 volt power has been removed and then reapplied and if the power controller's power switch is ON. This function is useful for an automatic restart of the hardware after a power outage.

Both 410AA power converters have separate -48 volt inputs and provide separate +5 volt outputs: P5VA and P5VB. Signals CCSTP and CCSTN are connected to relay contacts within the TN1821 that close to start the 410AAs. The TN1821 and TN1821B provide two power-on-reset outputs: CPWRCLR0 and MSTART0. These two signals are normally high, but go low momentarily when the power switch is started. CCALM0 and CBALM0 are low voltage alarm signals from the 410AAs. The TN1821 and TN1821B will handle these alarms differently. In the TN1821, both signals are tied together within the circuit pack. An alarm from either signal will cause the TN1821 to turn off both 410AA power converters. The TN1821B will turn off the power to both converters and indicate a power and major alarm when CCALM0 is active. When CBALM0 is active, the TN1821B only indicates the alarms.

CINTA0 and CINTB0 are part of the primary CU power interlock. When circuit packs are installed in the KLW32, KLW31, and KBN15 (DMA0) positions, the primary interlock circuit is closed, and CONVA will operate. CINTC0 is part of the secondary interlock, and is connected to the EX0, EX1, and DMA1 positions. The secondary interlock will indicate an alarm if CONVB is not installed and if there is a circuit pack in any of the EX0, EX1, or DMA1 slots.

The CUPS circuit packs have two alarm outputs. Signals MJ and MJR comprise the major alarm. Signals PA and PAR comprise the power alarm. Both signal pairs are connected to relay contacts within the TN1821 and TN1821B. Failure of an interlock, a low voltage alarm, or a loss of -48 volt power to the TN1821/TN1821B will cause its major alarm relay, MJ and MJR, to close. The power alarm relay, PA and PAR, will close under the same conditions, except that it requires that -48 volts be present at the TN1821. The major and power alarm outputs are connected in parallel with the alarm outputs on the other power switch circuit packs.

CPAN and CPAP connect programming resistors in the KLW31, KLW32, TN1820, UN379, and KBN15 (DMA0) to the overcurrent protection circuit in CONVA. CPBP and CPBN are the equivalent signals from the two expansion circuit slots and the second DMA controller to power converter CONVB. The status of the power switch is encoded in the two CSCXP and CSCYP scan outputs. CSCZP indicates the state of the input FALM1, which is used for a fuse alarm. CRQIPP and OOSP are inputs used to operate faceplate light emitting diode (LED) indicators on the TN1821.

The TN1821 boundary scan interface is not used at this time.

2.1.2 CENTRAL CONTROL (B.3)

The processor or central control (CC) circuit pack is the KLW31. It contains the main 3B21D central processing unit (CPU). It obtains instructions or data from the KLW32 main memory circuit pack and translates this information into a sequence of actions within itself or associated circuitry. There are four major backplane interfaces to the CC circuit pack. The first is the main memory bus to the KLW32 memory pack. This has a 36 bit wide data path (32 bits of data and four bits of parity), and an address width of 32 bits (28 for address and four of parity). Although the KLW32 pack supports up to 128 megabytes of memory, the address capability in the basic unit allows an address capability of 256 megabytes. There is also a 36 bit wide central control input output (CCIO) bus between the CC pack and the two DMA controller positions. This is used to communicate directly with the DMA channels. Third, there is a serial boundary scan bus from the KLW31 that has access directly or indirectly to all circuit pack positions in the 3B21D, except for the power converter slots. Finally, there is an interface to the UN379 utility circuit. There are three cabled interfaces on the KLW31. Direct control of the processor is provided by two emergency action interface (EAI) ports that are cross connected from the CC pack to the TN983 controllers in both IOPs of a duplex 3B21D. A second cable interface is the maintenance channel link, which allows processor-to-processor communications between CU0 and CU1. The last cable interface is a differential boundary scan bus port that is connected to the TN1820 IOP power switch in the IOP located in the other basic unit of a duplex 3B21D. This allows the CC is access boundary scan circuitry in the other backplane.

The CCID0 input determines whether the processor is part of CU0 or CU1. In CU1, this input is tied to ground.

There are eleven KLW31 interrupt inputs (SIS030 through SIS150) that are brought out to backplane pins. These are intended for connections to interrupt sources. Each KBN15 position has two interrupt outputs. Each expansion slot position has one interrupt output. All six outputs are routed in the backplane to a terminal field at equipment location (EQL) 13-037 that is adjacent to the KLW31 circuit pack position. The KLW31 will not recognize an interrupt output unless it is wired to one of its interrupt inputs. One wiring connection is mandatory. The basic 3B21D functions require that the KLW31 SIS100 input be connected to DMA0's D0INT00 output. All other connections are ordered as wiring options.

2.1.3 UTILITY CIRCUIT (B.4)

The UN379 utility circuit (UC) is an optional circuit pack. It is used to support special purpose software for monitoring or developing code.

2.1.4 MAIN MEMORY (B.5)

This position accepts the main memory circuit pack. There are five possible circuit packs that may be installed. These are the KLW32, KLW40, KLW48, KLW64, and KLW128, each containing 32, 40, 48, 64 and 128 megabytes, respectively of usable semiconductor memory. The various main memory circuit packs are all based on the KLW32 circuit pack, which has three open socket positions. Memory modules can be plugged into these sockets in various combinations to grow the memory capacity. The memory is used to provide storage of data and programs in the 3B21D.

The main memory supports six circuit pack positions. Five of these are in the same backplane. These are the KLW31 processor, the two KBN15 DMA controllers, and the two expansion slot positions. The sixth position is the memory pack located in the other processor backplane of a duplexed 3B21D. Memory accesses between backplanes is done when the 3B21D is running in duplex mode. In duplex mode, the offline memory will mirror the active memory. A write to an active main memory circuit pack will cause it to update the memory circuit pack in the other backplane. Since there are six positions that can request a

memory access, the main memory circuit pack must arbitrate simultaneous requests and grant them based on an internally programmed priority protocol.

The memory slot has two major interfaces. The first is the main memory bus which links it to the five backplane positions that can access the memory. The bus contains 32 data bits, 28 address bits, an 8 bit command word, plus 4 bits for error reporting. In addition, there are individual signals provided for memory access to each position. The second major interface is the update bus that connects to the KLW32 memory position in the other CU in a duplex 3B21D. Physically, this interface consists of five flat ribbon cables, each containing 25 pairs of twisted wire. The signals in the update bus are sent as differential signals on the cables.

In addition to the memory update signals, the update bus contains four signals used to implement the backup maintenance channel. This channel is used by the active processor in a duplex 3B21D to reset the other processor in certain situations where the regular maintenance channel is determined to be not working.

The KLW32 supports boundary scan, and is linked to the KLW31 circuit pack through the serial boundary scan bus.

2.1.5 DUAL SERIAL CHANNEL / DIRECT MEMORY ACCESS (B.6 - B.7)

The basic apparatus can have one or two KBN15 direct memory access controller (DMAC) circuit packs. Each DMAC interfaces with the KLW31 circuit pack through the CCIO bus. Each DMAC can also access memory in the KLW32 MM circuit pack. Data transfers to memory can either be a single word (36 bits) or a block transfer, which is 16 words. The KBN15 also has a quad word access mode that is not used and has been disabled by connecting a wire that grounds the QDINH0 inputs on both DMA0 and DMA1. Peripheral devices such as an IOP communicate to the DMAC using a dual serial channel (DSCH) port, which then interfaces a memory or the processor. The peripheral can access memory in the KLW32 in one of two modes of operation, set up by the CC. Unexpanded mode gives the peripheral access to 128K bytes of memory. Expanded mode allows 256 jobs, each of which can access 128K bytes.

A KBN15 circuit pack contains 16 dual serial channel ports, grouped into four channels, each containing four devices. Each circuit pack has two interrupt outputs which are routed to a terminal field at EQL 13-037 adjacent to the CC circuit pack. These are wired as required to the appropriate CC interrupt input pins. The DMA0 circuit pack at EQL 13-075 is powered by CONVA. If DMA1 is installed, then it will require a 410AA power converter to be installed at the CONVB position.

The KBN15 circuit packs support boundary scan.

2.2 INPUT OUTPUT PROCESSOR

The SD3T011 schematic drawing shows the UN33, TN983, and UN375 symbols. However, any of the peripheral controller (PC) slots can be equipped with the TN74, TN75, TN82, TN1420, TN1839, UN580, UN582, UN583, UN933 or UN376 circuit packs.

2.2.1 IOP POWER (B.8 - B.9)

Power control for the IOP power group is provided by a TN1820 or TN1820B IOP power switch (IOPPS). This circuit pack controls two 410AA DC-to-DC power converters (CONVC and CONVD). CONVC provides +5 volt power (P5VC) for the IOPPS, KBN10 (IOP), and eight positions in PC00-03 and PC10-13. CONVD provides +5 volt power (P5VD) for the seven positions in PC20-23 and PC30-32. Each 410AA and the TN1821 has its own separate -48 volt input. The converters are turned on by the ICSTN and the ICSTP signal pair. IINTA0, IINTB0, and IINTC0 are interlock inputs to the IOPPS. The primary interlock allows CONVC to operate only if the KBN10 (IOP) circuit pack is installed. The secondary interlock senses when a peripheral controller circuit pack is installed in any of the PC20-23 or PC30-32

slots. If CONVD is required, but not installed, turning on the IOP power will turn on CONVC, but it will also produce a secondary interlock fault. CPCP and CPCN comprise the signals used to program the overcurrent protection circuit for CONVC. CPDP and CPDN are the equivalent signals for CONVD.

The major alarms, MJ and MJR, and the power alarms PA and PAR, are activated if there is a primary or secondary interlock fault, or if there is a converter low voltage alarm. The MJ and MJR circuit also closes if -48 volts is not present to the TN1820. Both alarm circuits are connected in parallel to the other power switches in the backplanes.

ICALM0 and ICBLM0 are low voltage alarm outputs from the two power converters. The functionality of the alarm inputs differs in the TN1820B and TN1820. The TN1820 will turn off power to both CONVC and CONVD if either ICALM0 or IBALM0 are active. The TN1820B will turn off CONVC and CONVD if ICALM0 is active. For both power switch controllers, either active low voltage alarm will cause the power and major alarm outputs to be activated.

The power switch status is encoded into the ISCXP/N and ISCYP/N scan outputs. The ISCZP/N scan output reflects the state of the FALM1 input, which is tied in parallel with the FALM1 input on the TN1821 CU power switch. All three scans are cabled to the PC02 controller in the other CU. Also part of the same cable are the OOSP/N and RQIPP/N input pairs.

The TN1820 and TN1820B provide +12, -12, and -5 volt power to all fifteen positions in the four peripheral controller (PC) communities. Internal circuits within the TN1820 and TN1820B circuit pack monitor these voltages and activate a the OOL0 output when any of these three supplies is not within tolerance. FPWRF0 is a signal from the KBN10 used by diagnostics to activate the OOL0 signal for testing purposes.

The TN1820 and TN1820B also function as a secondary boundary scan controller. It will take commands from the active processor using either the serial link to the CC that is in the same backplane, or the differential cable interface from the CC in the other backplane. These signals can be selectively distributed to the KBN10, the fifteen IOP community positions, UN373/UN373B position, TN2116 position, both UN375/UN375B positions, and the UN376/UN376B or UN377 positions. These signals can also be retransmitted off the backplane using a differential boundary scan output port.

2.2.2 IOP (B.10)

The KBN10 input output processor (IOP) is a controller circuit that communicates with the 3B21D processor through a dual serial channel interface connected to the processor's direct memory access (DMA) interface. The KBN10 circuit pack has two DSCH circuits, that are cabled to the KBN10 DMA0 circuit pack in each CU. The KBN10 in turn interfaces with four communities of single board peripheral interface circuits called peripheral controllers (PC). Three of the communities have four PC positions and one has three PC positions, resulting in a total of fifteen available PC positions. Each community has its own common 9 bit data bus, a common 16 bit address bus, and 8 common control leads used by the IOP to control bus activities. Individual PC slots in each community have an additional five separate signals: used to select a PC, to provide interrupts, and to report and acknowledge errors. The bus configuration is identical in format to the (input/output [I/O] microprocessor interface [IOMI]) bus used in the 3B20D IOP community. It is entirely self-contained in the 3B21D basic unit, whereas the 3B20D IOP was equipped on separate units, and used connecting cables. IOMI cables are not required, nor supported for the 3B21D.

The KBN10 supports boundary scan, and a boundary scan interface is provided from the TN1820 IOPPS.

2.2.3 PC00 (B.12)

Position PC00 is reserved for a maintenance terminal controller (MTTYC). This circuit pack has two EAI ports, which are cabled to the KLW31 circuit pack in each CU. It also has one console and one printer port, both of which are cabled to the UN376 PSSD circuit pack in CU1. The SCC ports may be cabled in some

applications. PC00 may be equipped either with a TN983 or a UN583 circuit pack. Both have identical functionality, but have different locations for the printer and MTTY cables. The boundary scan interface at PC00 is not used by the TN983, but is functional in the UN583. The PC00 position shares a fused -48 volt input with PC01.

2.2.4 PC01 (B.13)

Position PC01 is a generic PC controller position that contains wiring to an adjacent terminal field at 04-109 and 04-108 to facilitate cable connections if a UN33 or UN933 circuit pack were installed. Sheet B.12 illustrates pin names for a UN33 circuit pack although all PC circuit packs supported by the 3B21D will work. On these other circuit packs, the terminal field wiring is redundant, and does not interfere with their functions. PC00 and PC01 share a fused -48 volt input.

In theory, position PC01 could be equipped with a UN375 disk drive circuit pack, so B.12 is drawn showing a UN375 symbol. PC01 would access SCSI bus B at terminal fields 04-108 and 04-109. In practice, no disk drive circuit packs are ever equipped at PC01, since it would interfere with the MTTYC controller in PC00.

2.2.5 PC02 (B.14)

Position PC02 is reserved for a UN33 or UN933 circuit pack. Seven groups of scanner and signal distributor (SC/SD) points on this circuit pack are also reserved. Five of these groups, which are power switch SC/SDs are shown on sheet B.14. These signals are routed in the backplane. The other two groups are not shown in B.14. These are: (1) signals on pins 550-555 and 450-455, used for the IOPPS scan cable, and (2) signals on pins 333-335 and 233-235, which are used for a fan alarm cable.

The scan signals must be isolated from the backplane power and grounds, or the UN33 or UN933 will fail its diagnostics. PC02 and PC03 share a fused -48 volt input with PC03.

Two terminal fields at EQLs 04-116 and 04-117 also contain the hard wired SC/SD signals.

2.2.6 PC03 (B.15)

Position PC03 is a generic PC controller position. PC03 shares a fused -48 volt input with PC02.

Like the PC01 position, PC03 could be equipped with a disk circuit pack, so sheet B.15 is drawn showing a UN375 symbol. PC03 would access SCSI bus B at terminal fields 04-116 and 04-117. Installation of a UN375/B/C would however, prevent the installation of the reserved UN33 or UN933 at PC02, and is not done in practice.

2.2.7 PC10-PC13 (B.16 - B.19)

Positions PC10-PC13 are generic peripheral controller positions that also have been wired to adjacent terminal fields to facilitate cable connections when a UN33 or UN933 circuit pack is installed. Sheets B.16 - B.19 illustrate pin names for the UN33 circuit pack, although all supported PC circuit packs will also work. The terminal fields that contain the supplementary scan wiring are shown on each sheet. PC10 and PC11 share a fused -48 volt input. PC12 and PC13 share a fused -48 volt input.

A UN375/UN375B/UN375C SCSI disk circuit pack may optionally be installed at PC11 or PC13. PC11 will be connected to terminal fields at 04-144 and 04-145 for access to SCSI bus B. PC13 will be connected to terminal fields at 04-161 and 14-160 for access to SCSI bus B. SCSI jumper connectors are required at these terminal fields to connect to the SCSI busses. Installation of a SCSI peripheral circuit pack would also require a power switch scan cable and an alarm cable.

2.2.8 PC20-23 (B.20 - B.23)

Positions PC20-23 are generic peripheral controller positions. IINTC0 is the secondary converter D interlock signal, routed to a pin normally used as a ground on all PC circuit packs. Installation of a PC circuit pack in this PC community will require installation of a 410AA at the CONVB position. PC20 and PC21 share a fused -48 volt input. PC12 and PC13 share a fused -48 volt input. A UN375/UN375B/UN375C SCSI peripheral may optionally be installed at PC21 or PC23. PC21 will be connected to terminal fields at 13-108 and 13-109 for access to SCSI bus A. PC23 will be connected to terminal fields at 13-116 and 13-117 for access to SCSI bus A. Installation of a SCSI peripheral circuit pack would also require a power switch scan cable and an alarm cable.

2.2.9 PC30-32 (B24 - B.26)

Positions PC30-32 are generic peripheral controller positions. All three slots use +5 volts from power converter CONVD. IINTC0 is the interlock signal used by the TN1820 to detect circuit packs in this PC community. All three positions share a fused -48 volt input.

Position PC30 is wired to terminal fields at 13-136 and 13-137 to facilitate cabling if a UN33 or UN933 were installed.

A SCSI circuit pack peripheral may optionally be installed at PC32. This position is denoted as SPU4 (SPU5 if CU1) when a UN375 is equipped. SPU04 will be connected to terminal fields at 13-108 and 13-109 for access to SCSI bus A. The UN375 has alarm outputs and scan SC/SD points. When a UN375 is equipped here, a UN33 or UN933 is installed at the PC30 position, and a scan cable is connected between PC30 and SPU04. The major and power alarms from SPU4/5 are not connected.

2.3 DISK FILE CONTROLLER

2.3.1 DFC (B.27 - B.30)

The UN373 or UN373B and TN2116 make a SCSI disk file controller (DFC), with power provided by power converter CONVE. The UN373B supports Auto Restart while the UN373 does not. An alternate arrangement allows a UN580 circuit pack to be equipped in place of the UN373. The UN580 includes the functionality of both the UN373 and TN2116 and also supports Auto Restart. A TN2116 is not required when the UN580 is equipped. The DFC supports two independent differential SCSI buses, called SCSI A and SCSI B. Each bus has 50 signals which are routed as differential pairs in the backplane. Bus A is connected to the UN373/UN580, the UN375 at 13-162, and the UN376 at 04-162. It is also connected to four terminal fields. Bus B is connected to the UN373/UN580 and the UN375 at 04-170. It is also connected to five terminal fields. Additional SCSI devices may be added to the system in the following ways. One is to extend the backplane SCSI buses through cables to another device or backplane. The other is to install SCSI peripherals in the IOP community slots and then to connect them to the SCSI buses through backplane connectors.

The UN373B and UN580 have two dual serial channel (DSCH) ports. These two interfaces are cables to the DMA0 circuit packs in CU0 and CU1. The UN373B and UN580 also contain SCSI bus interface circuitry, and two SCSI protocol controllera. The UN373 interfaces to the TN2116, which processes commands and directs information to the two SCSI buses. The UN580 includes the TN2116 functionality onboard. The power switch SC/SD nets are directly connected to the UN33 or UN933 at PC02. The major alarms MJ and MJR, and the power alarms PA and PAR are connected in parallel to the other power switch circuit packs.

Power control for the DFC group is provided by the UN373B or UN580. The UN373B is interlocked to the TN2116 and the 410AA converter (CONVE) with the DINTA0 and DINTA10 signals. The UN580 does not require an interlock, since it will not power up if CONVE is not equipped. PA/PAR outputs from the other power switch controllers. The SC/SD scan points are directly connected to reserved fields in the

UN33 or UN933 at PC02.

2.3.2 SCSI DISK 1 (B.34)

This position accepts a UN375 or UN375B SCSI disk circuit pack. The UN375B supports Auto Restart while the UN375 does not. A SCSI peripheral in this slot is directly connected to SCSI bus B. 3B21D system terminology will call this position SPU01 in CU0, and SPU03 in CU1. The same terminology will refer to SCSI bus B as SCSI 1 in CU0 and SCSI 3 in CU1. No additional cables or connectors are required to use this peripheral.

The alarm outputs from the UN375/UN375B are connected in parallel to the MJ/MJR and PA/PAR outputs from the other power switch controllers. The SC/SD scan points are directly connected to reserved fields in the UN33 or UN933 at PC02.

2.3.3 SCSI TAPE OR PORT SWITCH (B.35)

This position is dual purpose: in CU0, it is equipped with the UN376 or UN376 SCSI tape circuit pack, The UN376B supports Auto Restart while the UN376 does not. in CU 1, it is equipped with a UN377 port switch circuit pack. Both applications are powered by the fused -48 volt input at this position. The UN377 port switch will also use +5 volts from power converter CONVC to power non-critical internal circuitry.

The port switch application is installed in CU1, and cabled to the TN983 circuit packs in both CU0 and CU1. It receives console and printer data from both CUs, and transmits the information from the active CU to the display terminal or printer. It has scan points that are directly routed to reserved fields in the UN33 or UN933 at position PC02. These are used to decode the state of the port switch. The UN377 port switch also contains 24 opto-isolator devices with their IOs brought out to the circuit pack pins (SC[00:11]).

The UN376/UN376B SCSI disk application will be connected to SCSI bus A in CU0. Alarm outputs from this circuit pack are connected in parallel with the MJ/MJR and PA/PAR outputs from the other power switch controllers. The SC/SD scan points are directly connected to reserved fields in the UN33 or UN933 at PC02.

2.3.4 SPARE PORT SWITCH SLOT (B.36)

In CU1, space at 04-178 may be used to equip a second port switch. This circuit pack position shares -48 volt input power with the regular port switch slot at 04-186. It also receives +5 volt power from CONVC. The only connections are the power leads and a boundary scan port. All other signals would be applied using cables.

2.4 SCSI TERMINAL FIELDS (B.37 - B.38)

Sheets B.35 and B.36 illustrate the terminal fields available on SCSI buses A and B. Bus A has four terminal field pairs and Bus B has five terminal field pairs. Each pair contains fifty signals. Those signals that are not grounds, are routed as differential pairs. SCSI bus terminations are installed at 04-101 and 13-101. If it is desired to extend either bus to an SCSI device that is located off the backplane, the bus terminations are removed, and an SCSI cable attached.

2.5 BUS TERMINATIONS

The following bus termination resistor assemblies are used:

9824AP	13-075-732
9824AR	13-075-700
9824AS	13-018-532

The following SCSI terminations are used:

ED3T076-40G3	04-186-500
ED3T076-40G3	13-178-300
ED3T076-40G3	04-101-000
ED3T076-40G3	13-101-000

3. DETAILED DESCRIPTION

Refer to the individual circuit pack schematics and circuit descriptions (CDs) for additional information.

4. REFERENCE DATA

4.1 WORKING LIMITS

The unit will operate with an input voltage on the power converters from -39.5 volts to -57.0 volts. In addition, input power can range from 0 to -60 volts with no damage to any power converter components.

With the above constraints, nominal voltage output from the 410AA power converters is plus or minus two percent of the set point voltage (5.0 volts).

5. REASONS FOR REISSUE 2

5.1 Incorporate external wires into backplane

In the previous issue 1 release, the following connections were made via external backplane wiring on the 3B21D backplane. For issue 2, the connections are made in the backplane.

1. The pins at EQL 04-065-400, 04-065-200, and 04-065-000 are connected to P5VC, which disables the OOL20, OOL10, and OOL30 inputs for the KBN10 circuit pack.
2. The MJ, MJR, PA, and PAR outputs from the UN373/UN373B, UN377, UN375/UN375B, TN1820/TN1820B, and TN1821/TN1821B circuit pack positions are connected in parallel.
3. At position PC30, EQL 13-130 pin 108 is connected to the IINTC0 signal. It was previously connected to ground in earlier artwork and required an isolate and a wire to connect to IINTC0.
4. At position PC00, EQL 04-094 pin 108 is connected to ground. It was previously connected to signal IINTC0 in the earlier artwork, and required an isolate.

5.2 Ground Changes

Changes were made to the following pins. They do not affect functionality.

1. Pins 500 and 524 at EQL's 04-102, 04-110, 04-130, 04-138, 04-146, 04-154, and 13-130 are grounded in issue 2. They were previously unconnected. All circuit packs that use these positions had grounds on these pins.
2. Pins 451, 447 and 448 at EQL 04-186 are now unconnected in issue 2. They were previously grounded. These pins were not used by the circuit packs that are equipped at this position.

5.3 Functional Changes

The following items were new in issue 2.

1. The low voltage alarm outputs from power converter A and B are separated and routed to the CU power controller as two signals, rather than as one common signal. The TN1821B circuit pack can recognize the two alarm outputs. The TN1821 circuit pack ties the signals together again within the

circuit pack. The new signal is CCBLM0.

2. The low voltage alarm outputs from power converter C and D are separated and routed to the IOP power controller as two signals, rather than as one common signal. The TN1820B circuit pack can recognize the two alarm outputs. The TN1820 circuit pack ties the signals together again within the circuit pack. The new signal is ICBLM0.
3. The TCKB signal is split into two signals, TCKB and TCKB1, to improve signal integrity.

6. REASONS FOR REISSUE 3B

6.1 Functional Changes

The following items are new in issue 3B.

1. Pin 04-094-022 was formerly grounded, but is now isolated to become a no-connect or pass-thru pin. This was done so that slot 04-094 would be compatible with the UN583 Maintenance Terminal Controller (MTTYC) circuit pack, which uses this pin as a signaling connection. This change does not affect functionality if a TN983 is equipped in slot 04-094.
2. The UN580, UN933, and UN583 circuit packs are discussed in this CD.

7. ACRONYMS

CC	Central Control
CD	Circuit Description
CCIO	Central Control Input Output
CONVA	Converter A
CONVB	Converter B
CONVC	Converter C
CONVD	Converter D
CONVE	Converter E
CPU	Central Processing Unit
CU	Control Unit
CUPS	CU Power Switch
DFC	Disk File Controller
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DSCH	Dual Serial Channel
EAI	Emergency Action Interface
EQL	Equipment Location
EX	Expansion
IO	Input/Output
I/O	Input/Output
IOP	Input/Output Processor
IOMI	Input/Output Microprocessor Interface
IOPPS	IOP Power Switch
LED	Light Emitting Diode
MJ	Major Alarm
MJR	Major Alarm Relay

MM	Main Memory
MTTYC Maintenance Terminal Controller	
PA	Power Alarm
PAR	Power Alarm Relay
PC	Peripheral Controller
PSSD	Port Switch Signal Distributor
SCC	Signal Control Center
SC/SD	Scanner and Signal Distributor
SCSI	Small Computer System Interface
SPU	SCSI Peripheral Unit
UC	Utility Circuit

AT&T BELL LABORATORIES

DEPT