COMMON SYSTEMS
3B21D COMPUTER
GROWTH UNIT
CIRCUIT

CONTENTS

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The growth backplane unit provides additional functionality to the 3B21D duplex processor. It provides a growth input/output processor (IOP) controller with space for up to sixteen additional peripheral controller circuit packs. At the same time, it supports a growth disk file controller (DFC) subsystem. As an alternate to IOP growth, the growth backplane can be fitted with one to eight small computer system interface (SCSI) peripheral units with the DFC, or one to nine SCSI units without the DFC. Finally, the growth backplane may be configured with a mix of SCSI peripherals and peripheral controllers.

2. GENERAL DESCRIPTION

2.1 GROWTH IOP

2.1.1 IOP POWER (B.1 - B.2)

Power control for the IOP power group is provided by a TN1820 or TN1820B IOP power switch (IOPPS) shown in sheet B.1. This circuit pack controls two 410AA DC-to-DC power converters (CONVF and CONVG), shown on sheet B.2. Converter CONVF provides +5 volt power (P5VF) for the IOPPS, the KBN10 circuit pack on sheet B.6, and eight positions in peripheral controller (PC) communities 0 and 1. Power converter CONVG provides +5 volts power for eight positions in PC communities 2 and 3. Power control is provided by a TN1820 or TN1820B. The TN1820B differs from the TN1820 in that it supports auto restart. The auto restart function allows a power controller to restart automatically if -48 volt power has been removed and then reapplied, and if the power controller's power switch is ON. This function is useful for an automatic restart of the hardware after a power outage. The TN1820 or TN1820B and each 410AA circuit pack have their own fused -48 volt input.

The TN1820 or TN1820B turns on both 410AA converters using the ICSTP and ICSTN signals. It contains a power interlock circuit which uses the IINTA0, IINTB0, and IINTC0 signals. This interlock does not require the KBN10 to be equipped. It does require converter F to be equipped. If converter F is not equipped, and converter G is, power will not be applied. If both converter F and G are equipped, both converters will operate. If only converter F is equipped, it will always operate. If only converter F is equipped, and if there are any peripheral controller circuit packs installed in either PC community 2 or 3, the interlock circuit in the TN1820 or TN1820B will indicate a fault, because the circuit packs in PC communities 2 and 3 would have no power.

ICALM0 and ICBLM0 are low voltage alarm outputs from the two power converters. The TN1820 or TN1820B has two pairs of alarm outputs, called the major alarm and the power alarm. Each alarm pair is connected to a relay contact that closes when the alarm is activated. MJ and MJR are the major alarm and major alarm return signals. PA and PAR are the power alarm and power alarm return signals. The major alarm is closed if: (1) the TN1820 or TN1820B loses its -48 volt power, (2) there is an interlock fault, or (3) either low voltage alarm is active. The power alarm behaves the same, except it requires the -48 volt input to be present. These two alarms must be connected through a cable to an alarm grid to be used.

Power switch status is encoded into the ISCXP/N and ISCYP/N outputs and is sent to a UN33 scanner distributor circuit pack at position PC02 within the PC community in the basic 3B21D units. Also in this cable are the OOSP/N and RQIPP/N signals from PC02, which are used to drive TN1820 or TN1820B faceplate indicators. The ISCZP/N scan outputs are not used when the TN1820 or TN1820B is installed in the growth backplane. This output circuit pair is closed when the FALM1 input, which is also unused, is asserted low.

IPWRCLR0 is a power-on-reset to the KBN10. CPCP and CPCN connect programming resistors in the KBN10, TN1820 or TN1820B, and any circuit packs in the PC communities 0 and 1 to the current limiting

protection circuit in power converter CONVF. CPDP and CPDN are the equivalent signals for PC communities 2 and 3 for power converter CONVG.

The TN1820 or TN1820B also provide +12 volt, -12 volt, and -5 volt outputs. These outputs are sent to all four PC communities for use by the peripheral controllers. OOL0 is a signal sent from the TN1820 or TN1820B to the KBN10 to indicate if any of these three voltages are not within specifications. FPWRF0 is a signal from the KBN10 used to activate OOL0 for testing purposes.

The final function of the TN1820 or TN1820B is to relay boundary scan information from the active 3B21D processor. When installed in the growth backplane, boundary scan data is received as differential data through a cable attached to the TN1820 or TN1820B in the basic IOP. This data can then be retransmitted as digital data to any of the other circuit pack positions in the growth backplane using the BSSEL[00:21]0 signals to select a particular position. The data can also be retransmitted to another backplane by attaching a cable to the differential output pins. The boundary scan control logic in the TN1820 or TN1820B is normally inactive, and must be programmed ON by an incoming boundary scan data stream.

2.1.2 IOP PERIPHERAL CONTROLLER (B.6)

The KBN10 and TN1820 or TN1820B circuit packs, and one or two 410AA power converters make up a growth IOP.

The KBN10 input output processor (IOP) is a controller circuit that communicates with the 3B21D processor through a dual serial channel interface connected to the processor's direct memory access (DMA) interface. The KBN10 circuit pack has two dual serial channel (DSCH) circuits, which are cabled to the KBN10 DMA0 circuit pack in each CU. The KBN10 in turn interfaces with four communities of single board peripheral interface circuits called peripheral controllers (PCs). Each of the communities have four PC positions. The communities are referred to as either IOP or PC communities. Each PC community has its own common nine bit data bus, a common 16 bit address bus, and eight common control leads used by the IOP to control bus activities. Individual PC slots in each community have an additional five separate signals, used to select a PC, to provide interrupts, and to report and acknowledge errors. The bus configuration is identical in format to the (input/output [I/O] microprocessor interface [IOMI]) bus used in the 3B20D IOP community. It is entirely self-contained in the 3B21D basic unit, whereas the 3B20D IOP was equipped on separate units, and used connecting cables. IOMI cables are not required, nor supported for the 3B21D.

The KBN10 supports boundary scan, and a boundary scan interface is provided from the TN1820 or TN1820B IOPPS.

2.2 DISK FILE CONTROLLER

2.2.1 DFC (B.3 - B.5)

A growth disk file controller (DFC) is configured in the growth backplane by installing a UN373 or UN373B, a TN2116, and a 410AA power converter. The UN373B differs from the UN373 in that it supports auto restart. The UN373/UN373B at 04-180 has two DSCH ports which allow the DFC to communicate with the 3B21D processors. When equipped, the UN373/UN373B DSCH ports are connected to the KBN15 DMA0 circuit packs in both CU0 and CU1 of the 3B21D. The UN373/UN373B also contains an interface circuit for two SCSI ports and SCSI protocol control circuitry. Each port is directly connected to one of the two SCSI buses in the growth unit. A TN2116 is required with the UN373/UN373B. It contains the processor that operates the DFC. The 410AA, which is power converter (CONVH), provides +5 volt power for both the UN373 and TN2116.

2.2.2 DFC BOUNDARY SCAN

The UN373/UN373B supports boundary scan, while the TN2116 does not. The UN375/UN375B SCSI peripheral circuit pack does not support boundary scan. To use boundary scan, a suitable controller must be installed at the 04-026 position. At this time, only the TN1820 or TN1820B circuit pack will serve this purpose. Installation of the TN1820 or TN1820B also requires installation of a 410AA at the converter F position. At this time, use of the boundary scan in a growth DFC is not anticipated.

2.2.3 SCSI INTERFACE

Two independent SCSI buses, called SCSI "X", and SCSI "Y", are routed in the backplane and directly connected to the UN373 position. Both buses are routed to five terminal field positions located within the four PC communities. SCSI peripherals can be installed in the PC slots and connected to the appropriate SCSI bus terminal fields. The backplane capacity provides up to four SCSI units on either SCSI bus, if the DFC is present. When the DFC is not equipped, a SCSI peripheral unit may also be installed at 04-180 in place of the UN373, and SCSI bus X will now have up to five SCSI units. In this case, the SCSI DFC controller is on another backplane and must be cabled to the growth backplane with SCSI cables. There is flexibility in how SCSI devices and the DFC may be equipped on the growth backplane. An equipped DFC could be used to interface with only with SCSI devices on another backplane, for example.

2.2.4 DFC POWER

The UN373 and UN373B circuit packs also have power switch control circuitry to operate the 410AA power converter CONVH. The power interlock requires the TN2116 to be present to turn on CONVH. If not, the UN373 major and power alarms are set. These operate much like those in the TN1820 or TN1820B, described in 2.1.1. Like the TN1820 or TN1820B, there are two scan output pairs, DSCXP/N and DSCYP/N, used to denote power switch status.

2.3 PC COMMUNITIES (B.7 - B.22)

The four PC communities each contain four circuit pack positions. All sixteen positions receive commands and communicate data to the KBN10 IOP controller. These positions all have the standard IOMI bus interface.

2.3.1 UN33 SCANNER CAPABILITY

The UN33 is a circuit pack that contains 48 scan input pairs and 32 scan distributor output pairs which are cabled to other circuit packs as needed. To facilitate the grouping of signals on cable fields, some of the scan inputs and distributor outputs are also connected to an adjacent pair of terminal fields. These connections appear on the 3B21D growth backplane at PC positions PC02, PC03, PC10, and PC11. Sheets B.9 through B.12 are drawn showing a UN33 in these positions. These four positions can also accept any other peripheral controller. Positions PC11 and PC10 can also accept a SCSI peripheral circuit pack.

2.3.2 SCSI PERIPHERAL CAPABILITY

The UN375 or UN375B SCSI disk circuit pack and UN376 or UN376B SCSI tape circuit pack can both be installed in the PC community positions. The B-series on these two circuit packs support auto restart. Otherwise, they are identical. The SCSI peripheral circuit packs are wider than the normal UN circuit pack and require two pack positions. SCSI devices may be installed at PC01, PC03, PC11, PC13, PC21, PC23, PC31, and PC33. The SCSI devices will not interfere with the IOMI signals from the IOP controller, if one is equipped. SCSI peripherals and PC circuit packs can be installed together in the growth backplane. The SCSI peripherals will require a backplane connector to interface with the SCSI buses provided in the backplane. In addition to the backplane connection that must be made to a SCSI bus, a SCSI peripheral also requires that a scan cable be provided to monitor its internal power controller status. The SCSI

peripherals also have major and power alarm outputs, but these are typically not monitored, as the scan outputs provide similar information.

2.3.3 PC COMMUNITY POWER

Every two PC community slots share a fused -48 volt power input. All sixteen positions receive +12 volts, -12 volts, and -5 volts from the TN1820 or TN1820B, when it is equipped. IOP communities 0 and 1 receive +5 volts from power converter F, IOP Communities 2 and 3 receive +5 volts from power converter G.

2.4 BUS TERMINATIONS (B.23)

If the DFC is equipped in the growth backplane, SCSI bus termination assemblies (ED3T076-40-G3) are installed at the following locations.

04-180-500
04-180-300
04-063-000
04-063-000

3. DETAILED DESCRIPTION

Refer to the individual circuit pack schematics and circuit descriptions (CDs) for additional information.

4. REFERENCE DATA

4.1 WORKING LIMITS

The unit will operate with an input voltage on the power converters from -39.5 volts to -57.0 volts. In addition, input power can range from 0 to -60 volts with no damage to any power converter components.

With the above constraints, nominal voltage output from the 410AA power converters is plus or minus two percent of the set point voltage (5.0 volts).

5. REASONS FOR REISSUE

5.1 Nonfunctional Changes

The backplane artwork was corrected to eliminate wiring and pin isolates needed in issue 1. These are:

1. The pins at EQL 04-011-400, 04-011-200, and 04-011-000 are connected to P5VC, which disables the OOL20, OOL10, and OOL30 inputs for the KBN10 circuit pack. In previous artwork, these connections were wired.
2. Pin 315 at EQL 04-148 is connected to signal DMA3101. In previous artwork, this pin required an isolation and a wired connection to DMA3101.
3. Pin 315 at EQL 04-116 is connected to signal DMA2101. In previous artwork, this pin required an isolation and a wired connection to DMA2101.

5.2 Functional Changes

The following items are new in issue 2.

1. The low voltage alarm outputs from power converters C and D are separated and routed to the IOP power controller as two signals, rather than as one common signal. The TN1820B circuit pack can recognize the two alarm outputs. The TN1820 circuit pack ties the signals together again within the circuit pack.

6. ACRONYMS

CD	Circuit Description
CONVF	Converter F
CONVG	Converter G
CONVH	Converter H
DFC	Disk File Controller
DMA	Direct Memory Access
DSCH	Dual Serial Channel
I/O	Input/Output
IOMI	I/O Microprocessor Interface
IOP	Input/Output Processor
IOPPS	IOP Power Switch
MJ/MJR	Major/Major Alarm Return
PA/PAR	Power Alarm/Power Alarm Return
PC	Peripheral Controller
SCSI	Small Computer System Interface

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