COMMON SYSTEMS
3B21D PROCESSOR
COMPUTER SYSTEMS
CIRCUIT

Description of Changes

The following circuit pack options are allowed:

- A UN583 may be used in place of a TN983 at EQL 19-094 and 45-094. The EAI, ROP, and MTTY cable connections to the UN583 change when it is equipped.

- A UN933 may be used in place of a UN33 at EQL 19-110 and 45-110.

- A UN580 may be used in place of a UN373 at EQL 28-178 and 53-178. When a UN580 is equipped, the TN2116 at EQL 28-170 and 53-170 is removed.

- All three of the above circuit pack options will require appropriate software upgrades.

AT&T

NQ9430200-hs

**COMMON SYSTEMS
3B21D PROCESSOR
COMPUTER SYSTEMS
CIRCUIT**

CONTENTS

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The 3B21D computer is a high reliability, fault tolerant duplex computer. It is bit compatible with the 3B20D computer that is used in AT&T switching products. It is used as the administrative module (AM) in applications such as 5EI, 5EUS, Autoplex™ cellular equipment, 1A ESS™, and signal transfer point (STP). Its primary feature is its excellent reliability, achieved by hardware with built-in error checking and fault detection circuitry, and an operating system which monitors the hardware and provides many levels of software recovery.

1.2 GENERAL DESCRIPTION OF OPERATION

To obtain a general description of the 3B21D functionality, refer to circuit description (CD) 3T011-01 and CD 3T012-01 which describe the processing and growth units. In addition, consult the individual circuit pack CDs for the KLW31, KLW32, KBN10, KBN15, UN373, and TN2116.

1.2.1 Configuration (B.1)

Sheet B.1 of schematic drawing (SD), SD3T015-01 shows the maximum 3B21D configuration consisting of two peripheral growth cabinets which contain one or two nine track small computer system interface (SCSI) drives, and the processor cabinet containing the duplex 3B21 processor. There are four separate SCSI buses available in a 3B21D. As nine track units are added to a 3B21D system, they are installed on separate SCSI buses. This limits the growth to four nine track units, but enhances reliability and provides a control on the maximum length of each SCSI bus. The SCSI nine track drives require nominal 110 or 220 VAC. The processor requires 48 VDC. It is anticipated that most applications will not require more than one peripheral growth cabinet. Many applications will not require the SCSI nine track tape drive and will use the UN376 SCSI DAT drive that is equipped in processor 0. These applications will then only require the processor cabinet.

The processor cabinet is provided with a printer and a control console.

1.2.2 Processor Cabinet (B.2)

The processor cabinet has six units. Two of these units are always equipped with the two processor units, processor 0 and processor 1. The middle unit is equipped with the fan unit which contains six fans, three blowing upward and three blowing downward. The top units hold the fuse unit, which receives and redistributes -48 volt DC power. The remaining upper and lower units may be equipped with optional growth units.

Sheet B.2 illustrates the cabling arrangements between the two CUs and the rest of the units in the processor cabinet.

1.2.2.1 DFC DSCH (B.3)

Sheet B.3 illustrates the dual serial channel (DSCH) connections for DFC0 and DFC1. This consists of four cables. Each DFC is cross coupled to a DMA circuit pack in processor 0 and processor 1.

1.2.2.2 IOP DSCH (B.4)

Sheet B.4 illustrates the dual serial channel connections for IOP0 and IOP1. This consists of four cables. Each IOP is cross coupled to a DMA circuit pack in processor 0 and processor 1.

1.2.2.3 Growth IOP2 and IOP3 (B.5)

One or two growth IOP units may be equipped in the processor cabinet. The core circuit packs for a growth IOP consist of a KBN10 at equipment location (EQL) 011 in the growth unit, a TN1820 at EQL 026, and a 410AA at EQL 006. The KBN10 must be cross connected to processor 0 and processor 1 with dual serial

channel cables as shown in sheet B.5. IOP3 is connected to DMAC channel 11, device 0 in both CUs. IOP2 is connected to DMAC channel 11, device 2 in both CUs.

In addition, the TN1820 is cabled to the UN33 in the CU with the SCAN1 and SCAN3 cables. The scan cable allows the 3B21D to monitor the status of the TN1820, and also to control the out-of-service (OOS) and RQIPP light emitting diodes (LEDs) on the TN1820 faceplate. The TN1820 also has two pairs of alarm outputs. One is the major alarm (MJ), and is a closed circuit if the TN1820 does not have -48 volt power, or if there is an internal power alarm. The other, called power alarm (PA), is a closed circuit when the TN1820 has an internal power alarm. These may be connected as desired by the application.

1.2.2.4 Growth DFC2 (B.6)

One growth DFC is supported in the lower growth unit. The core circuit packs for a growth DFC consist of a UN373 at EQL 011-180, a TN2116 at EQL 11-172, and a 410AA at EQL 11-190. The UN373 has two dual serial channel ports that are connected to DMA channel 13, device 3 in each 3B21D processor. In addition, the power function scans in the UN373 are connected with the SCAN5 cable to the UN33 at EQL 028-130. Sheet B.6 shows these interfaces, although it does not show the 410AA or TN2116.

The MJ-MJR output on the UN373 is a closed circuit if the UN373 does not receive -48 volt power, or if there is an internal power alarm. The PA-PAR output is a closed circuit when there is an internal power alarm. Applications may wish to connect the MJ and PA alarms as needed.

1.2.2.5 Port Switch (B.7)

The port switch is a circuit pack that receives display and printer information from both IOP0 and IOP1. The TN983 at EQLs 45-094 and 19-094 control the port switch. Each TN983 has an MTTY and an read-only printer (ROP) cable connected to the UN377 port switch at EQL 45-186. The port switch faceplate has two switches which can be used to force the MTTY and ROP links to either IOP. If the switch is set in "AUTO" mode, the link is chosen at the craft terminal interface. Sheet B.7 shows the two pairs of MTTY and ROP cables connecting to the port switch, as well as the two cables to the ROP and display console (MTTY).

1.2.2.6 EAI (B.8)

The TN983s in IOP0 and IOP1 are cross-connected to the emergency action interface (EAI) circuit in each processor. Sheet B.8 shows this cabling. Recall that each TN983 is routed to the port switch as described in the preceding section.

1.2.2.7 Boundary Scan (B.9)

The 3B21D boundary scan interface allows the active processor to access all circuit packs in the 3B21D cabinet that support boundary scan. The TN1820 circuit pack at EQLs 045-080 and 019-080 are used to relay the boundary scan commands and data. Each processor is cabled to the TN1820 in the opposite control unit, as shown in sheet B.9. In turn, the TN1820 in each IOP is cabled to IOP2 and IOP3. A TN1820 can be equipped in the growth IOPs to receive the boundary scan data.

1.2.2.8 Maintenance Channel (B.10)

The maintenance channel is used to interface processors 0 and 1. The active processor will use it to pass diagnostic commands to the inactive processor. It is also used for maintenance operations, such as the sanity timer reset on the inactive processor. These commands are passed on the maintenance channel cable shown in sheet B.10.

1.2.2.9 IOPPS Cables (B.11)

The fuse unit has two sections. One side provides power to the top half of the cabinet, which includes processor 1, the IOP3/SPU unit, and the three fans that cool these units. The other side powers the lower

half of the cabinet, which includes processor 0, the IOP2/SPU unit, and the three fans that blow downward. Each section of the fuse unit has an alarm output that is activated if a fuse has failed in that section. The alarm for the lower section is connected to the TN1821 in processor 1. The upper section's fuse alarm is wired to the TN1821 in processor 0. The TN821 circuit packs in each unit are connected to the PC02 scanner circuit pack , also in the same unit, which is monitored by software for alarms. For additional redundancy, the fuse alarms are also connected to the TN1820 circuit pack in each unit. The TN1820 scan outputs are then cross-connected to the PC02 in the opposite IOP. Therefore, the fuse alarms for each half of the fuse unit are monitored by software in both processors simultaneously when the 3B21D is in duplex mode. Sheet B.11 shows the scan signals in the TN1820 scan cable. ISCZ reflects the state of the fuse alarm. ISCY and ISCX are used to encode the TN1820 status.

The TN1821 in each processor also has a cabled output for the PA and MJ alarms. The power and major alarm outputs for all of the power controller circuit packs are connected in parallel in each processor. For processor 0, this represents the TN1820, TN1821, UN373, UN376, and the UN375s for MHD-0 and MHD-2. For processor 1, this represents the TN1820, TN1821, UN373, and the two UN375s for MHD-1 and MHD-3. The PA output is activated if the power controller sees a power fault. Power faults include a converter interlock failure, a low voltage output, or an internal controller fault. The major alarm output includes the power alarm faults, plus the condition when -48 volts is not present at the power controller. Although the individual power controllers have scan outputs that indicate the same fault information, many applications also will interface alarm circuitry to the MJ outputs from processor 0 and processor 1, so that they have another means for detecting a power fault in the 3B21D. The cable interface is application dependent. Individual growth IOPs, DFC2, and SPUs also have MJ and PA outputs, but these are not connected to the primary MJ and PA networks for processor 0 and processor 1. An application wishing to add a growth device to the major alarm network would need to provide its own cable.

The cooling unit is cabled to PC02 in each IOP. Although each IOP receives two signal pairs with unique names, the signals are identical. The 3BSCAN01/00 signal indicates when a fan is not running at normal speed. If a fan is off, or is running at high speed, this signal becomes active, and the software reading the scan points reports a fan alarm. The alarm signal latches when set. The 3BRST11/10 signal is used to reset it.

1.2.2.10 Update Cable (B.12-B.16)

The update bus links the two memories in processor 0 and processor 1. In duplex mode, a memory write occurs simultaneously to both memories (KLW32 circuit packs). The update bus consists of five ribbon cables carrying the memory address, data, and command signals. Sheet B.12 shows a cable connected to a terminal field in processor 1 and to the KLW32 in processor 0. The terminal field is used to swap those update base signals that must be cross-connected. This allows the update cable to be manufactured as a point-to-point cable for lowered costs. All the other four cables are connected directly to both circuit pack positions.

The PUDISA, PUDISB, PODISA, and PODISB signals in sheet B.12 are four signal pairs that are not part of the memory update bus. These encode pulse points (PPs) PP14 and PP15 from each processor, which comprise the backup maintenance channel. In the event that the regular maintenance channel is unavailable, these signals are driven in a pattern which allows certain essential commands to be passed between both processors.

1.2.2.11 3B21D Power (D.15-D.16)

The 3B21D requires a separate fused -48 volt input for each 410AA power converter, each power controller (TN1820, TN1821, or UN373), the UN377 port switch, and each UN375 or UN376 SCSI peripheral unit. In addition, every two IOP community slots have a separate -48 volt fused supply, except for IOP community 3 in IOP0 and IOP1 which puts three slots on one fuse. Sheet D.16 illustrates the fuse

arrangements for one half of the processor cabinet. The -48 volt returns are individually routed to each position.

1.2.2.12 SCSI Buses (H1-H3)

Sheet H1 illustrates a block diagram of processor 0 and processor 1 that includes the four available SCSI buses. SBUS0 and SBUS2 are in processor 0 and are controlled by DFC0. SBUS1 and SBUS3 are in processor 1 and are controlled by DFC1. Any bus can be extended with a SCSI extension cable. Sheet H2 illustrates a configuration without growth units. All four buses are contained within the processor backplane. The basic 3B21D is equipped with one UN376 tape drive (MT-0) located at the SPU54 position, and two UN375 disk drives (MHD-0 and MHD-1) at the SPU00 and SPU01 positions. Additional disk or tape drives may be installed at SPU02-SPU05. Therefore, each basic backplane unit may be equipped with a maximum of three SCSI disk drives. All electrical connections for the SPU02 and SPU03 positions are provided in the backplane wiring, minimizing the growth procedure when MHD-2 and MHD-3 are added. The SPU04 and SPU05 positions require a connector to attach the circuit pack to the SBUS. A detail of the 9824AN connector appears in sheet H2. In addition, a scan cable would also be required.

Sheet H3 illustrates two SCSI growth options. Option 1 uses two growth units. The four SBUSs are extended through cables to the upper and lower growth units. Option 2 uses only one growth unit. Each growth unit may be equipped with up to five SCSI peripheral units. Positions SPU18 and SPU19 provide connectivity to the SBUS when a UN375 or UN376 circuit pack is equipped. The other growth positions require a 9824AN connector to attach the peripheral to the SBUS. All growth SPU positions require scan cables. Information note 306 on sheet D5 describes these cables. The SCSI protocol allows a maximum of seven devices on any SBUS. The maximum number of units in any 3B21D configuration would be seven. This would be a fully configured SBUS0, with SCSI nine track unit.

Sheet H4 illustrates the attachment of the SCSI nine track units in the peripheral growth cabinets. In principle, up to four 9 track units could be equipped, with one on each SBUS. The addition of a SCSI nine track unit does not prevent the growth of the SBUS. The SBUS can still be grown to a growth unit, as described in the previous paragraph.

2. DETAILED DESCRIPTION

Refer to the individual circuit pack schematics and circuit descriptions for additional information.

3. REFERENCES

X-20902 *"Manufacturing Testing Requirements for the 3B21D,"* June, 1993.

4. ACRONYMS

AM   Administrative Module
CD   Circuit Description
CU   Control Unit
DAT   Digital Audio Tape
DFC   Disk File Controller
DMA   Direct Memory Access
DMAC   Direct Memory Access Controller
DSCH   Dual Serial Channel
EAI   Emergency Action Interface

EQL   Equipment Location
IOP   Input/Output Processor
ISCX   Part of IOP PS Scan Output for Power Control
ISCY   Part of IOP PS Scan Output for Power Control
ISCZ   Part of IOP PS Scan Output for Power Control
LED   Light Emitting Diode
MHD   Moving Head Disk
MJ/MJR   Major Alarm
MTTY   Maintenance Teletype Terminal
OOS   Out-Of-Service
PA   Power Alarm
PA-PAR   Power Alarm Return
PC02   Peripheral Controller 2
PP   Pulse Points
ROP   Read Only Printer
RQIPP   Request In Progress
SBUS   SCSI Bus
SCSI   Small Computer System Interface
SD   Schematic Drawing
SPU   SCSI Peripheral Unit
STP   Signal Transfer Point
VAC   Volts Alternating Current
VDC   Volts Direct Current

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