2

COMMON SYSTEMS

PROGRAMMABLE READ ONLY MEMORY CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The programmable read only memory (PROM) circuit is used in the 3A central control (CC). The 3A CC is a microprogrammed processor utilizing PROMs for its microprogram store. This microstore contains up to 4096 32-bit words. Each microstore circuit pack (CP) contains four PROMs; each PROM is 1024 words by 4 bits. These memories are arranged for a CP organization of 1024 words by 16 bits. Two of these CPs are read out in parallel to obtain a 32-bit microprogram word. The basic building block of the microstore, then, is 1024 32-bit words, which are contained on two CPs.

SECTION II - DETAILED DESCRIPTION

1. ADDRESS BUFFER

1.01 The selection of a word in the microstore is performed in two steps. First, address bits 0 through 8 of the processor's microprogram store address register (MAR) are bused to all of the microstore CPs. The decoding of these nine address bits is performed on each CP for a one of 512-word selection. Concurrently, address bits 9 through 11 of the MAR are decoded in the processor and a plane select is generated. This plane select lead is designed for the enabling of a pair of microstore CPs containing the 32-bit microprogram word.

1.02 Address information to the microstore CP is derived from the processor's 3-volt collector diffusion integration (CDI) logic. Since all of the devices in the microstore are 5-volt TTL (transistor-transistor logic), an interface is required. This interface is performed on the address and plane select leads by using 3-volt pull-up resistors (R1 to R11) at the input of the buffers in the microstore. Each input to the microstore is driven by a MAR gate on a 1024-word basis. Each gate must drive two of the microstore CPs.

1.03 Address input bits to the microstore circuit, A0 through A8, are pulled up to 3 volts through 470-ohm resistors, then they are buffered and inverted in IC2 and IC3. Finally, these address bits are paralleled to address inputs A0 through A8, respectively, for all four PROMs. Each PROM decodes these nine address bits for a one of 512-word selection.

1.04 Plane select inputs to the microstore circuit pack, designated as plane select low ($\overline{PSL}$) and plane select high ($\overline{PSH}$), are pulled up to 3 volts through 470-ohm resistors. These two signals are then logically combined in IC2 and IC3 to generate the A9 input and the two $\overline{CS}$ inputs of the PROMs. The logical combinations which exist are as follows: When $\overline{PSL}$ is enabled (low) and $\overline{PSH}$ is disabled (high), A9, which is high, selects the lower 512 words of the PROMs. When $\overline{PSH}$ is enabled and $\overline{PSL}$ is disabled, A9, which is low, selects the upper 512 words of the PROMs. When either $\overline{PSL}$ or $\overline{PSH}$ is enabled, both $\overline{CS}$ inputs of the PROMs are enabled (low), allowing data to be gated onto the microstore output bus. When $\overline{PSL}$ and $\overline{PSH}$ are disabled, both $\overline{CS}$ leads on the PROMs are disabled (high), preventing the transfer of the PROMs' data onto the microstore output bus. $\overline{PSL}$ and $\overline{PSH}$ should never be enabled simultaneously. This illegal state would cause data to be outputted onto the microstore output bus at the same time that another microstore CP is selected.

2. MEMORY

2.01 The memory used in the microstore is comprised of four PROMs. These devices are specified as KS-21951 L1, L2, or L3. Although three list numbers are shown for the PROMs, each PROM has only one list number. Only PROMs with the same list number are allowed on the same CP.

2.02 The PROMs are Schottky bipolar devices, each containing 4096 memory cells. Data content within the cell is determined during the programming of the devices. Programming is accomplished by passing an applied current through a selected fusible link. Each memory cell has an associated fusible link. The binary value of the cell is determined by the link being open or left intact. List 1 and List 3 devices use nichrome material for the fusible link. List 2 devices use a polycrystalline silicon material. The selection of four of the 4096 memory cells within the PROMs is performed in two steps. First, while six of the address bits are selecting one of 64 rows of cells, the remaining four address bits are selecting one of 16 columns of cells. In the second step, the chip-selects allow the contents of the four memory cells to be gated onto the outputs of the device.

2.03 At the output of the microstore, a voltage interface is required since the PROM devices are 5-volt TTL and the logic in the processor is 3-volt CDI. This interface is accomplished by using PROM devices with open collector outputs which can be pulled up to 3-volt logic levels by processor logic.

SECTION III - REFERENCE DATA

1.01 None.

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