COMMON SYSTEMS
3B20D MODEL 2 AND 3 PROCESSOR
MAIN STORE AND IOP GROWTH UNIT
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Main Store Growth unit provides up to an additional 32 megabytes of memory depending on the feature selected. The initial memory provided in the growth main store unit was 8 megabytes. This was expanded to 16 Mb using the Expanded Memory Module (EMM), and further growth, up to 32 Mb of memory, was available in the Very Large Memory Module (VLMM) option.

1.02 The IOP Growth Unit provides the capability to grow the 3B20D from two peripheral controller communities to four peripheral communities. This allows the number of PCs to be expanded from eight PCs to sixteen PCs.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The growth main store adds up to eight memory array circuit packs to the 3B20D, controlled by the main store controller in the basic main store unit.

2.02 The growth IOP unit adds two IOP communities, comprising four PCs in each community.

MAIN STORE

2.03 For information regarding the main store, see the "Main Store" paragraphs of the "3B20D, Model 2 and 3, Processor, Main Store, IO, and DFC Unit" Circuit Description (CD-4C099-01).

IOP GROWTH UNIT

2.04 The 3B20D IOP growth unit comprises two communities of single board Peripheral Controllers (PCs). Each community consists of four PCs, and each PC is interconnected to a common 9-bit data bus, a 16-bit address bus, and eight control leads. For each PC, there are five private control signals for requests, errors, interrupts, selection, and acknowledgement. All these signals are wired to the fanout section of the backplane. Each PC is capable of interfacing with up to four separate peripherals, depending on the particular PC design. For a complete description of the IOP operation, refer to CD-4C099-01.

PROCESSOR APPLICATION

2.05 When the growth unit is connected to a 3B20D IOP, the signals mentioned in the above paragraph are cabled to the I/O microprocessor interface section of the basic IOP backplane. The growth unit then extends the IOP capacity from eight PCs (two communities) to sixteen PCs (four communities). In the 3B20D application, communities are separately alarmed.

SECTION II - DETAILED DESCRIPTION

1. MAIN STORE INTERCONNECTION AND FLOW DIAGRAM - FS1

1.01 FS 1 shows the interconnection of the eight memory array circuit pack locations in the Growth Main Store. The three options (S, U, and M) define which memory array circuit pack is to be used to provide the required memory capability. Option S provides the TN28 array for an 8 Mb capability, option U provides the TN56 array for a 16 Mb storage capability, and option M (VLMM) provides the TN2012 for a total of up to 32 Mb of memory.

1.02 With option N, the EADP0 (Extra Address Parity Bit) from the main store controller provides parity for the extra two address bits added in the VLMM option. The data, address, select, and control signals are cabled from the main store controller in the main store unit to memory arrays in the growth main store unit.

2. BUS TERMINATING DIODES - FS2

2.01 FS2 provides the bus terminating diode interconnection information for the growth main store unit signals.

These leads include the data, address, select, and control signals. These diodes are mounted on paddleboard assemblies which are connected to the backplane connector at EQL 04-156.

3. I/O CHANNELS - FS3

3.01 FS3 describes the interconnection and apparatus information for the I/O channels. There are three options available for I/O channels: Dual Serial Channel (Option Z), Application Channel Interface (Option Y), and 3BNET (Option Q). The required connecting information for these options is provided in FS3.

4. PERIPHERAL CONTROLLERS - COMMUNITY 2 AND 3 - FS4

4.01 FS4 contains the interconnection information for the four PCs in community 2 (PC20 -PC23) and the four PCs in community 3 (PC30-PC33). These growth IOP communities (2 and 3) are ordered at the system level drawing and are job engineered per user instructions.

5. IOP GROWTH POWER - FS5

5.01 The schematic for the growth power required is provided in FS5, which includes the 495FA converter and the TN9 power switch. The 495FA converter supplies -5V to the PCs (PC20-23 and PC30-33). The TN9 provides the EIA voltages +/-12V and -5V to the PCs in IOP community 2.

6. POWER CONVERTERS FOR COMMUNITY 3 - FS6

6.01 FS6 contains the interconnection information for the TN9 for IOP community 3. The TN9 supplies +12, -12, and -5 volts, as well as power control to the four PCs in IOP community 3.

7. 5 VOLT POWER FOR MAIN STORE AND IOP - FS7

7.01 The 495FA power converter interconnections for the growth main store and IOP are provided in FS7. The 495FA supplies -5V (P5VF) to the eight main store array circuit packs (FS1 1-8), two I/O channel packs (FS3 3-4), and eight bus terminating diodes (FS2 1-8).

7.02 The 495FA converter is designed to be inserted or removed with -48V applied to the circuit.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The 3B20D Main Store and IOP Growth unit requires -48V -/-10 percent at approximately 6 amperes. The -5 volt logic supply, furnished by the 495FA power converters, must be within -/-10 percent. Memory voltages of -12V and -5V, provided by circuit pack TN9, must also be within -/-10 percent.

1.02 EIA voltages from the TN9 are monitored and must be greater than 4.5 volts.

1.03 When this unit is used in an international system, the converters and TN9B will operate at the ETSI voltage requirements of -39V to -72V.

2. FUNCTIONAL DESIGNATION

CIRCUIT PACKS

Designation	Meaning
ACHI	Application Channel Interface
BUFR	Networking Buffer
DSCH	Dual Serial Channel
IMI	Interconnection Medium Interface
MASA(08-15)	Main Store Array(08-15)
NICP	Network Interface Circuit Pack
PC(20-23,30-33)	Peripheral Controller(20-23,30-33)
PWRCONV(2,3)	Power Converter(2,3)
PWRUE	Power Unit E
PWRUF	Power Unit F

3. CONNECTING CIRCUITS

3.01 When the Main Store and IOP Growth circuit is listed on a keysheet, the connecting information thereon is to be followed:

(a) 3B20D IOP - SD-4C052-02

(b) Circuit Packs and Converters: Power Converters - 495FA Power Converter/Monitor - TN9 Peripheral Controller (per office requirements)

4. MANUFACTURING TEST REQUIREMENTS

4.01 The Manufacturing Test Requirements for the Main Store and IOP Growth Unit Circuit are included in the Manufacturing Test Requirements for 3B20D Processor (Model I, II and III), X-79516.

SECTION IV - REASONS FOR REISSUE

1. CHANGES IN FUNCTIONAL SCHEMATICS OR APPARATUS FIGURES

1.01 This reissue is made to rewrite the circuit description and to provide the information pertaining to the Very Large Memory Module (VLMM) Feature (Option N).

2. DESCRIPTION OF CHANGES

2.01 Note: This reissue also covers information authorized by the following appendixes to Issue 9B of this CD.

APPX 1A	–	DWG ISS 2A
APPX 2AC	–	DWG ISS 3AC
APPX 3D	–	DWG ISS 4D
APPX 4B	–	DWG ISS 5B
APPX 5B	–	DWG ISS 6B
APPX 6B	–	DWG ISS 7B
APPX 7B	–	DWG ISS 8B

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