

COMMON SYSTEMS
3B20D MODEL 2 AND 3 PROCESSOR
CENTRAL PROCESSING UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added isolate pin at EQL 04-138 140 to remove connection to SCR311 node, and added wire from EQL 04-138 140 to EQL 04-110 350 (Option ZV).

E. Reason for Changes

E.1 These changes were made to prevent the cache from skipping "invalidate" operations if the Direct Memory Access Controller (DMAC) writes to main store and the Control Central (CC) asserts the maintenance bit SCR31 at the same time.

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DEPT 55854-DLE-JCL

CIRCUIT DESCRIPTION

CD-4C098-Q1
ISSUE 2B
APPENDIX 3B
DWG ISSUE 13E
DISTR CODE 7N98

COMMON SYSTEMS
3B27D MODEL 2 AND 3 PROCESSOR
CENTRAL PROCESSOR UNIT
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Change terminal numbers on the "MSTMOUTO" net to correct a documentation error.
- D.2 Deleted CCIDO net for CU1. This net belongs on the system drawing, SD-4C127-01.

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DEPT 45182-MPV-HAD

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CIRCUIT DESCRIPTION

CD-40098-01
ISSUE 2B
APPENDIX 2B
DWG ISSUE 12B
DISTN CODE 7N98

COMMON SYSTEMS
3B20D MODEL 2 AND MODEL 3 PROCESSOR
CENTRAL PROCESSING UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Provide the inrush protection feature. The (TN5) power switch circuit pack can be replaced with a new (TN5B) power switch circuit pack that is downward compatible with all Model 2 and Model 3 computers, and provides additional inrush current protection.

E. Reason for Change

E.1 The TN5B power switch circuit pack provides additional inrush protection.

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DEPT 45182-JLW-RGW

CIRCUIT DESCRIPTION

CD-4C098-01
ISSUE 2B
APPENDIX 1B
DWC ISSUE 11B
DSTN CODE 7N98

COMMON SYSTEMS
3B20D MODEL 2 AND 3 PROCESSOR
CENTRAL PROCESSING UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Add option B wiring to FS 1/13, 2/1, and 2/2 to show program resistor net strapping and power connections for basic processor configurations (power arrangement 10). Options D, P and Q are rated Manufacture Discontinued (MD) and replaced by option B to reduce noise sensitivity and simplify the circuit.

D.2 Add CAD 55, Note 314 and 315 to support Option B wiring and modify Notes 302, 303, 310, FS 1/1 and 1/4 to show Options D, P & Q are MD.

D.3 Add option A wiring to FS 1/3, 1/4 and 7/3 to show program resistor net strapping and power connections for control store slots 02, 03 (power arrangement 11). Option A provides power wiring required in addition to option B.

D.4 Add CAD 56 and Note 316 to support Option A wiring.

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COMMON SYSTEMS
3B20D MODEL 2 AND 3 PROCESSOR
CENTRAL PROCESSING UNIT
CIRCUITSECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 The central processing unit (CPU)* is the execution unit of the 3B20D Processor. The CPU obtains an instruction or command from the main store (MS) and translates these commands into a sequence of actions within the 3B20D or its associated circuitry.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The CPU contains the following functional units: microstore, data manipulation unit, special registers, maintenance channel, store interface, cache, main store update, and emergency action interface. The frame also includes slots for the microlevel test set interface (MLTSI) and the dual-access utility circuit (DUC), both of which are optional items.

MICROSTORE SYSTEM

2.02 The microstore system is directed by the microstore controller MC4C076A1 (UN135). This circuit pack controls microstore addressing and sequencing, as well as source and destination bus enabling. The microstore itself consists of four circuit pack

slots, two of which are optional. The first microstore slot (equipment location EQL 036) contains a permanent-memory microstore circuit pack (UN28B). The second microstore slot usually contains a UN48B (4KWMS) or a UN248 (16KWMS) circuit pack. The third and fourth slots are available for application programming and usually contain UN28B or UN48B (4K MEMORY) circuit packs when the slots are equipped. The fourth slot, EQL 058, may also be equipped with a floating point unit (UN140) as a feature.

DATA MANIPULATION

2.03 The data manipulation unit (DMU), which resides on two circuit packs (UN1 and UN23C), provides masking, arithmetic, and logic operations for the 3B20D. The data that results from DMU operations can be stored in internal DMU registers or can be gated to the destination bus that connects to other circuit packs via the backplane.

SPECIAL REGISTERS

2.04 The special registers function resides on two circuit packs, UN2B and UN3B, which contain the processor status word register (PSW), pulse point register (PPR), system status register (SSR), hardware status register (HSR), error register (ER),

* Also called central control (CC) unit in associated documents.

interrupt mask register (IM), interrupt set register (IS), channel data register (CDR), real time counter (RTC), and interrupt timer (IT).

MAINTENANCE CHANNEL

2.05 The maintenance channel (UN22C) allows diagnostic and maintenance access to a 3B20D processor. This channel furnishes communication between duplex processors and supplies access ports to a nonduplex processor. The UN22 interfaces to the processor over the bidirectional gating bus (BGB), the microstore data bus (MSD), the microstore address bus (MSA), and the maintenance bus (MTC).

CPU STORE INTERFACE

2.06 The CPU store interface consists of two circuit packs, the store data control circuit pack (UN6B) and the store address control circuit pack (UN43C). The UN6B provides data information for main store access and also includes the instruction buffer (IB), which contains the current instruction being executed by the microcode. The UN6B also accesses the source and destination buses. The UN43C furnishes addressing information for the main store and also has access to the source and destination buses.

CACHE

2.07 The cache, consisting of three circuit packs (two UN10Bs and one UN11B), contains a small high-speed store that is accessed by the processor before the main store is accessed. Since the cache is faster than the main store, if the cache contains the word being accessed, the processor will run faster. The main store is automatically accessed on a cache "miss".

MAIN STORE UPDATE

2.08 The main store update circuit pack (UN133) arbitrates the use of the main store between four units: one of the 3B20D CCS, one or two direct memory access (DMA) units (if used), and the other 3B20D processor. The UN133 determines which one of the above units controls the main store buses, consisting of the main store address bus, main store data bus, and main store control bus.

EMERGENCY ACTION INTERFACE

2.09 The emergency action interface (EAI) consists of the TN10 circuit pack. The EAI, which is accessed via the maintenance teletype peripheral controller (MTTYPC) in the input/output processor (IOP) unit through the maintenance terminal, supplies a means of manually forcing certain 3B20D recovery configurations in the event that automatic system error recovery is unsuccessful. The EAI also captures processor recovery progress data and forwards it to the MTTYPC.

SECTION II - DETAILED DESCRIPTION

1.01 A more detailed circuit description can be found in the individual circuit pack schematics.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

<u>1.01 NOMINAL</u>	<u>LIMITS</u>
+5 Volt Power	+5.00 Volts \pm 10 Percent Measured at Net P5S

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 None.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

- (a) Power Distribution Circuit, SD-4C053-01.
- (b) 3B20D Model 3 Processor System Circuit SD-4C127-01.
- (c) Moving Head Disk Drive Interface, KS-22072 and KS-22875.
- (d) Circuit Packs and Power Converters per SD-4C098-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are specified in the X79625 specification.

6. TAKING EQUIPMENT OUT OF SERVICE

6.01 This information is contained in the Task Oriented Practice for 3B20D Model 2, BSP 254-302-811.

SECTION IV - REASONS FOR REISSUE

A. Changed and Added Functions

A.1 Provide a power arrangement for the floating point accelerator and cache option features.

D. Description of Changes

D.1 Add Option D and CAD 54 to provide floating point and/or cache option power arrangement 7 for Model 3 applications.

D.2 This reissue also covers information authorized by the following appendixes to Issue 1 of this CD.

<u>APPENDIX</u>	<u>DWG ISSUE</u>
1A	2A
2D	3D
3B	4B
4D	5D
5B	6B
6B	7B
7B	8B
8A	9A

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