COMMON SYSTEMS
3B20D MODEL 2 & 3 PROCESSOR
MAIN STORE, IO AND DFC UNIT
CIRCUIT

CHANGES

D. Description of Change

D.1 Allow new versions of circuit packs to be used:
TN19
MC4C127A1D [option ZJ] in place of MC4C127A1B [option F]
MC3TO97A1 [option ZK]
TN70
TN70C [option ZM] in place of TN70B [option ZL]

E. Reason for Change

E.1 Some of the components on the old circuit packs are either no longer available or are outdated. New components have been used.

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COMMON SYSTEMS
3B20D MODEL 2 AND 3 PROCESSOR
MAIN STORE, IO AND DFC UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added option ZB and information note 319, which adds the VLMM-backward compatible wiring.

D.2 Added option ZC and information note 319 to add the VLMM feature wiring.

D.3 Added option ZE and information notes 312 and 322 to add the UN618 Main Store Controller.

D.4 Added option ZF and information note 323 to add up to eight of the TN2012 4 megabyte main store array circuit pack.

D.5 Added option ZD and information note 320 to add the UN46D as the minimum version of the DMAC circuit pack when installing the VLMM feature.

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COMMON SYSTEMS
3B20D MODEL 2 AND MODEL 3 PROCESSOR
MAIN STORE, IO AND DFC UNIT
CIRCUIT

CHANGES

D. Description of Change

D.1 Provide the inrush protection feature. The (TN3) power switch circuit pack can be replaced with a new (TN3B) power switch circuit pack that is downward compatible with all model 2 and model 3 computers, and provides additional inrush current protection.

E. Reason for Change

E.1 The TN3B power switch circuit pack provides additional inrush protection.

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COMMON SYSTEMS
3B20D MODEL 2 & 3 PROCESSOR
MAIN STORE, IO, AND DFC UNIT CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The main store (MAS), IO, and, disk file controller (DFC) circuit provide: program and data storage for the 3B20D processor, mass storage for the 3B20D processor (in the main store subunit), basic input/output capability between the 3B20D processor and IO devices (in the IO subunit), and firmware control of fixed or removable media disk systems (in the DFC subunit).

2. GENERAL DESCRIPTION OF OPERATION

MAIN STORE

2.01 The main store is physically partitioned into two units, a main unit (J1C147BB-1) and a growth unit (J1C147BC-1). The main unit contains the main store controller (MASC) and up to eight main store memory arrays (MASAs). The growth unit is connected to the main unit via a tape cable assembly and can consist of up to eight additional MASAs. The 3B20D main store growth increment is on a per MASA basis, i.e., each additional MASA increases the addressable memory by 1 or 2 megabytes. The maximum address spectrum of the 3B20D is 16 megabytes without and 32 megabytes with memory expansion.

A. Interface

2.02 The MASC interfaces to the MASAs and, via the main store update (MASU), to the central control (CC)*, direct memory access controller (DMAC), and the other processor. Communication between the two control units is through the MASU in each CU. The MASU controls all access to the MAS and, in the case of multiple store requests, determines which unit has the highest priority and allows access from that unit to the main store buses.

B. Features

2.03 The MASC contains the hamming circuitry, data and address parity check circuits, a timing sequencer for system or refresh store cycles, the array addressing circuitry, and maintenance access circuitry.

2.04 Since the memory used in the 3B20D main store is dynamic, the stored information must be refreshed periodically. The main store controller determines the time and rate at which refresh operations occur. When possible, the controller makes the refresh operation transparent to the

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* Also called central processing unit (CPU) in associated documents.

system by inserting it at the end of a system access.

2.05 The 3B20D main store performs error checking and correction. Hamming circuitry in the main store controller and hamming coding of data in the memory arrays result in the correction of all single-bit errors; this circuitry also flags all double and detectable multi-bit errors. The state of the memory is continually checked during refresh cycles. Each refresh cycle selects a particular memory array, reads the data at the current refresh address, and checks this data for data parity errors. The memory arrays that were not selected are refreshed only. The entire memory is thus verified for good data every 32.8 seconds. In addition to the hamming correction and refresh/data parity checking, the store performs various hardware checks on internal circuitry and bus communications. If the check circuit detects an error, the MAS returns four error signals to the system. Based on the type of error, the CC can attempt to remedy the error, or to mask the error and continue to run. Additional data on the error source is retained in three registers in the store. These registers contain information as to which of the four error sources is applicable, when the error occurred (refresh or system access), and the address that was being accessed at the time of the error.

C. Store Access

2.06 A store access is initiated when the STORE GO signal (SGO0) is received. Upon receiving this signal, the main store controller begins a timing sequence which accesses memory or performs the required maintenance operation. The command leads indicate whether the operation is a WRITE, READ, CLEAR, BYTE, HALFWORD, or MAINTENANCE operation. The store signals the CC that the store no longer requires the address, command, and data buses with the STORE COMPLETE (SCM00) signal. This signal is issued by a timing sequencer in the main store controller to the MASU. The trailing edge of the SCM00 signal from the main store on read operations indicates to the CC that the data on the store data bus is valid.

INPUT/OUTPUT (IO)

A. Physical Description

2.07 The input/output subunit consists of four circuit pack slots. Two of these slots accept the single-board direct memory access controller (DMAC) (UN46), while the other two slots accept the dual serial channel (DSCH) circuit pack (UN9). A minimum equipage would be one UN46 and one UN9.

B. Interface

2.08 The DMAC interfaces with the central control unit via the central control input/output (CCIO) bus. In addition, each UN46 can interface with a maximum of two DSCH boards via the DIO (direct memory access/input/output) bus. Each DSCH can interface with a maximum of 16 devices through five pairs of dedicated wires. These wires connect between the DSCH and each device. The dual serial channel can also communicate directly with the central control via the CCIO bus. Each central control unit can interface with a maximum of two DMACs over the CCIO bus. The DMA also interfaces to the main store over the main store bus.

C. Features

2.09 The purpose of the direct memory access system is to transfer data to or from a peripheral device using its own data transfer control circuitry. This transfer can be a word

transfer (32 bits and 4 parity bits) or a block transfer (16 words). Each device is set up by the CC in one of two modes: expanded or unexpanded. Unexpanded devices have access to up to 128k bytes of main store memory; expanded devices can have up to 256 jobs, each of which has access to 128k bytes of memory.

2.10 The DSCH performs word and block data transfers between the DMA and the devices. The DSCH can also perform interprocessor communication operations (CHIP mode). Data communication to and from devices occurs over two pairs of data leads. The low order bits (0-15) are transmitted serially over the data low lead, and the high order bits (16-31) are transmitted over the data high lead.

DISK FILE CONTROLLER (DFC)

2.11 The DFC interfaces to the 3B20D processor via the DMAC/DSCH. Up to eight moving-head disk drives can be accommodated by a single DFC, giving a gross storage capacity of 1280, 2400, or 2720 megabytes, depending on the disk drive model used.

2.12 The 3B20D DFC consists of a 3B20D processor interface (TN69, TN70); a moving-head disk drive interface (UN54/UN55 and UN64); a 16-bit microprocessor, and its associated program store (TN68/TN19); and a power/power control circuit (TN3). The microprocessor interprets and executes commands generated in the 3B20D processor; provides control input to, and monitors the operational status of the moving-head disk drives; and manages the flow of data between the 3B20D processor and the moving-head disk drives.

2.13 The DFC/3B20D processor interface allows the microprocessor to communicate with the 3B20D processor via a dual serial-bit stream for transmitting data and commands, and a DMAC service request line for transmitting data setup, data transfer, and interrupt requests. The microprocessor communicates directly with the TN70 via 16-bit data and 10-bit address buses. The TN70 serves as a parallel data and command buffer for the microprocessor, while the TN69 functions as a serial/parallel data converter between the TN70 and DSCH in the 3B20D processor.

2.14 The moving-head disk drive interface furnishes the microprocessor access to the moving-head disk drives. The UN54/UN55 contains several registers that are accessible by the microprocessor via the data and address buses; the outputs of this circuit pack form a control bus to the disk drives for selecting a drive, moving the heads on a drive to a specific cylinder, selecting a head from which to READ/WRITE data, and monitoring disk drive status.

2.15 Data transfer between the DFC and the moving-head disk drives takes place on dedicated serial data and clock from each disk drive via the UN54/UN55 and UN64 packs. The UN64 serves as a voltage level converter and multiplexer for serial data and clock signals from up to eight moving-head disk drives.

2.16 The UN64 also performs parallel/serial data conversion; computes and WRITEs a 32-bit error correction code on the disk on a per-sector basis; verifies data byte parity on disk WRITEs; computes data byte parity on disk READs; and processes error correction information on a per-sector basis on disk READs. The UN64 operates under the control of the microprocessor via the address and data buses.

2.17 The 495F1 power unit supplies +5 volt power to each of the circuit packs within the DFC. TN3 furnishes -5 volts to the UN54/UN55 and UN64 circuit packs and also monitors the +5 volt and -5 volt power on the DFC backplane.

2.18 The power switch, TN3, directs the sequencing of power within the DFC, and is controlled by the operator from pushbutton switches mounted at the rear of the pack. During power up/down sequencing, TN3 provides a microprocessor initialization signal that initializes TN69, UN54/UN55, and UN64. In addition, TN3 automatically removes all power when +5 volt or -5 volt power is absent or when any fuse is blown.

SECTION II - DETAILED DESCRIPTION

1.01 More detailed circuit descriptions can be found in the individual circuit pack schematics.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 NOMINAL LIMITS

+5-volt power	+5.00 volts	±10 percent, measured at net +P5S
-5-volt power	-5.00 volts	±10 percent, measured at input to UN54/UN55 and UN64 on DFC backplane

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 None.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) Power Distribution Circuit SD-4C053-01.

(b) 3B20D Model 3 Processor System Circuit SD-4C127-01.

(c) Moving Head Disk Drive Interface KS-22072 and KS-22875.

(d) Circuit Packs and Power Converters per SD-4C099-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are specified in the X-79874 specification.

6. TAKING EQUIPMENT OUT OF SERVICE

6.01 This information is contained in the task oriented practice for 3B20D Model 2 BSP 254-302-811.

SECTION IV - REASONS FOR REISSUE

A. Changed and Added Functions

A.1 Provide new power arrangements to reduce noise sensitivity and simplify the circuit options.

D. Description of Changes

D.1 Added option K wiring to FS 8/1, 8/2 and 9/1 to show the program resistor net strapping and power

connections for basic processor configurations (power arrangement 10). Options P, Q, and R are rated manufacture discontinued on an after date basis and are replaced by option K, to reduce noise sensitivity and simplify the circuit.

D.2 Added CAD 56, Information Note 316 and Information Note 317 to support option K wiring and modify Information Notes 302, 303, 314, 315, FS 8/1, 8/2, CAD 54 and CAD 55 to show options P, Q and R MANUF DISC.

D.3 This reissue also covers information authorized by the following appendixes to Issue 1 of this CD.

APPENDIX	DRAWING ISSUE
1A	2A
2AC	3AC
3D	4D
4A	5A
5B	6B
6B	7B
7A	8A
8AC	9AC

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