

CIRCUIT DESCRIPTION

CD-4C119-01  
ISSUE 1  
APPENDIX 8B  
DWG ISSUE 9B  
DISTN CODE RN98

COMMON SYSTEMS  
3B20D MODEL 2 & 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS®

CHANGES

D. Description of Changes

- D.1 Added option D, to indicate changed wiring between backplane units to support the VLMM feature.
- D.2 Added option C and information note 314, to describe the use of the SSR010 wiring change.

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DEPT 55427-RWR-PCF

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CIRCUIT DESCRIPTION

CD-4019-01  
ISSUE 1  
APPENDIX 7M  
DWG ISSUE 8M  
DISTN CODE RN98

COMMON SYSTEMS  
3B20D MODEL 2 & 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS®

CHANGES

D. DESCRIPTION OF CHANGES

D.1 Added two wires per unit to Main Store, IO, and DFC Units, and to P5VDA and P5VDB nets. The added wires improve the load voltage regulation to DMAC0 and Channel 11 circuit packs in slots 080 and 084.

E. REASONS FOR CHANGE

E.1 Two wires were added to the 3B20D Main Store, IO, and DFC Unit backplane to improve +5 Volt load voltage regulation in the backplane.

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CIRCUIT DESCRIPTION

CD-4C119-01  
ISSUE 1  
APPENDIX 6AC  
DRAWING ISSUE 7AC  
DISTN CODE 7N98

COMMON SYSTEMS  
3B20D MODEL 2 & 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS<sup>TM</sup>

**CHANGES**

1. Description of Change

For the Model 2 System:

- A. Add option E to existing MC4C127A1 (TN19).
- B. Add option F which omits option E and provides the new MC4C127A1B (TN19) 16k writable micro-control store for the disk file controllers.

For the Model 3 System:

- A. Add option L which provides the new MC4C127A1B (TN19) as part of App. Fig 1, for the disk file controllers.

2. Reason for Change

Add the MC4C127A1B (TN19) circuit pack to the disk file controller to correct a B5 timeout error.

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COMMON SYSTEMS  
3B20D MODEL 2 AND MODEL 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS™

**CHANGES**

D. Description of Change

D.1 The TN3, TN5, and TN6 power switch circuit packs will be replaced with new TN3B, TN5B, and TN6B power switch circuit packs that provide additional inrush protection.

E. Reason for Change

E.1 The power switch circuit packs are changed to provide additional inrush protection, and additional protection from lightning discharge.

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COMMON SYSTEMS  
3B20D MODEL 2 & 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS™

CHANGES

D. Description of Changes

3B20D MODEL 2 PROCESSOR

D.1 Change App. Fig. 9 to provide only the Store Address Translator Circuit Pack (UN45C).

D.2 Add App. Fig. 11 that provides backplane wiring which enables circuitry on the STORE ADDRESS TRANSLATOR (UN45C) and provides the IMPROVED OPERATING SYSTEM PERFORMANCE FEATURE.

3B20D MODEL 3 PROCESSOR

D.3 Change App. Fig. 5 to provide only the Store Address Translator Circuit Pack (UN45C).

D.4 Add App. Fig. 7 that provides backplane wiring which enables circuitry on the STORE ADDRESS TRANSLATOR (UN45C) and provides the IMPROVED OPERATING SYSTEM PERFORMANCE FEATURE.

E. Reason for Change

E.1 To correct an error in a previously-released feature. The backplane wiring that enables the IMPROVED OPERATING SYSTEM PERFORMANCE FEATURE is not downward compatible to previous DMERT Generic 1 and 2 software releases.

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CIRCUIT DESCRIPTION

CD-4C119-01  
ISSUE :  
APPENDIX 3B  
DWG ISSUE 4B  
DISTN CODE 7N98

COMMON SYSTEMS  
3B20D MODEL 2 & 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS\*

**CHANGES**

D. Description of Changes

D.1 Updated feature and option table to include the FAST BACK-UP TAPE UNIT FEATURE.

D.2 Reason for change

Provided the FAST BACK-UP TAPE UNIT FEATURE associated with the 340 MB fixed media disk drives.

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DEPT 45154-JW-MPV

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CIRCUIT DESCRIPTION

CD 4C119-01  
ISSUE 1  
APPENDIX 2AC  
DRAWING ISSUE 3AC  
DISTN CODE 7N98

COMMON SYSTEMS  
3B20D MODEL 2 AND 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS™ SWITCH

CHANGES

D. DESCRIPTION OF CHANGES

D.1 This change corrects circuit pack power arrangements 5 and 6, which would not power up, by removing options N and M respectively.

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DEPT 45153-CAB-MFS

COMMON SYSTEMS  
3B20D MODEL 2 AND 3 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS™ SWITCH

**CHANGES**

D. DESCRIPTION OF CHANGES

- D.1 Provides an alarm configuration for 5ESS as summarized in notes 306, 307 and 309.
- D.2 Provides cabling documentation (option G) associated with memory expansion.
- D.3 Adds 3B20D model 3 to the feature and option table.

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DEPT 45153-CAB-MFS

COMMON SYSTEMS  
3B20D MODEL 2 PROCESSOR  
PROCESSOR CONTROL CABINET CIRCUIT  
FOR 5ESS\*SECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 The 3B20D Model 2 processor control cabinet circuit provides a housing for the unit circuits that make up the 3B20D Model 2 processor system.

2. GENERAL DESCRIPTION

2.01 Five unit circuits are available for the 3B20D Model 2 processor control frame.

2.02 The power distribution unit circuit provides fusing and distribution for -48v frame input power for the 3B20D Model 2 processor system. Information about this unit is contained in CD 4C102-01.

2.03 The central processing unit circuit provides the central control for the 3B20D Model 2 processor system. Information about this unit is contained in CD 4C098-01.

2.04 The main store, IO and DFC unit circuit provides the basic main store system, input/output system, and disk file controller system for the 3B20D Model 2 processor system. Information about this unit is contained in CD 4C099-01.

2.05 The IOP basic unit circuit provides a basic input/output processor system for the 3B20D Model 2 processor system. Information about this unit is contained in CD 4C101-01.

2.06 The Main Store and IOP growth unit circuit is an optional unit that provides growth capability for the main store memory system in the 3B20D Model 2 processor system. Information about this unit is contained in CD 4C097-01.

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SECTION II - DETAILED DESCRIPTION

None.

SECTION III - REFERENCE DATA

None.

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DEPT 45142-LEL-MWR