

4

5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH CONTROL UNIT
CIRCUIT

TABLE OF CONTENTS	PAGE
SECTION I - GENERAL DESCRIPTION . . .	1
1. PURPOSE OF CIRCUIT.	1
SECTION II - DETAILED DESCRIPTION . . .	1
1. DUPLEX DUAL SERIAL BUS SELECTOR	2
2. BUS INTERFACE CONTROLLER.	2
3. PERIPHERAL INTERFACE CONTROLLER	3
4. MICRO-CONTROL STORE	4
5. INPUT/OUTPUT MICROPROCESSOR INTERFACE.	4
SECTION III - REFERENCE DATA.	4
SECTION IV - REASON FOR REISSUE	4

(MMP), a Foundation Peripheral Controller (FPC), or a Pump Peripheral Controller (PPC). Message transfers are accomplished by a bit-slice processor called the Peripheral Interface Controller (PIC). The functions of the MSCU follow:

- (a) Performs the serial-to-parallel conversion of data received from the CP, and the parallel-to-serial conversion of data transmitted to the CP via the Duplex Dual Serial Bus Selector (DDSBS).
- (b) Provides a Bus Interface Controller (BIC) to interface the 16-bit PIC to the 32-bit DDSBS.
- (c) Provides one or two Input/Output Microprocessor Interfaces (IOMI) to interface the PIC to the MMPs, FPC, and PPC.
- (d) Controls the BIC and IOMIs to transfer data between MMPs or between the CP and MMPs.
- (e) Controls the BIC and IOMIs to transfer data between the CP and the FPC or PPC.
- (f) Performs self diagnostics resident in the Micro-Control Store (MCS).

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Message Switch Control Unit (MSCU) controls the message transfers between the AT&T 3B20 computer Central Processor (CP), and as many as eight communities -- each consisting of one to four peripheral controllers. A peripheral controller can be a Module Message Processor

NOTICE

This document is either
AT&T - Proprietary, or WESTERN
ELECTRIC - Proprietary

Pursuant to Judge Greene's Order of August 5, 1983,
beginning on January 1, 1984, AT&T will cease to use
"Bell" and the Bell symbol, with the exceptions as set
forth in that Order. Pursuant thereto, any reference to
"BELL" and/or the BELL symbol in this document is here-
by deleted and "expunged".

SECTION II - DETAILED DESCRIPTION

1. DUPLEX DUAL SERIAL BUS SELECTOR

1.01 The DDSBS interfaces the MSCU with the 3B computer Dual Serial Channel (DSCH). From one to 16 DDSBSs can be connected to a single DSCH. All signaling is compatible with EIA standard RS422. Each DDSBS interfaces with the DSCH through connectorized cables, each of which consists of two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The data rate between the DDSBS and DSCH is 10MHz.

1.02 To specify the operation type, four bit start codes are transmitted to the DDSBS over the two bidirectional data leads. The DSCH issues seven different start codes to the DDSBS:

1. Write data in the word mode
2. Send device command
3. Write data in the block mode
4. Read data in the word mode
5. Sense DDSBS status
6. Read data in the block mode
7. End of transfer (EOT).

1.03 Similarly, the DDSBS issues one of the following four start codes to the DSCH to specify the success or failure of the operation:

1. All seems well
2. Device reported an error
3. Invalid DDSBS command
4. Illegal start code received

1.04 The DDSBS receives and decodes the incoming serial message, executes the specified operation with

the BIC, and transmits the serial reply message back to the DSCH.

1.05 The DDSBS interacts with the BIC over information, control and respond leads, as follows:

Information - Thirty-six bidirectional information leads include four parity leads which are used either to send data or commands to the BIC; or, to receive data or status from the BIC.

Control - Five control signals to the BIC:

- Command Present (CP)
- Data Present (DP)
- Data Request (DR)
- Sense Status (SST)
- End of Transfer (EOT).

Response - Five response signals from the BIC:

- Sync
- Error (ER)
- Interrupt (INT)
- Transfer (XFER)
- Setup.

2. BUS INTERFACE CONTROLLER

2.01 The BIC serves as a buffer between the 32-bit DDSBS and the 16-bit PIC. The BIC includes a 16-word by 32-bit data FIFO register, a 32-bit command register, a 32-bit status register, and a 16-bit sanity timer. The PIC can access each of these registers, 16 bits at a time. The BIC buffers data and commands to the PIC,

buffers data and status from the PIC, and performs the hand shaking necessary to communicate with the DDSBS.

2.02 The FIFO may be accessed by both the PIC and DDSBS but not at the same time. Parity checks over transfers between the BIC and DDSBS are always performed by the BIC. Parity checks over transfers between the PIC and BIC may, or may not, be performed by the BIC, depending on the state of an internal flag controlled by the PIC.

2.03 The command register records commands from the CP destined for the PIC. The PIC may read and, for maintenance purposes, write this register.

2.04 The timer provided on the BIC is used to maintain the sanity of the MSCU. The PIC has read/write access to the timer, which is incremented once every 5 microseconds. A timer interrupt is issued to the PIC every 100 ms. The PIC has 30 ms to reset the timer or a sanity error bit will be set to report the detection of an error to the 3B20 computer.

2.05 The BIC flags are segmented into 16 bits for status and 16 bits for errors. The flags are used to request interrupt and direct memory access (DMA) service from the 3B20 computer, to alert the PIC of the presence of a 3B20 command or data requests, and to record the detection of error conditions.

3. PERIPHERAL INTERFACE CONTROLLER

3.01 The central processing unit for the PIC is made up of four, 4-bit-slice processors. The bit-slices work together to form a very fast 16-bit processor.

3.02 The microprogram register provides a data latch for the MCS programmable read-only store (PROM) output. This register contains all

control information required to execute a signal microinstruction.

3.03 The source and destination register decoders decode 5 bits of the microprogram register into the appropriate register input and output enable signals.

3.04 The special overlay buffer is provided on the PIC as a diagnostic aid to allow the user to generate invalid or special combinations of bit patterns to test hardware components.

3.05 The arithmetic logic unit (ALU) comprises four 4-bit sliced microprocessors that form a 16-bit microprocessor. The ALU can perform addition, two forms of subtraction, and five logical operations.

3.06 A 4K by 16+2 parity bit random access memory (RAM) is equipped on the PIC and is used as temporary data storage. Associated with the RAM is a 12-bit address sequencer that provides a four-level stack onto which an interim address is pushed and popped.

3.07 Eight vectored interrupt levels are incorporated by priority on the PIC. A 7-bit mask register is included to block individually selected levels. The MSCU interrupt assignments are shown below:

- LEVEL 1 MCS parity error
- LEVEL 2 PIC instruction timer
- LEVEL 3 BIC command flag, alerts the PIC that a command from the 3B20 computer is present and awaiting execution.
- LEVEL 4 spare and not connected
- LEVEL 5 IOMI-A PC interrupt request summary
- LEVEL 6 IOMI-B PC interrupt request summary
- LEVEL 7 BIC sanity timer.

3.08 The microprogram address sequencer provides full control capability to perform normal sequential execution up to 64K of MCS. The sequencer also performs conditional and unconditional jumps for the following six conditions:

- 1) carry
- 2) overflow
- 3) negative
- 4) zero
- 5) BIC data flag
- 6) BIC error summary.

4. MICRO-CONTROL STORE

4.01 The MSCU may contain one or two MCS circuit packs, each with 8K by 40-bits. Bits 0-31 are used by the PIC. Bits 32-35 are used by the MCS to determine the instruction execution speed of every microinstruction. Instruction speeds may vary from 100 ns to 300 ns in increments of 50 ns. Bits 36-39 are used by the MCS to calculate parity over the 40-bit word.

5. INPUT/OUTPUT MICROPROCESSOR INTERFACE

5.01 The IOMI interfaces the 16-bit PIC with one to four communities

of four 8-bit peripheral processors. The MSCU can equip two IOMIs for a maximum of eight communities. Selection of the IOMI by the PIC is accomplished by data bus bits 0 and 1.

5.02 All signals between the IOMI and the MSPUs are at TTL levels. Each community consists of a 16-bit DMA address bus, an 8+1 parity bit bidirectional data bus, eight control signals, and one out-of-level signal. Each of the four peripheral processors in each community has an individual service, interrupt, error, service request, and control signal acknowledge signals.

5.03 The interface between the PIC and IOMI consists of a 16+2 parity bit data bus, five source signals, and five destination signals for control of the IOMI.

SECTION III - REFERENCE DATA

1.01 See the individual circuit pack CDs.

SECTION IV - REASON FOR REISSUE

1.01 Replaced the 496A power converter with the 495FB module 3 in all units to reduce EMI affecting the converter.

AT&T BELL LABORATORIES

DEPT 55617-KTK-RFM