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## SESS™ SWITCHING EQUIPMENT

DIGITAL SERVICE UNIT  
CIRCUITB. Changes in Apparatus

B.1 No change in apparatus.

D. Description of Changes

D.1 Added TN853, Revertive Pulsing Transceiver (RVPT), and TN1032, 6-port Conference Circuit Packs to the DSU.

F. Changes in CD Sections

F.1 Changed SECTION II, 1.02, last sentence to read: ... - the TN130 tone decoder, TN132 tone generator, and TN234 and TN1032 conference circuits.

F.2 Changed SECTION II, 2.07, second sentence to read: Voice bridging capability for 3- and 6-party conferencing is provided.

F.3 Added CD for TN1032: CONFERENCE CIRCUIT - TN1032

7.85 The TN1032 conference circuit is identical to the TN234 conference circuit, with the following exceptions:

1. The TN1032 operates with a clock speed of 8MHz, instead of 4MHz, to allow conferencing of six ports instead of three.
2. The TN1032 functions as a conference circuit only; the TN234, along with the conferencing feature, also performs "busy" line verification."

3. Because the TN1032 conferences six ports, the time slot assignment differs from that of the TN234. The time slot assignment format for the TN1032 is shown in Figure 16.

S. Revertive Pulsing Transceiver - TN853

7.86 Revertive pulsing transceiver (RVPT) circuit packs are located in the local DSU, where they perform the SESS™ revertive pulse transmitting and receiving functions required for call processing. Each TN853 can handle incoming or outgoing pulsing on up to 32 time slots simultaneously.

The RVPT receives 4-MHz clock, 8-KHz frame sync, 32 time slots of data, and control information from the DSUCOM. Data and control return information from the RVPT is sent to the DSUCOM for reply to the MCU/TSIU, as are RVPT faults, parity errors, and summary scan interrupts.

T. DSUCOM-TN853 Interface

7.87 The TN853 transmits and receives all signals to and from the DSUCOM, which functions as the interface between the MCU/TSIU and the service circuits. The signals between the DSUCOM and the TN853 are shown in Figure 17 and include clock, sync, data, control channel signals, and interrupt signals. The incoming data signal transmits the A and B bit samples to the TN853; the control

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channel lines permit reading and writing of the RVPTs source and destination registers; and the interrupt leads transmit fault indicators and service requests to the DSUCOM.

7.88 Three data signals are sent from the DSUCOM to the RVPT: a 4.096-Mb/s serial data bus, a 4.096-MHz clock, and an 8-KHz sync line. The data line presents the RVPT with 32 time slots of data, each of which is 16 bits long. The first 8 bits of each time slot contain the u255 PCM sample; the last eight contain the A through D signaling bits, E, F, and G bits, and an odd parity bit. The 4.096-MHz clock line is buffered and directed to the clock inputs of all the flip-flops and is also buffered and directed to the delayed sync generator. The delayed sync generator generates delayed 8-KHz sync pulses that are used to initialize circuit counters in the time slot select register (TSSR), the clock generator, the parity generator, and the parity checker. One data signal is sent from the RVPT to the DSUCOM. This line presents the DSUCOM with 32 time slots of data having the same format as that in the DSUCOM to RVPT direction.

7.89 The control channel lines allow software to read and write the numerous source and destination registers of the RVPT. Control words are transmitted and received on separate bus lines at a 2.048-Mb/s rate. These reads and writes occur asynchronously with respect to the 4.096-Mb/s data bus, 8-KHz sync, and 4.096-MHz clock. The DSUCOM generates address by simultaneously activating one of two possible B address signals and one of eight possible A address signals. Additional signals involved in each control channel operation include a 2.048-MHz data shift clock, a read select lead, and a write select lead. The control channel expects an acknowledgment pulse on one of two all seems well (ASW) leads for every control channel operation.

7.90 Three interrupt lines transmit RVPT interrupts back to the DSUCOM. The first, the parity error interrupt signal, generates an interrupt pulse whenever an incoming time slot parity error has been detected. The second, the fault interrupt signal, generates a latched interrupt level whenever an error is detected by the RVPTs fault detection circuitry. The third, the summary scan interrupt signal, generates a latched service request interrupt whenever a time slot requires attention. The summary scan interrupt and the fault interrupt are latched on the RVPT, and they remain present until cleared by control channel write operations.

#### U. RVPT Hardware and Operation

7.91 The revertive pulse transceiver (RVPT) hardware is divided into two groups: functional and maintenance. The functional group is the circuitry that performs the actual revertive pulse transmitting and receiving. The maintenance group is additional circuitry that performs monitoring and checking and permits software access to exercise the RVPT hardware.

#### V. Maintenance

7.92 Each DSC, including the RVPT, has a maintenance register and an identification loop-back register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out-of-service LAMP; another is looped back to the identification loop-back register for control channel verification. The identification loop-back register, when read, returns the looped bit and a 7-bit RVPT identification code. Each DSC type has a unique code. Seven bits of the maintenance register are used to set specific summary scan register bits.

W. Parity Checker

7.93 The parity checker monitors the incoming 4.096-MHz data bus and checks for odd parity over the 16 bits in each time slot. If a time slot parity error (even parity) occurs, the corresponding bit of an internal 32-bit latch is set. Also, a parity check error pulse is generated to the DSUCOM on the parity error interrupt line. Two time slot select register bits allow per-time-slot mask control over parity interrupts and parity error bit setting in the 32-bit latch. The 32-bit register can be read and cleared by the control channel.

X. Fault Interrupt Register

7.94 The fault interrupt register monitors seven internal board error lines. Each line can cause a fault interrupt to the DSUCOM. The interrupt signal generated is a latched level. Each interrupt input, when active, sets an internal latch. The latch outputs are ORed together so that any of the seven inputs can generate an interrupt out of the gate array. The latch outputs into the OR circuits can be masked individually to ignore undesired inputs. The latches can be read, cleared, and the per-line mask enabled by control channel writes. Two retriggerable, monostable multivibrators monitor the incoming 4.096-MHz clock and the 8K sync lines. If either signal is missing or intermittent, the monostables send active low-error signals to the fault interrupt register inputs. The sanity check is a timer that must be updated continually by the RVPT firmware to prevent it from expiring. If the timer does expire, an active low-error signal (SANITYE) is sent to the fault interrupt register. The parity check/gen block generates parity on any write to RAM and checks parity on any read from EPROM or RAM. If this parity check fails, an active low-error signal (DBUSPE) is sent to the fault interrupt register. Other fault lines monitor a

TSSR parity error output, the parity checker 8-KHz sync-loss output, and the parity generator 8-KHz sync loss output.

Y. Functional Description

7.95 Figure 18 shows a functional diagram of the RVPT. Timing and synchronization signals required for operation of the RVPT are derived from the the 4MHZCKN and the 8KSYN signals, which are inputs from the DSUCOM. The delayed sync generator supplies 8K sync pulses that have been delayed by the amounts required for proper synchronization to the clock generator, the parity checker, the parity generator, and the time slot select register. The clock generator supplies the clock signals required by the A-B Bit input register, the A-B output register, the DMA controller, the timer, and the microprocessor complex. These are shown in Figure 18 as CK2M, ICKAB, ILDAB, OCKAB, OLDAB, and OENAB. CK2M provides the clock for the timer, the DMA controller, and the microprocessor complex. ICKAB and ILDAB shift and load the A-B bits into the A-B Bit input register. OLDAB, OCKAB, and OENAB load, shift, and enable the A-B bits in the A-B output register.

7.96 Proper operation of the RVPT is determined by control signals that are received from the module control unit (MCU) via the DSUCOM. The control buffer and driver circuitry serves as the distribution point for these signals shown as CIN in Figure 18. These signals are inputs to the clear generate register, fault interrupt register, maintenance register, loop register, summary scan register, I/O address register, I/O data register, parity generator, TSSR, and the parity checker.

7.97 Control signals perform either a write or a read from a register. At the end of a write or read command to a register in the RVPT, an all seems

well pulse (ASW in Figure 18) is returned to the MCU via the DSUCOM. This signal indicates only that a write or read was performed by the associated register. When a read command is sent to a particular register, the register will clock out the data that exists at its input. This data appears on the DTRD lead and is sent to the MCU via the DSUCOM at a 2.048-MHz rate.

7.98 The microprocessor must execute its reset routine any time initialization of the RVPT is required. RESET enables this function. This reset pulse is provided by the clear generate register. This register produces a single pulse output in the desired bit position when addressed. The state of this register need not be remembered because the register automatically clears after each write. The clear generate register also is used to clear the parity fault registers in the parity checker, the fault interrupt register, and the summary scan register.

7.99 The TSSR gate array and a 38A random access memory operate together as a per-time-slot controller. The TSSR has eight output control bits that are available to enable and disable per-time-slot RVPT functions. The 38A stores eight bits of control data for each of the 32 time slots. These 32, 8-bit words are sequentially displayed at the control outputs, and the pattern is repeated every 125  $\mu$ s. The TSSR allows the contents of 38A's to be written and read asynchronously through the control channel without affecting the synchronous output of the stored data.

7.100 The RVPT uses three of the TSSR's eight output control bits. Two are directed to the parity checker, where they control per-time-slot masking of the interrupt output and per-time-slot masking of parity error latching. The other bit enables time slots to the A-B Bit input register. The A and B bits are forced

to "0"s in time slots that are not enabled. Flexibility of the TSSRs permits the transceiver to receive any of the 32 incoming time slots.

7.101 Input data to the RVPT is from the time slot interchange unit (TSIU) via the DSUCOM. This input is a 4.096-MHz, 32-time-slot, 16-bits-per-time-slot, serial bit stream. The 32 time slots of data are reclocked and then used as an input to the parity checker and the A-B bit input register. Only the A and B bits are shifted into this register. The shifting is controlled by lead ICKAB, which contains transitions only during A and B bit times. This register is eight bits long, so it can hold the A and B bits for four time slots. A transition occurs on lead ILDAB every four time slots. This transition is used to transfer the A-B bits from a shift register to a latch within the A-B bit input register. Lead TSEN from the TSSR forces the A-B bits to a "0" in unused time slots.

7.102 The A-B bit output register supplies the A and B bits for the outgoing data stream. Lead OLDAB transfers a byte from a latch to a shift register in the A-B bit output register. This transfer occurs once every four time slots. Lead OCKAB shifts the A-B bits to the output at the appropriate time. Lead OENAB forces all the remaining 14 bits in each time slot to "0"s. This bit stream is presented to the parity generator, which calculates odd parity over each time slot for normal operation.

7.103 The DMA controller transfers bytes from RAM to the comparator, from the A-B bit input register to RAM, from RAM to the A-B bit output register, from the I/O data register to RAM, and from RAM to the I/O data register. When the appropriate transition occurs on lead ILDAB to latch a byte in the A-B bit input register, a request for service

is made to the DMA controller. The DMA controller responds to this request with the following actions:

1. A byte that contains the previous and hit timed values for the A-B bits that are presently in the two least significant bits of the A-B bit input register is read from RAM and presented to the comparator.
2. The hit timed value is updated if the present values of the A-B bits equal the previous values.
3. The change FIFO is written with the time slot address and the A-B bit values if the hit timed values have changed.
4. The present values and the hit timed values of the A-B bits are written to RAM.

7.104 This sequence is repeated for all four sets of A-B bits in the A-B bit input register. Then the A-B bit input register is updated, and the sequence is repeated. The process continues until all the time slots in a frame have been analyzed. This process is applied to one frame in eight to provide a scanning rate on incoming A-B bits of 1 millisecond. These bits must be equal on two successive scans before a change is written into the change FIFO.

7.105 When the appropriate transition occurs on lead OLDA to cause a transfer from the latch to shift register in the A-B output register, a request to the DMA controller is registered. The DMA controller responds with a transfer from the appropriate location in RAM to the A-B bit output register.

7.106 The I/O data and address registers, along with two channels of the DMA controller, are used to give the MCU read/write access

to the RVPTs RAM. The MCU uses this capability to communicate with the RVPT firmware. The MCU uses the I/O address register to specify a specific address to be written to or read from. The MCU then writes or reads the data word to or from the I/O data register. A write to the I/O address register initiates a request to the DMA controller and results in a transfer from the location in RAM pointed to by the I/O address register to the I/O data register. A subsequent read from the I/O data register results in the following actions:

1. Data from the I/O data register is returned to the MCU.
2. The I/O address register is incremented.
3. A request is sent to the DMA controller.
4. The DMA controller does a transfer from the location in RAM pointed to by the I/O address register to the I/O data register.

A write to the I/O data register results in the following actions:

1. A request is sent to the DMA controller.
2. The DMA controller does a transfer from the I/O data register to the location in RAM pointed to by the I/O address register.
3. The I/O address register is incremented.
4. A request is sent to the DMA controller.

5. The DMA controller does a transfer from the location in RAM pointed to by the I/O address register to the I/O data register.

7.107 The microprocessor, a WE<sup>™</sup> 8000, executes the firmware that resides in the EPROM to perform the functions necessary to execute the revertive pulsing function. The change FIFO is read periodically to determine if any incoming A-B bits have changed. The timer is used for hit timing on incoming A-B bits and to produce a 10-millisecond base cycle interrupt. When the microprocessor has written to RAM the information that it wants to pass to the MCU, it sets the appropriate bit in the summary scan register. This action generates a summary scan interrupt to the MCU. After the MCU has serviced this interrupt, it clears the summary scan register.

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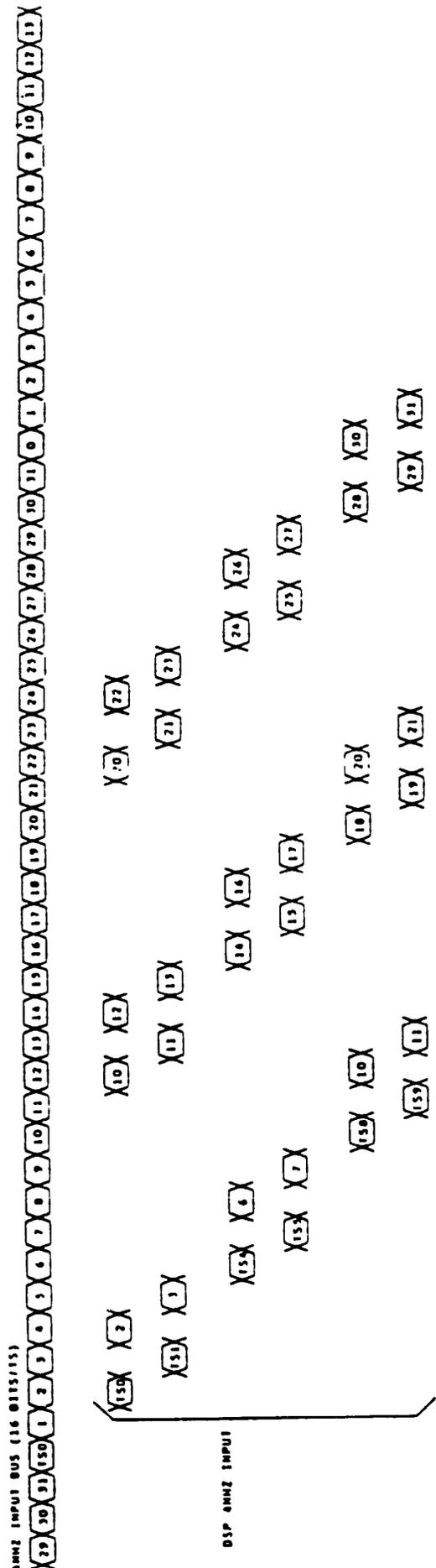
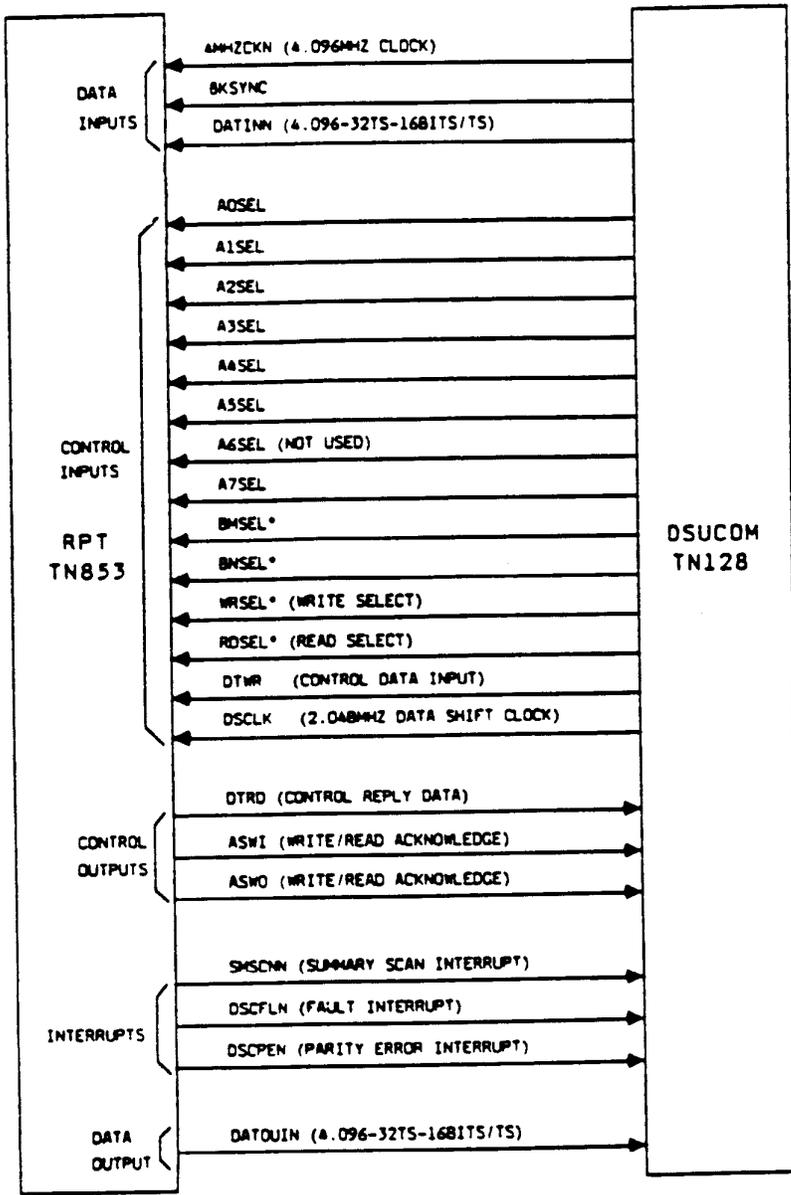


FIGURE 16 TIME SLOT ASSIGNMENT FORMAT FOR CONFERENCE CIRCUIT PACK 1M1032

IN WITHDRAWN



\*THESE SIGNALS ARE SLOT POSITION DEPENDENT

FIGURE 17 DSUCOM - RPT INTERFACE

IHL50196A02



5ESS™ SWITCHING EQUIPMENT  
DIGITAL SERVICE UNIT  
CIRCUIT

CHANGES

D. Description of Changes

D.1 This revised pack TN304B provides approximately 40% faster Electronic Loop Segregation (ELS). Use of the TN304B is office size and traffic driven. TN304B is the revised TTF measuring-responder pack.

F. Changes in CD Section

F.1 In Section II. 2.09 add the following: Two different TN304s exist: TN304 and TN304B. TN304B provides certain features for larger offices (see Appendix L1). Equipage depends on office engineering. TN304B must be used in conjunction with TN305 microcode MC-5D214A1 to achieve the new features.

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SESS™ SWITCHING EQUIPMENT  
DIGITAL SERVICE UNIT  
CIRCUIT

CHANGES

D. Description of Changes

D.1 The microcode for TN305 has been changed from MC5D003A1 to MC5D214A1 to meet original design intent and to provide one enhancement. The TN305 is the TTP CPU circuit pack. The new microcode for TN305 is required to allow multiple responder boards (TN304/TN304B) in the TTF, and to provide 40% faster Electronic Loop Segregation (ELS). Both are required for larger offices. The new microcode is also required to provide Touch-Tone Test Line (TTTL) that was part of the original design intent.

F. Changes in CD Section

F.1 In Section II, 2.09 add the following: A new TN305 microcode exists in the TTF that is required for use with the new TN304B. See Appendix J.1. Equipage depends on office engineering.

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DEPT 55614-CEJ-MJK

CIRCUIT DESCRIPTION

CD-5D035-01  
ISSUE 1  
APPENDIX 2AC  
DWG ISSUE 3AC  
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT  
DIGITAL SERVICE UNIT  
CIRCUIT

CHANGES

D. Description of Changes

D.1 The information showing how to set switch S1 on TN304/TN304B for each of the three possible positions. TN304/TN304B is the Global Digital Service Unit (GDSU) TTF measuring circuit pack.

D.2 Fusing information on this unit is also included.

D.3 The information concerning the replacement of the Universal Tone Generator (UTG) and Decoder with the new version 2 type of each pack. TN892 replaces the TN132 as UTG for this unit. TN133 replaces the TN130 as UTD for this unit. TN341 version 2 of the TN234 supplements, rather than replaces, the TN234.

F. Changes in CD Section

F.1 In Section II, change all occurrences of TN132 to TN132/TN892. Change all occurrences of UTG to UTG/UTG2.

F.2 In Section II, 7.34 through 7.57 change comments about EPROM/ROM and other comments about memory to reflect those differences between the TN132 CD and the TN892 CD.

F.3 In Section II, change all occurrences of TN130 to TN130/TN133. Change all occurrences of UTD to UTD/UTD2.

F.4 In Section II, 7.20 through 7.33 change comments about 2 decoders per board, and other model related comments to reflect those differences between the TN130 CD and the TN133 CD.

F.5 In Section II, change all occurrences of TN234 to TN234/TN841. Change all occurrences of UCC to UCC/UCC2.

F.6 In Section II, 7.58 through 7.84 add circuit notes to the text on TN234 to change and add material on the TN841.

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ELECTRONIC SWITCHING SYSTEMS  
NO. 5  
DIGITAL SERVICE UNIT  
CIRCUIT

## CHANGES

D. Description of Changes

- D.1 Replaced power converter unit 495A with 495FB, on a line-out basis.
- D.2 Added fuse information, which was omitted in Issue 1, to Circuit Note 101.
- D.3 Added Equipment Note 212 to define the switch positions for each of the three TN304 circuit packs.
- D.4 Added circuit packs TN133, TN892, and TN841 to the apparatus index, FS2 - Symbols 1 through 8, FS5 - Symbols 1 through 8, and App Figs. 4, 5, and 6 to complete circuit board complement lists for option Y.
- D.5 Changed feature and option table (Information Note 302) and Information Notes 303, 304, 306 and 307; and added 308 and 309 to show option Z and add option Y.
- D.6 Added Information Note 310 to define options Z and Y.
- D.7 Changed Information Note 304 to reflect current CLEI status.
- D.8 Added circuit pack TN128 to correct Information Note 307.

F. Changes in CD Sections

- F.1 Section II, 6.01 - Change paragraph to read:

6.01 The DSU communicates control information to and from the interface module processor unit (IMPU) via the peripheral interface control bus (PICB). Each service group provides a duplex PICB interface to the duplicated IMPU. A duplex to simplex interface conversion is performed at the interface by decoding a select lead on each bus whereby the DSU listens to only the active side of the IMPU. Reply messages are sent to both IMPU halves. The interrupt signal to the IMPU, however, is sent only to the active IMPU half.

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F.2 Section II, 6.03 - Change the third sentence to read:

Each service group contains a -48V to +5V BELLPAC power converter (coded 495A, 495FB, or 495G) which supplies +5V power to the entire service group with a maximum rating of 108 usable watts (12 watts per circuit pack).

F.3 Section II, 7.02 - Change the first four sentences to read:

7.02 The DSU Common circuit pack (DSUCOM) serves primarily as the interface between the duplex IMPU/TSIU and the simplex digital service circuits (DSCs). The DSUCOM, coded TN128, performs the required duplex <-> simplex conversion on the data and control buses from the IMPU/TSIU, typically listening on the active bus and replying on both. The DSUCOM distributes the 4 MHz clock, 8KHz frame sync, 32 time slots of data, and control information to all DSCs. The DSUCOM multiplexes data and control return information from the DSCs for reply to the IMPU/TSIU.

F.4 Section II, 7.03 - Change the first two sentences to read:

7.03 The DSUCOM control interface to the IMPU/TSIU is the peripheral interface control bus (PICB). The DSUCOM receives a simplex PICB from each interface module processor unit (IMPU) half as shown in Figure 2.

F.5 Section II, 7.05 - Change the first sentence to read:

7.05 The DSUCOM data interface to the IMPU/TSIU is via the peripheral interface data bus (PIDB) for a Global DSU and via the local DSU bus (LDSUB) for a Local DSU.

F.6 Section II, 7.13 - Change the second sentence to read:

If a parity error is detected on any time slot, a bit corresponding to the time slot number is set in a 32-bit error source register, and an interrupt is sent back to the active IMPU.

F.7 Section II, 7.19 - Change the second sentence to read:

The output from the summary scan register is sent to the active IMPU/TSIU via an opto-isolator.

F.8 Section II, 7.22 - Change the first sentence to read:

7.22 The TN130 transmits and receives all signals to and from the DSUCOM which functions as the interface between the IMPU/TSIU and the service circuits.

F.9 Section II, 7.37 - Change the first sentence to read:

7.37 Proper operation of the UTG is determined by control signals (CONTROL IN on Figure 12) that are received from the interface module processor unit (IMPU) via the DSUCOM.

F.10 Section II, 7.38 - Change the second sentence to read:

At the end of a write or read command to a register in the UTG, an all-seems-well pulse (ASW in Figure 12) is returned to the IMPU via the DSUCOM.

F.11 Section II, 7.64 - Change the second sentence to read:

Control signals are received from the interface module processor unit (IMPU) via the DSUCOM.

F.12 Section II, 7.65 - Change the second sentence to read:

At the end of a write or read command to a register in the CC, an all seems well pulse (ASW in Figure 14) is returned to the IMPU via the DSUCOM.

F.13 Section II, 7.65 - Change the last sentence to read:

This data appears on the DTRD lead and is sent to the IMPU via the DSUCOM at a 2.048 MHz rate.

F.14 Section II, Figure 1 and Figure 2 - Change the names of the following blocks:

MCU 0, MCU 1 to IMPU 0, IMPU 1, respectively.

F.15 Section II, Figure 3 - Change the following references at the inputs and outputs of the block diagram:

MCU 0, MCU 1 to IMPU 0, IMPU 1, respectively.

F.16 Section II, Figure 7 - Change the following references at the outputs of the block diagram:

MCU 0, MCU 1 to IMPU 0, IMPU 1, respectively

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The digital service unit (DSU) provides No. 5 ESS with the functions of tone decoding, tone generation, conferencing, and certain AC tests. Each DSU consists of two independent service groups to provide partial service availability in the presence of a single hardware failure. Each service group provides up to 32 time slots of service features and consists of one common circuit pack and up to eight service circuit boards. Both service groups share a single 2-foot, 2-inch wide equipment shelf.

The current No. 5 ESS system architecture designates two types of DSUs - a local DSU and a global DSU. They differ only in the

equipage of the optional service circuit boards, and their position in the No. 5 ESS network architecture. The local DSU is module dedicated, ie, each local DSU serves a single interface module. It provides the high usage functions of tone generation and tone decoding for its associated interface module (IM). The local DSU connects to the IM via the local digital service unit bus (LDSUB), and does not use any of the 512 internal time slots in the IM. The global DSU can be shared by all modules in the No. 5 ESS office and is accessed via the switching network. It provides low usage functions, such as conferencing and transmission testing. Global DSUs connect to the IM via the peripheral interface data bus (PIDB) and are engineered over the entire office as needed. Both the local and global DSUs communicate control information to the IM via the peripheral interface control bus (PICB).

SECTION II - DETAILED DESCRIPTION

1. INTRODUCTION

1.01 The Digital Service Unit is a No. 5 ESS peripheral which provides the No. 5 ESS with tone decoding, tone generation, conferencing, AC testing, and other appropriate functions. The No. 5 ESS system architecture requires two types of DSUs - a local DSU and a global DSU. A flexible hardware architecture for the DSU was developed so that a common hardware framework with optional plug-in circuits could serve as either a local or global DSU.

1.02 This design specification first addresses the high-level functional and interface requirements of the DSU. Subsequent sections describe the implementation details of the DSU, beginning with its internal architecture, then with the DSU common circuit (TN128), interface requirements for all service circuit plug-ins, and then with a description of the existing service circuits - the TN130 tone decoder, TN132 tone generator, and TN234 conference circuit.

2. DSU REQUIREMENTS

OPERATIONAL REQUIREMENTS

2.01 The DSU is required to provide the following functions in No. 5 ESS:

- (a) Tone Decoding
- (b) Tone Generation
- (c) Conferencing
- (d) Transmission Testing

2.02 In addition to the above, the architecture of the DSU must be flexible to allow for the addition of new service functions in later No. 5 ESS generics as these services become available for DSU inclusion.

A. Tone Decoding

2.03 The DSU provides the tone recognition functions required by No. 5 ESS call processing. The following tone types must be recognized by the DSU:

- (a) TOUCH-TONE\* Signals (16 tone pairs)
- (b) Multifrequency Signals (15 tone pairs)

2.04 When performing the tone decoding function for the above classes of tones, the DSU must meet the frequency, amplitude, and timing requirements established for tone decoders of each respective signaling type as specified in

the local switching system specifications (LSSS).

B. Tone Generation

2.05 The DSU must be capable of generating the following tones required by No. 5 ESS:

- (a) Call Progress Tones - audible ring
  - dial tone
  - high tone
  - low tone
  - call waiting
  - preemption
- (b) Multifrequency Signals (15 tone pairs), TOUCH-TONE Signals (16 tone pairs), and CCIS Continuity Check Tones (1780 and 2010 Hz)

2.06 All tones generated by the DSU must meet the amplitude and frequency requirements specified in the LSSS. The DSU must supply enough different tones at any given time to satisfy the load requirements placed on it by a fully equipped IM. The fanout of a given tone to multiple destinations is performed by the time slot interchange (TSI) circuit in the interface module (IM). The TSI also supplies cadence or other special timing functions for those tones which require such features, i.e. busy tone, audible ring, etc.

C. Conferencing

2.07 The DSU provides conference calling features for No. 5 ESS. Voice bridging capability for only three party conferencing is provided. Three party conference calling is used as a customer service, for busy line verification, and for certain switch maintenance functions.

2.08 For the special case of busy line verification, the DSU also performs the required interchange of the A, B, C, and D signaling bits for the three parties involved in the call.

D. Transmission Test Function

2.09 The DSU provides a transmission test function (TTF) which performs all voice band transmission tests required in a No. 5 ESS office. These include facility testing and CODEC testing, in addition to noise, loss, and frequency response measurements. Test lines provided for the SE1 generic include:

- (a) 100 Test Line
- (b) 102 Test Line
- (c) 105 Test Line
- (d) Remote Office Test Line (ROTL)
- (e) TOUCH-TONE Test Line

A separate development specification has been issued for the TTF.[1]

\* A registered service mark of AT&T.

3. MAINTENANCE REQUIREMENTS

3.01 The following is a list of general maintenance objectives which govern the design of the DSU as well as other maintainable No. 5 ESS units:

- (a) The maintenance philosophy of the DSU is consistent with the maintenance philosophy of No. 5 ESS.
- (b) The DSU must contain sufficient redundancy so that no single DSU failure results in complete loss of DSU service.
- (c) The DSU must contain circuits with sufficient error detection capability which use both self-checking circuits and software initiated per call tests, such that undetected failures in the DSU do not result in a grade of service which exceeds the reliability requirements for call failures in No. 5 ESS.
- (d) Conservative design, which prevents intermittent or marginal operation of the unit from occurring, is followed in the DSU.
- (e) The design of the DSU must be modularly partitioned, such that the ability of the diagnostic programs to resolve faults meets the No. 5 ESS maintenance requirements.
- (f) All DSU circuit packs which contain EPROM devices are compatible with the version C of the prompt remotely operated memory updating system (PRONUS-C). The PRONUS-C system is a BELLFAC compatible piece of equipment which allows the erasure and programming of EPROM contents while the devices remain intact on the circuit packs.

4. DSU DESIGN IMPLEMENTATION

4.01 The No. 5 ESS architecture identifies two types of DSUs: a local DSU and a global DSU. The local and global DSUs differ primarily in the types of service functions performed by each and their positions in the No. 5 ESS network architecture.

LOCAL DSU

4.02 The local DSU provides the heavily used functions of tone generation and tone decoding for No. 5 ESS. Each interface module is equipped with a single local DSU, and that local DSU is dedicated, providing tone generation and tone decoding only for lines and trunks terminating on that interface module. Tone generation and tone decoding are segregated from the rest of the DSU functions. Distributing these functions to each module, rather than providing them in a centralized pool shared by all modules greatly reduces the amount of intermodule message traffic, since these services are heavily used in call processing.

4.03 The local DSU is connected to the local digital service unit bus (LDSUB) of the TSI and receives time slot data from the alternate data ram in the TSI. Access to the local DSU is gained by creating TSI paths from peripheral side time slots into the alternate data ram. The 64 time slots used by the local DSU are not part of the 512 TSI time slots, and thus the appearance of a local DSU on each IM does not reduce the switching capacity of the TSI.

GLOBAL DSU

4.04 The global DSU provides conferencing, transmission testing, and other low runner services which can be developed in the future. Global DSUs, because they provide low usage service functions, are not module dedicated, but are shared by all modules in the No. 5 ESS office. The global DSU is attached to the TSI via the peripheral interface data bus (PIDB) in a manner identical to all other TSI peripheral units (line unit, trunk unit, etc.). Access to the global DSU is obtained via the TSI/TMS switching network. The 64 time slots used by the global DSU are part of the 512 TSI time slots, and thus the termination capability of the network is reduced by that amount with the addition of each global DSU.

5. DSU ARCHITECTURE

5.01 The architecture of the DSU is shown in Figure 1. It consists of two independent service groups to provide redundancy and service availability. Each service group accesses 32 time slots from the TSI and consists of the DSU common board (DSUCOM) and up to eight digital service circuit (DSC) plug-ins. Both the local and global DSUs exhibit this architecture. Their hardware differs only with the equipage of different types of DSCs.

5.02 Proper engineering of the DSCs in each DSU service group is important to ensure adequate reliability for each service. In the local DSU, the service groups must be engineered with one tone generator circuit, and identical complements of tone decoder circuits. This ensures that under any single failure condition in the DSU (loss of one service group at most), a maximum of only half of each service is lost. This allows call processing to continue in the IM, resulting in only a degraded form of service (50 percent of peak capacity).

5.03 Service circuit engineering on the global DSUs is much less critical, but must follow the guidelines listed below to obtain optimum service availability:

- (a) In an office with only one global DSU, services must be split between the two service groups for reasons explained in the previous paragraph.
- (b) For the case of multiple global DSUs, service circuits of each type must be distributed as evenly as

possible between global DSUs to provide service availability in the presence of duplex failures (i.e., both DSU service groups fail or a duplex IM failure).

6. EXTERNAL INTERFACES

A. Control Interface

6.01 The DSU communicates control information to and from the module control unit (MCU) via the peripheral interface control bus (PICB). Each service group provides a duplex PICB interface to the duplicated MCU. A duplex to simplex interface conversion is performed at the interface by decoding a select lead on each bus such that the DSU listens to only the active side of the MCU. Reply messages are sent to both MCU halves. The interrupt signal to the MCU, however, is sent only to the active MCU half.

B. Data Interface

6.02 The DSU communicates data information to and from the time slot interchange unit (TSIU). The data interface to the Local DSU is the local DSU Bus (LDSUB) and to the global DSU is the peripheral interface data bus (PIDB). In either case, the buses are electrically identical, consisting of four differential balanced TTL signals: a 4 MHz clock, an 8 KHz frame synchronization pulse, and a 32 time slot serial data stream in each direction. As with the PICB, this bus is presented in duplicate to each DSU service group (one from each half of the TSI). A peripheral control channel (PCC) writable bit selects the active bus to listen to, but the 32 time slot data bus to the TSI is returned to both TSI halves.

C. Power Interface

6.03 Each DSU service group is powered from the -48V battery plant. DSU service group 0 and DSU service group 1 each receive -48V from separate battery feeds. Each service group contains a -48V to +5V BELLPAK power converter (coded F60894) which supplies +5V power to the entire service group with a maximum rating of 108 usable watts (12 watts per circuit pack). Current programming resistors located on each DSU circuit pack determine the output current limitations of the power converter. The value of each current programming resistor is calculated using the circuit pack current requirements as follows:

$$R(\text{Kohms}) = 10 / (I_{19} \pm I_{19} \text{ MAX})$$

The power converter will shut down should the total service group current drain exceed the total specified by the sum total of current programming resistors.

6.04 It is required that DSU circuit packs can be inserted or removed from a powered-up DSU without causing converter shut down. As indicated above, the power converter shuts down, if the total service

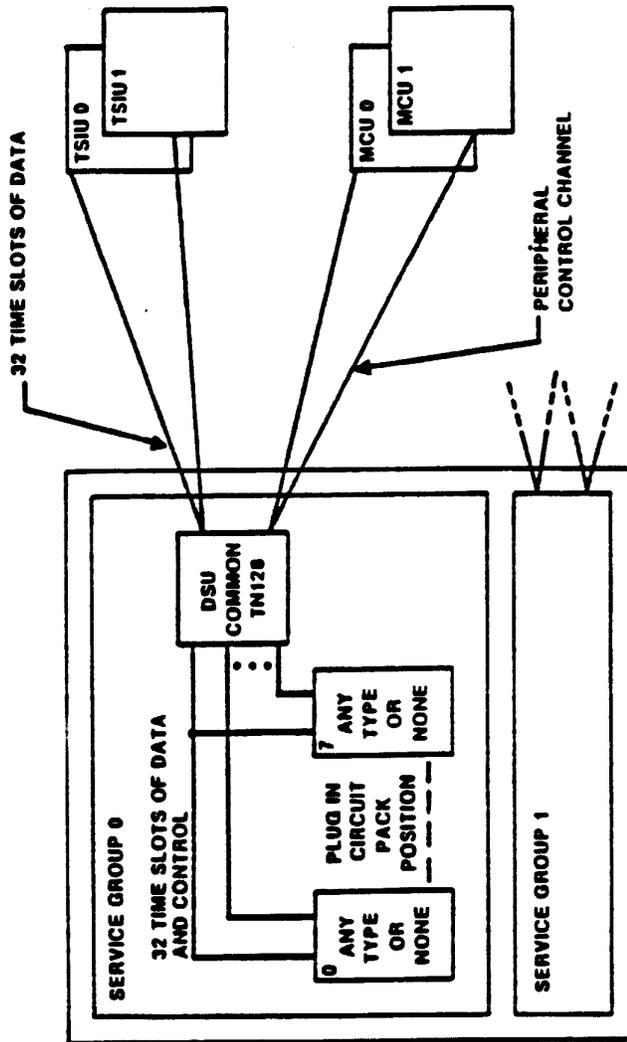
group current drain exceeds the total specified by the sum total of the current programming resistors. Exceeding the specified current can occur momentarily when a circuit pack is inserted into a powered-up DSU, if the current programming resistor pins on the circuit pack do not engage with the backplane pins before the +5V power pins and ground pins. Also, upon insertion, the circuit pack +5V bus capacitance causes a surge current which in turn causes a transient on the backplane +5V bus. In order to restrict the overdraw current to a level that is compatible with the time delay requirements for converter shut down and to reduce the transient on the backplane +5V bus, the following design will be implemented.

6.05 First, each circuit pack position excluding the power converter and the TM128 (DSUCOM) are equipped with seven long (0.75 inch) backplane pins. The converter and the TM128 are not to be pulled in the powered up position. When a circuit pack is inserted into the DSU, these seven pins engage the circuit pack connector before the normal length pins. Four of the pins are connected to ground. Two pins are associated with the circuit pack programming resistor. The last pin is +5 volts. The circuit pack connector pin associated with this +5V backplane pin has a high inductance, low resistance choke connected between it and the circuit pack +5V bus. When a circuit pack is inserted into a powered up DSU, the programming resistor, ground, and +5 volts (single pin with the choke in series) make contact first. The programming resistor adjusts the converter for the expected circuit pack current drain and the choke restricts the surge current to reduce the transient on the backplane +5V bus. The overall current is restricted to a level which does not exceed the converter shut down requirements. When the circuit pack is fully inserted, the remaining power and ground connections are made and the pack functions in a normal fashion. Removing a circuit pack from a powered-up DSU does not cause a problem in regards to converter shut down, nor is it detrimental to the circuit pack. An additional power converter requirement is that the equivalent series resistance of the converter output filter be low enough to accommodate power surges under worst case conditions.

7. DSU CIRCUIT PACKS

7.01 In subsequent sections of this document, reference is made to five commonly used DSU gate array devices. These LSI devices are designed to save board area and reduce power consumption, both of which are necessary to provide a flexible DSU architecture having one service circuit per board. The five gate arrays are listed below:

- (a) Delayed Synchronization Generator
- (b) Interrupt Register



Digital Service Unit Architecture

Figure 1

11-100015

11-4

- (c) Parity Generator
- (d) Parity Checker
- (e) Time Slot Select Register

## DSU COMMON - TN128

7.02 The DSU Common circuit pack (DSUCOM) serves primarily as the interface between the duplex MCU/TSIU and the simplex digital service circuits (DSCs). The DSUCOM, coded TN128, performs the required duplex (-) simplex conversion on the data and control buses from the MCU/TSIU, typically listening on the active bus and replying on both. The DSUCOM distributes the 4 MHz clock, 8 KHz frame sync, 32 time slots of data, and control information to all DSCs. The DSUCOM multiplexes data and control return information from the DSCs for reply to the MCU/TSIU. In addition, the DSUCOM contains interrupt registers with each DSCs parity error, and summary scan interrupt status. Partial equipage of DSCs is allowable because the DSUCOM uses a pecking strategy and writable control memories to ignore unused DSC positions.

## A. Control Interface

7.03 The DSUCOM control interface to the MCU/TSIU is the peripheral interface control bus (PICB). The DSUCOM receives a simplex PICB from each module control unit (MCU) half as shown in Figure 2. Each PICB consists of clock (CLK), data in (DI), data out (DO), controller select (CSEL), and interrupt request (INTREQ) as shown. Clock, data in, and data out are balanced differentially driven twisted pair signals. Clock and data in are terminated with a 220 ohm shunt resistance. Controller select and interrupt request also use twisted pairs and are opto-isolated. The controller select leads enable the DSUCOM to select one of the PICBs as the active bus. If both select leads contain the same logical value, PICB0 is selected as the active bus; if their values differ, then PICB1 is selected.

7.04 As shown in Figure 3, the clock (CLK) and data in (DI) from the selected bus are sent to a peripheral sequencer gate array (WE code 241AA), through a line receiver. The input clock (2.048 MHz) is also monitored by a retriggerable monostable multivibrator with a typical pulse width of 800 nanoseconds to provide a reset to the peripheral sequencer between control messages. The peripheral sequencer checks the serial input message for correct format and outputs data shift clock (DSCKOUT) and serial message data signals (DWOUT) which are buffered for use on the DSUCOM and separately buffered to the backplane for use by the DSCs. In conjunction with three decoder gate arrays (WE code 41JU), the 241AA produces a 24-bit parallel peripheral address from the 9-bit serial address contained in the input message. Refer to Figure 4. This is done by doing a 3-to-8 decoding function on the input message address bits 3-5, 6-8, and 9-11 to produce three groups of eight address bits each as shown. Like the data

shift clock and serial message data signals, the 24 address bits are then buffered twice - once to supply address information to the DSCs and once for addressing the scan and distribute gate arrays on the DSUCOM. The 512 address spectrum of the PICB is divided among the eight DSC positions and the DSUCOM as shown in Figure 4. Each DSC is allotted 16 read and 16 write addresses, with the absolute address dependent upon the DSU slot position number. The DSUCOM is allotted the remainder of the address space (128 write and 128 read addresses).

## B. Data

7.05 The DSUCOM data interface to the MCU/TSIU is via the peripheral interface data bus (PIDB) for a Global DSU and via the local DSU bus (LDSUB) for a Local DSU. The buses are electrically identical and as shown in Figure 5, each consists of a 4 MHz input clock, and 8 KHz frame synchronization pulse and a 32 time slot (16 bits/time slot) serial data bus as inputs, and a 32 time slot serial data bus output. During this discussion only the PIDB is referenced.

7.06 All inputs and outputs on the PIDB are balanced differentially driven twisted pair signals. Incoming signals are terminated with a 220 ohm shunt resistance. The DSUCOM selects the active PIDB by a control channel writable bit. For the following discussion, refer to Figure 6.

7.07 The 4 MHz input clock (4MCO) and the 8 KHz synchronization pulse (8KCO) are buffered and fanned out separately to each DSC position and internally to the remainder of the DSUCOM. The 8 KHz sync is reclocked and thus delayed by one full clock cycle (244 ns). A 16-bit destination register controls inhibit circuitry which permits the 4 MHz clock and/or 8 KHz syncs to be selectively disabled to any DSC for diagnostic purposes.

7.08 The DSUCOM checks parity on each time slot of the incoming data bus. The sense of the incoming parity (even or odd) on each time slot is returned to the TSI on the same time slot during the following frame. This parity loop around feature is useful in maintaining both directions of the data bus on the PIDB, since the TSI periodically walks even parity through the time slots on each PIDB and checks for even parity on the same time slot of the returning data bus. This walking parity is used with global DSUs only.

7.09 The incoming data bus is fanned out separately to each DSC after being reclocked and regenerating parity on each time slot. This results in a 3 clock cycle (732 ns) delay from input to output. A 32-bit register, located in the parity generator gate array, is writable via the FCC, and is used to select even or odd parity to be regenerated on each time slot. Each bit in the register controls the parity selection for its respective time slot. Parity is regenerated so that incoming parity errors on the PIDB do not

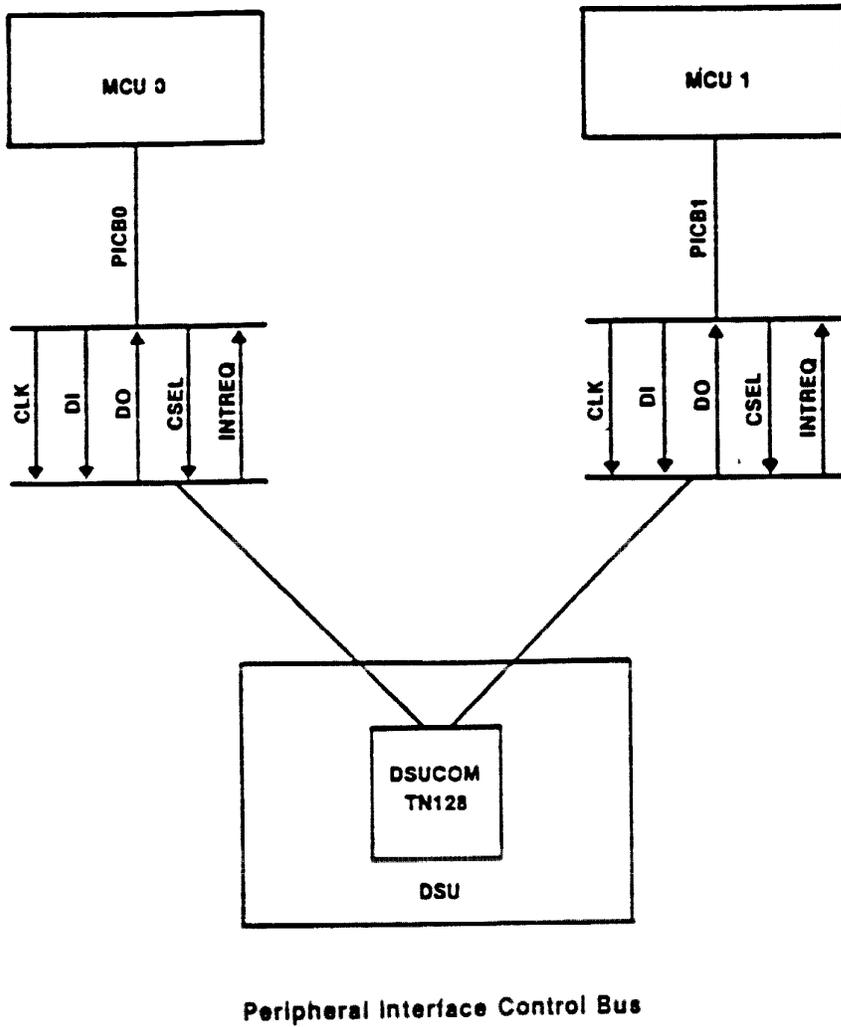
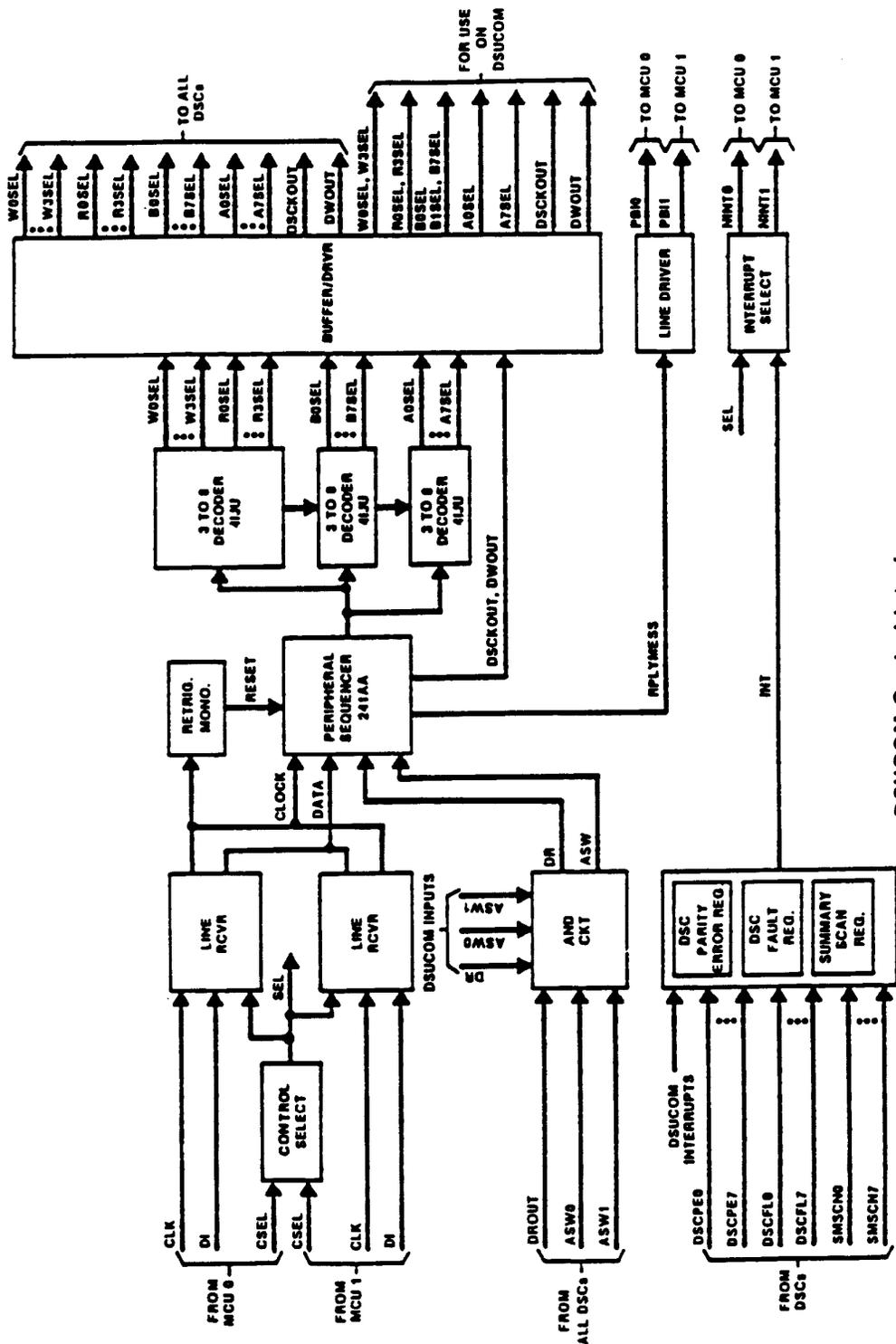


Figure 2

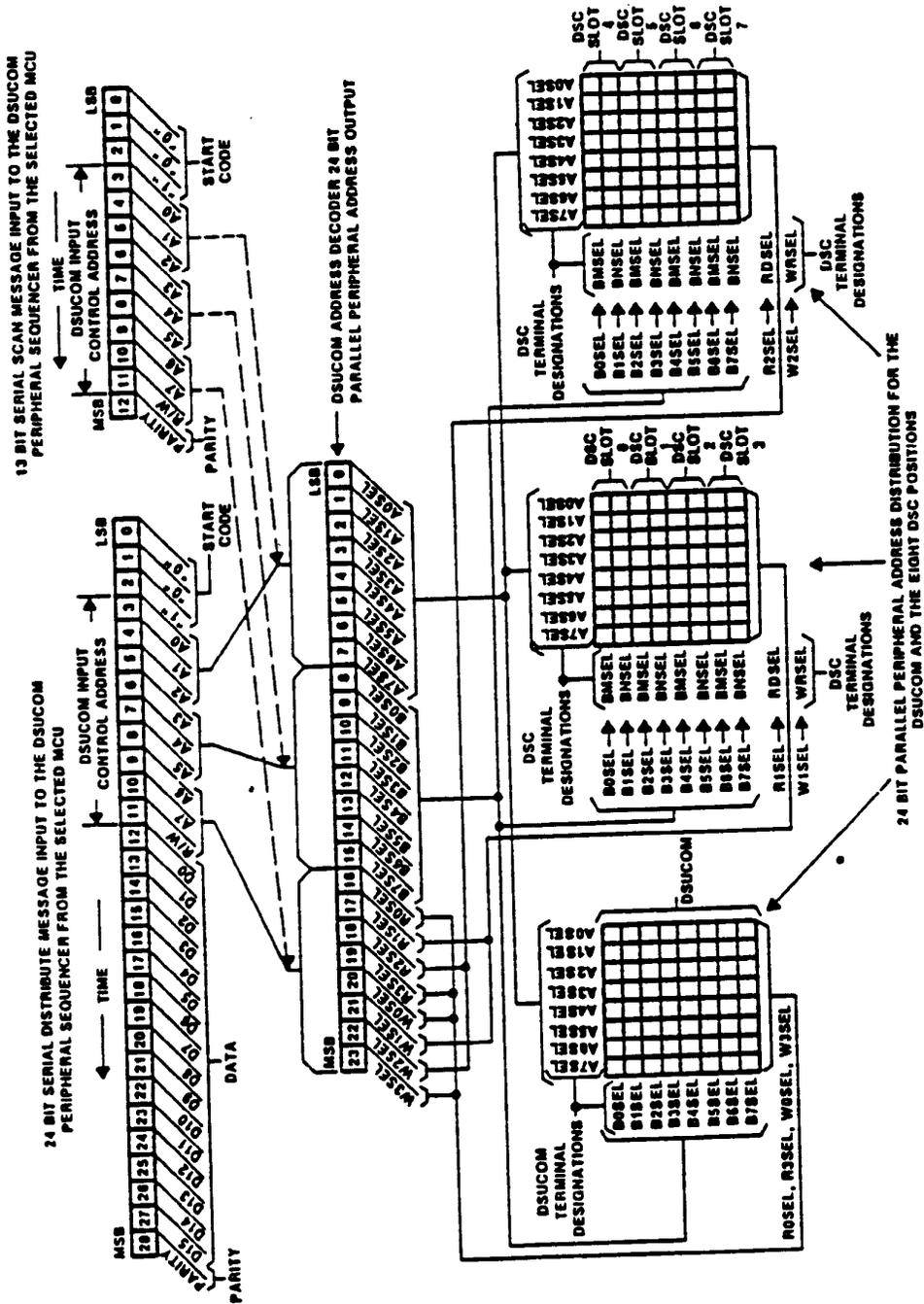
M14180014



DSUCOM Control Interface

Figure 3

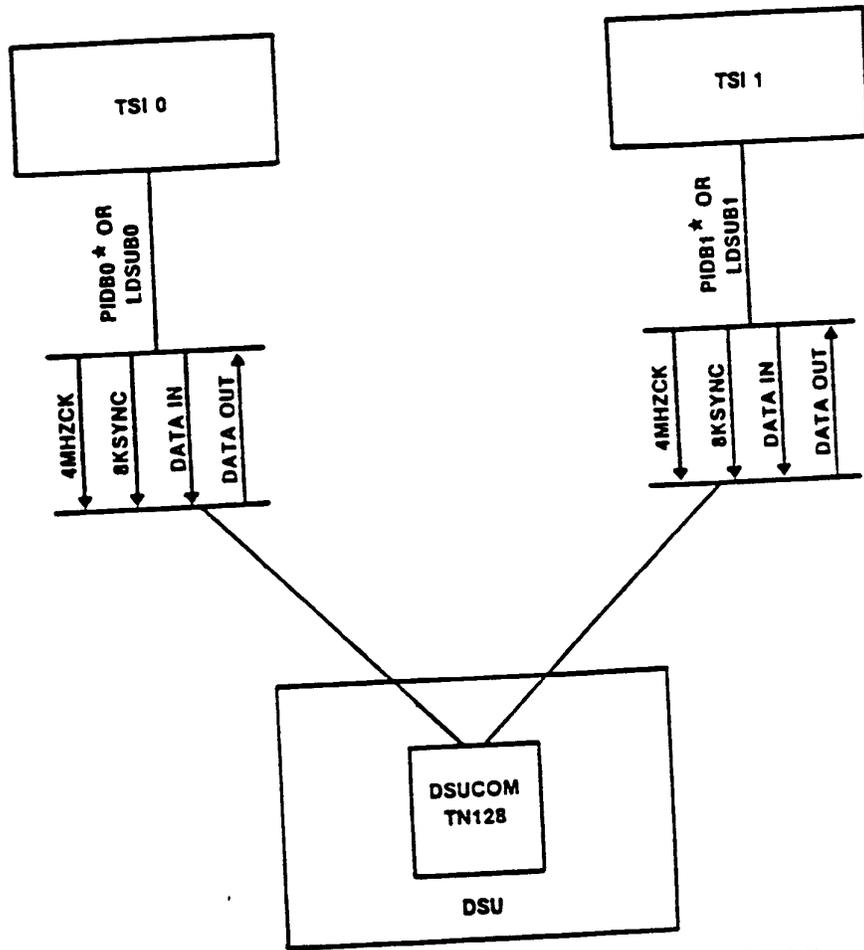
M14180013



DSU Control Address

Figure 4

M14180012



★ PIDB IS ASSOCIATED WITH A GLOBAL DSU AND LDSUB IS ASSOCIATED WITH A LOCAL DSU. ELECTRICALLY BOTH BUSSES ARE THE SAME.

Peripheral Interface Data Bus

Figure 5

M141800011



propagate to the DSCs. The ability to generate even or odd parity with per time slot control is useful as a maintenance feature.

7.10 The time slot select register gate array (TSSR) is a per time slot controller which is used in conjunction with a 38A memory to produce eight control outputs for every 3.906 usec time slot. The 38A is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC with the TSSR operating as a memory controller. The TSSR autonomously reads the 38A memory once per time slot to fetch the eight control bits for the following time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906 usec time slot and are held valid for the remainder of the time slot to provide control functions on a per time slot basis.

7.11 The DSUCOM has the capability to receive a 32-time slot serial data bus from each of the eight DSCs. During each time slot, the DSUCOM selects one of the eight DSCs as the source for data transmitted to the TSI and using an 8 to 1 multiplexer circuit routes the 16 data bits from the selected DSC to a parity check circuit through a 2-to-1 multiplexer. A pullup resistor to +5V is attached to all eight inputs to the 8 to 1 multiplexer so that the inputs from unequipped DSC positions are a constant logic one (bad parity). DSCs which do not transmit data to the DSUCOM must ground their data out lead so the DSUCOM input is a constant logic zero (also bad parity).

7.12 For diagnostic purposes, the DSUCOM has an internal data loopback which allows the 32 time slot data bus normally transmitted to the DSCs to be selected as return data. This is done in the 2-to-1 multiplexer which follows the 8-to-1 DSC multiplexer. The control leads to both multiplexers are supplied by the TSSR, so that during any time slot, any of the eight DSCs or the internal loopback can be selected for data transmitted to the TSI. The internal loopback, due to circuit timing, inserts a three time slot offset in the looped back data stream, i.e., if loopback is selected in the DSUCOM for time slot N, the data which is looped back to the TSI is that data which the TSI sent to the DSUCOM in time slot N-3. The circuitry required to exactly align the loopback time slot data is an additional 304-bit shift register, which was judged too costly to implement. Since the loopback feature is used only in the diagnostic, the slip translations are compensated for in software.

7.13 The 32-time slot serial output of the multiplexer circuits is then checked for parity errors on each time slot as well as having parity regenerated for all time slots, so that parity errors do not propagate to the TSIs. Should a parity error be detected on any time slot, a bit corresponding to the time slot number is

set in a 32-bit error source register, as well as an interrupt sent back to the active MCU/TSIU. Also, it is at this point where the input parity sense (even or odd) for each time slot from the TSI is inserted into the outgoing time slots for transmission to the TSI. Two TSSR control bits, an error mask bit, and interrupt mask bit inhibit errors and interrupts respectively, on a per time slot basis, so that parity errors on unused or out-of-service time slots can be ignored.

7.14 The 32-time slot serial output from the parity check gate array is reclocked, buffered, and then transmitted on both FIDBs, with balanced differential TTL bus drivers.

### C. Interrupts

7.15 The interrupt structure on the DSUCOM is shown in Figure 7. Three separate interrupt registers are contained on the TN128: the DSC fault register, the DSC parity error register, and the DSC summary scan register. A logic zero level on interrupt inputs to each of the interrupt registers sets a corresponding latch to hold the interrupt. The interrupt latches are readable and clearable on each register via the PCC. Should any of the latches contain an interrupt (be set), an interrupt output lead from the interrupt register goes low. The contribution of each latch to the output interrupt can be inhibited by setting the corresponding bit in an interrupt mask register.

7.16 The 8-bit DSC fault register contains an input from each of the eight DSCs which indicates if that DSC detected an internal failure. A low-level on a lead sets the corresponding bit in the fault register.

7.17 The 8-bit DSC parity error register contains an input from each DSC which indicates if that DSC detected a parity error. An active low level on a lead indicates that a parity error is detected and sets the corresponding bit in the parity error register.

7.18 The summary scan register contains a lead from each DSC which goes low when the DSC initiates some type of service request (i.e., a tone decoder has a digit in its buffer ready for unloading). Pullup resistors to +5 volts are provided on all interrupt register inputs supplied by the DSCs, so if a DSC position is unequipped, the interrupt input is in the noninterrupting state.

7.19 The remaining eight inputs to the summary scan register contain the interrupt outputs of the DSC fault register, DSC parity error register, DSUCOM internal failure indicators, and one spare. The output from the summary scan register is sent to the active MCU/TSIU via an opto-isolator.

## UNIVERSAL TONE DECODER - TN130

7.20 Universal tone decoder (UTD) circuit packs are located in the local DSU where they perform the No. 5 ESS tone decoding functions required for call processing. Each TN130 contains two independent tone decoders which can be configured to decode either TOUCH-TONE or multifrequency (MF) tones. The decoding of CCIS continuity check tones is not a 5E1 feature, but can be added for the 5E2 generic.

7.21 The following sections describe the TN130 architecture and operation.

## D. DSUCOM-TN130 Interface

7.22 The TN130 transmits and receives all signals to and from the DSUCOM which functions as the interface between the MCU/TSIU and the service circuits. The signals between the DSUCOM and the TN130 are shown in Figure 8 and include clock, sync, data, control channel signals, and interrupt signals. The incoming data signal transmits the tone samples to the TN130, the control channel lines permit reading and writing of the UTD's source and destination registers, and the interrupt leads transmit fault indicators and service requests to the DSUCOM.

7.23 Three data signals are sent from the DSUCOM to the UTD: a 4.096 Mb/s serial data bus, a 4.096 MHz clock, and an 8 KHz Sync line. The data line presents the UTD with 32 time slots of data. Each time slot is 16 bits in length. The first eight bits of each time slot contain the u255 PCM sample, while the last eight contain the A through D signaling bits. E, F, and G bits and an odd parity bit. The 4.096 MHz clock line is buffered and directed to the clock inputs of all the flip-flops and is also buffered and directed to two delayed sync generator gate arrays. These gate arrays generate delayed 8 KHz Sync pulses which are used to initialize circuit counters in the time slot select register (TSSR) and the parity check gate array.

7.24 The control channel lines allow software to read and write the numerous source and destination registers of the UTD. Control words are transmitted and received on separate bus lines at a 2.048 Mb/s rate. These reads and writes occur asynchronously with respect to the 4.096 Mb/s data bus, 8 KHz Sync, and 4.096 MHz clock. The DSUCOM generates addresses by simultaneously activating 1 of 2 possible B address signals and 1 of 8 possible A address signals. Additional signals involved in each control channel operation include a 2.048 MHz data shift clock, a read select lead, and a write select lead. The control channel expects an acknowledgment pulse on one of two all seems well (ASW) leads for every control channel operation.

7.25 Three interrupt lines transmit UTD interrupts back to the DSUCOM. The first, the parity error interrupt signal,

generates an interrupt pulse whenever an incoming time slot parity error has been detected. The second, the fault interrupt signal, generates a latched interrupt level whenever an error is detected by the UTD's fault detection circuitry. The third, the summary scan interrupt signal, generates a latched service request interrupt whenever a decoder requires attention. The summary scan interrupt and the fault interrupt are latched, and remain present until they are cleared by control channel write operations.

## E. UTD Hardware and Operation

7.26 The UTD's hardware is divided into two groups: a functional group and a maintenance group. The functional group is the circuitry which performs the actual tone decoding on the UTD. The maintenance group is additional circuitry which performs monitoring and checking and permits software access to exercise the UTD hardware.

## F. Maintenance

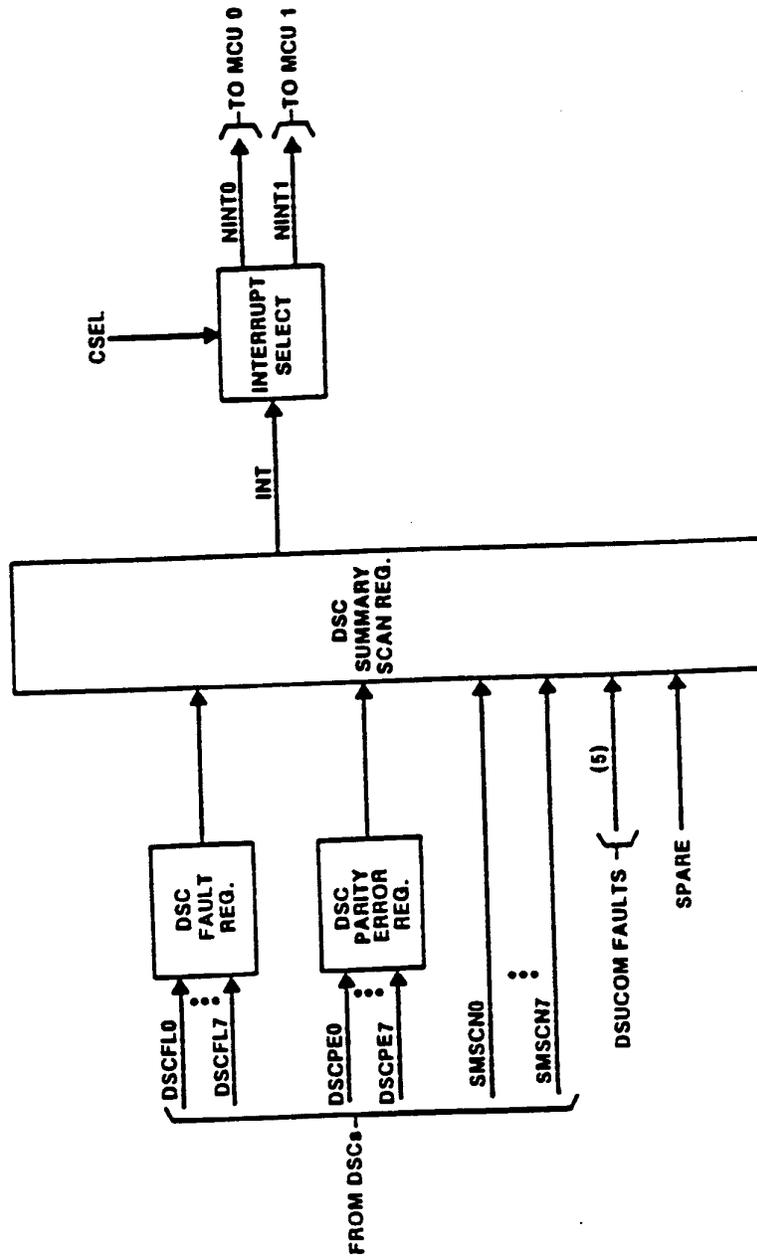
7.27 Each DSC, including the UTD, has a maintenance register and an identification-loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also one bit controls the out-of-service lamp and another is looped back to the identification-loopback register for control channel verification. The identification loop-back register, when read, returns the looped bit and a seven bit UTD identification code. Each DSC has a unique code.

## G. Parity Check Gate Array

7.28 The parity check gate array monitors the incoming 4.096 MHz data bus. It checks for odd parity over the 16 bits in each time slot. If a time slot parity error (even parity) occurs, the corresponding bit of an internal 32-bit latch is set. Also a parity check error pulse is generated to the DSUCOM on the parity error interrupt line. Two time slot select register bits allow per time slot control over parity interrupt masking and masking of bit setting in the 32-bit latch. The 32-bit register can be read and cleared by the control channel.

## H. Fault Interrupt Gate Array

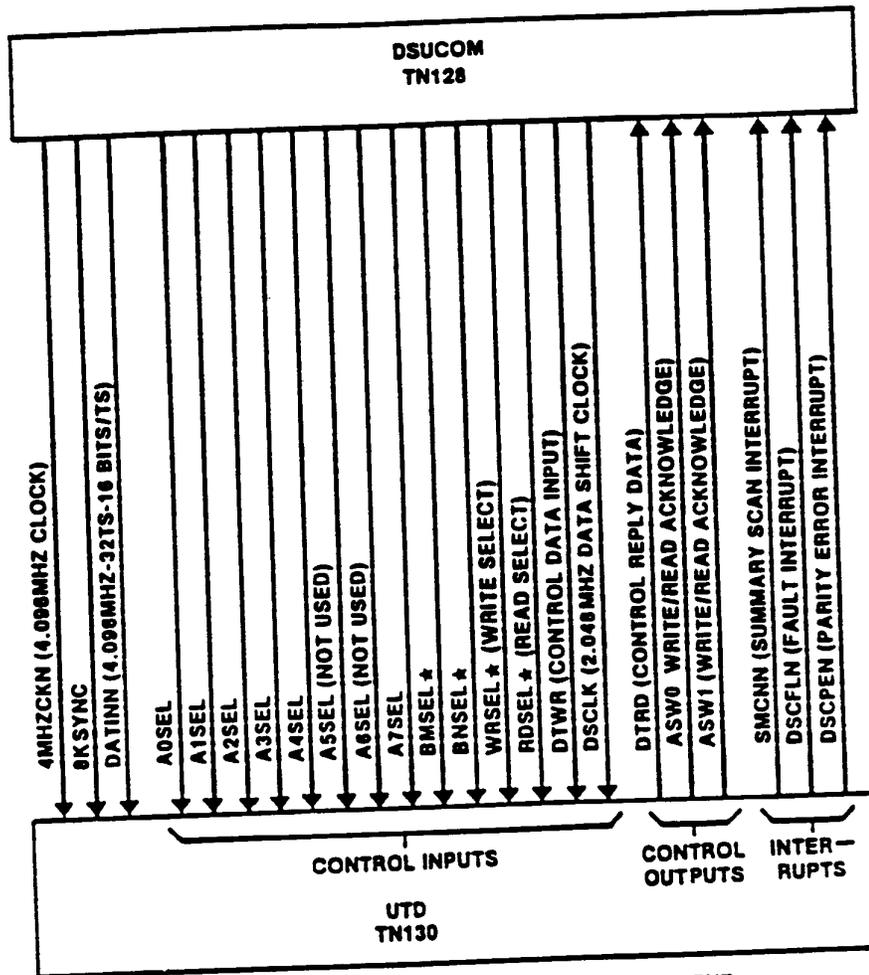
7.29 The fault interrupt gate array monitors four board error fault lines. Each line can cause a fault interrupt to the DSUCOM. The interrupt signal generated is a latched level. Each interrupt input when active sets an internal latch. The latch outputs are ORed together so that any of the four inputs can generate an interrupt out of the gate array. The latch outputs into the OR circuits can be masked individually to ignore undesired inputs. The latches can be read, cleared, and the per line mask enabled by control channel writes. Two



DSUCOM Interrupt Architecture

Figure 7

M14180009



\* THESE SIGNALS ARE SLOT POSITION DEPENDENT.

DSUCOM-UTD Interface

M14180008

Figure 8

retriggerable monostable multivibrators monitor the incoming 4.096 MHz clock and the SK sync lines. If either signal is missing or intermittent, the monostables send active low error signals to the fault interrupt register inputs. Other fault lines monitor a TSSR parity error output, and the parity checker 8 KHz sync loss output.

#### I. Functional Description

7.30 Figure 9 shows a functional diagram of the UTD. The incoming data stream is buffered through a flip-flop and proceeds into the Parity Check Gate Array and to the two decoder circuits.

7.31 The time slot select register (TSSR) gate array and a 38A random access memory serve together to function as a per time slot controller. The TSSR has eight output control bits which are available to enable and disable per time slot UTD functions. The 38A stores 8 bits of control data for each of the 32 time slots. These 32 8-bit words are synchronously outputted to the control outputs and are repeated to the outputs every 125 usec. The TSSR allows the 38A's contents to be written and read asynchronously through the control channel without affecting the synchronous output of the stored data.

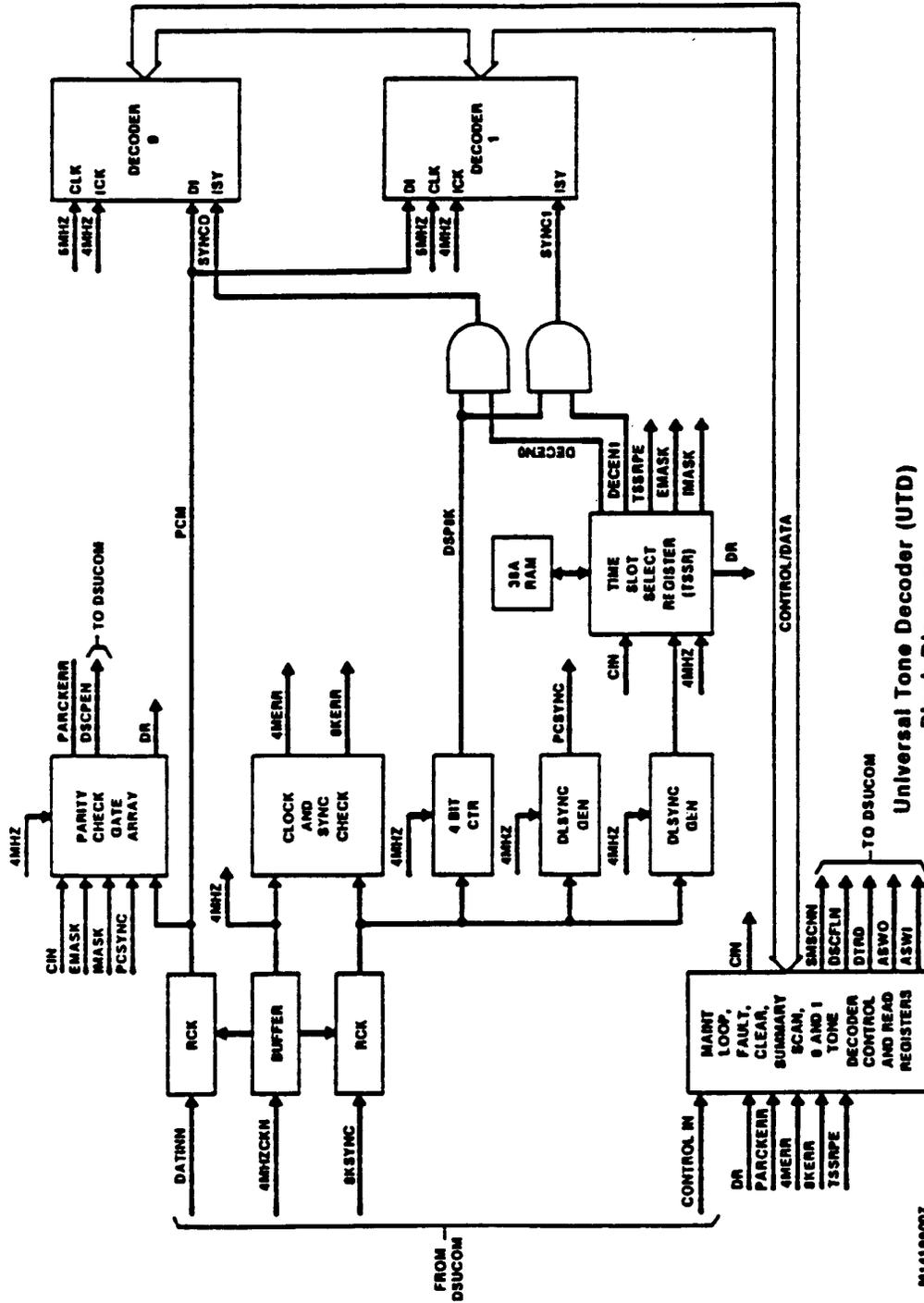
7.32 The UTD uses four of the TSSR's eight output control bits. Two are directed to the parity check gate array, where they control per time slot masking of the interrupt output and per time slot masking of parity error latching. The other two bits each enable a tone decoder circuit. When enabled, the decoder uses the next 8 PCM bits as inputs. During normal decoding operation, a decoder reads only one time slot's PCM bits per frame. The TSSR's flexibility permits a decoder to receive any of the 32 incoming time slots. Figure 10 displays the architecture of a decoder section. The block has two major components, the digital signal processor (DSP) and an 8748 microcomputer. The DSP is a programmable digital signal processor device packaged in a 40-pin DIP. It is a specialized microcomputer optimized to perform signal processing oriented functions, and in this application is programmed to perform digital filtering on the incoming PCM bits. The 8748 is an 8-bit single chip microcomputer which performs digit timing and verification. The two work together to perform the complete tone decoding function. Both are initialized simultaneously through the control channel to choose the mode configuration (TOUCH-TONE reception, multifrequency, etc.). Each mode selects a different operating program in the DSP and 8748. The DSP firmware is stored in an external EPROM memory circuit which can be replaced by internal ROM storage when the DSP firmware becomes more stable. The 8748 firmware is stored in an internal EPROM. Planned operating modes include TT and MF.

7.33 Each DSP, when receiving sync from the TSSR, reads 8 PCM bits every frame, and performs digital filtering on the incoming PCM samples. The algorithms, stored in EPROM, contain the filter coefficients, threshold detectors, and encoding routines which are required for the DSP to perform the different filtering functions. During operation, the DSP provides an 8-bit output response when requested by the 8748. This response represents the results of the digital filtering, with the 8-bit code indicating which frequencies are present at the input. The DSP's serial output is converted to a parallel word and made available to the 8748 to read. The 8748 performs the tone validation and digit timing analysis using the DSP's output response. When a valid tone or tone combination is recognized, a 4-bit encoding of the tone combination is generated and stored in a first-in-first-out (FIFO) firmware controlled buffer inside the 8748. Refer to Figure 11. The first stored digit is placed at the 8748 output ports, readable via the control channel. Subsequently, decoded digits are stored in sequential FIFO buffer locations. The FIFO is programmed to store a maximum of 16 digits per call. Peripheral software is informed of the digit storage by a summary scan interrupt. This interrupt is initiated by the digit present interrupt (DPI) of the 8748. This signal remains active as long as digits remain in the buffer. Two control channel operations alter the buffer status. First, the buffer pointer can be incremented. This operation shifts the buffer's contents so that the previously decoded digit is lost and the next stored digit is shifted to the 8748 output ports. Second, another control channel write will reset both the DSP and 8748 decoder processors, initializing them to the selected mode and clearing the FIFO buffer completely. Interrupt responses from the decoder circuit are sent to the summary scan interrupt register which generates a summary scan interrupt response to the DSUCOM.

#### UNIVERSAL TONE GENERATOR - TN132

7.34 The universal tone generator service circuit provides up to 48 different tones on any or all of the 32 time slots in the DSU service group. The tones are generated using read only memory (ROM) to store the digital samples (mu 255 PCM) of each tone. Eight hundred samples of each tone are stored in ROM to provide tone generation with frequencies possible at 10Hz intervals. Thus, all frequencies generated are within  $\pm 5$ Hz of specification.

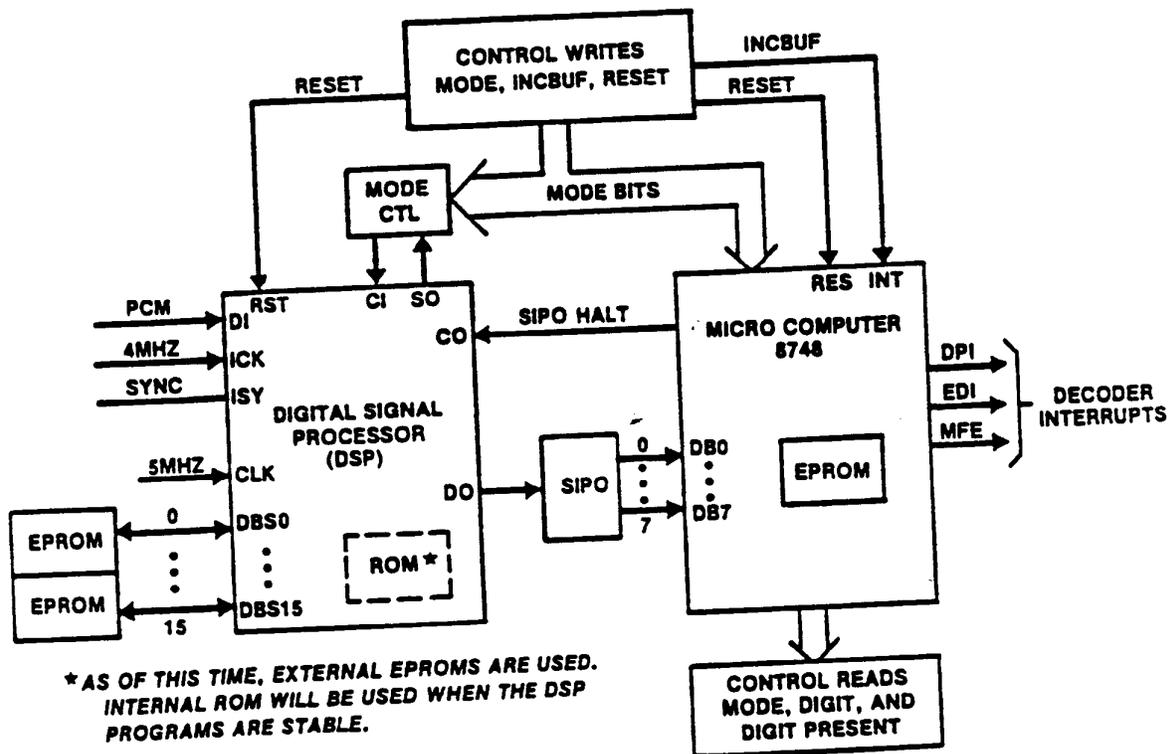
Early versions of the TN132 are restricted to 32 tones because of the use of 32K bit EPROMs instead of 64K bit ROMs. Final versions of the board use a combination of ROM and EPROM (four 64K bit ROMs and four 32K bit EPROMs) to provide the full 48 tone capacity.



Universal Tone Decoder (UTD) Block Diagram

Figure 9

M14180007



UTD Decoder Architecture

Figure 10

## J. Introduction

7.35 A functional block diagram of the universal tone generator (UTG) is shown in Figure 12. This circuit can be separated into two distinct groups - a functional group and a maintenance group. The functional group is the circuitry which performs the actual tone generation on the UTG. The maintenance group is additional circuitry which performs monitoring and checking and permits software access to exercise the UTG hardware.

## K. Functional

7.36 Timing and synchronization signals required for operation of the UTG are derived from the 4 MHzCKM and the 8KSYNC signals which are inputs from the digital service unit common board (DSUCOM).

7.37 Proper operation of the UTG is determined by control signals (CONTROL IN on Figure 12) which are received from the module control unit (MCU) via the DSUCOM. The data control section serves as the distribution point for these signals shown as CIN in Figure 12. These signals are inputs to the maintenance register, loop register, clear generate register, time slot select register (TSSR), interrupt register, and parity generator gate array.

7.38 Control signals perform either a write to or a read from a register. At the end of a write or read command to a register in the UTG, an all seems well pulse (ASW in Figure 12) is returned to the MCU via the DSUCOM. This signal indicates only that a write or read is performed by the associated register. When a read command is sent to a particular register, the register clocks out the data that exists at its input. This data appears on the DTRD lead and is sent to the MCU via the DSUCOM at a 2 MHz rate.

7.39 Two 10-bit counters (address and parity) are used in the UTG. The counters count an 800 count sequence, starting at 224, incrementing to 1023, and resetting to 224 again. The address counter provides the lower 10 bits (A0 through A9) of address for the EPROMs/ROMs. The parity counter is used to check the address counter. Its outputs are used as inputs to the parity check circuit. Both counters are clocked by the 8 KHz CTRSYNC pulse. These counters can be stopped, cleared, and incremented under program control for diagnostic purposes.

7.40 The time slot select register gate array (TSSR) is a per time slot controller which is used in conjunction with a 38A memory to produce eight control outputs for every 3.906 usec time slot. The 38A is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC and DSUCOM with the TSSR operating as a memory controller. The TSSR autonomously reads the 38A memory once per time slot to fetch the eight control bits

for the following time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906 usec time slot and are held valid for the remainder of the time slot to provide control functions on a per time slot basis.

7.41 The UTG uses seven of the TSSR's eight output control bits. Three bits (A10 - A12) are used to select 1 of 8 memory address levels in the eight EPROMs/ROMs that store the digital tones. Two of these bits (A10 and A11) are also used as address leads for the two Parity Bit Store EPROMs. The third bit (A12) is used to enable the appropriate parity bit store EPROM. Three bits (A13 - A15) are used as inputs to a 3 to 8 line decoder to enable 1 of 8 EPROMs/ROMs. These three bits are also used as inputs to a 1 of 8 data selector which selects a parity bit column in the parity bit store. And, one bit (ACTTS) is used to mask data from appearing at the UTG output for unused time slots.

7.42 Eight EPROMs or ROMs are used to store the digital tones in the UTG. The circuit is wired to accept either 2732 (4K x 8) or 2564 (8K x 8) EPROMs. It also accepts 37A (8K x 8) ROMs. The prototype uses 2732s; the production version uses a combination of four 2732s and four 37As.

7.43 Each tone occupies the upper 800 contiguous bytes of memory in a 1024 byte memory block. Therefore, a 2732 EPROM stores four tones and a 37A ROM stores eight tones. Eight 2732s allow 32 tones to be stored and four 2732s and four 37As provide storage of 48 tones. Tones are stored as true sign, magnitude inverted 8-bit mu 255 code (sign bit, plus seven data bits).

7.44 Ten bits, A0 through A9, from the address counter provide the address of the stored tones. Three bits, A10 through A12, from the TSSR select tones 0 through 7 in each EPROM or ROM and the desired EPROM or ROM is enabled by the 3 to 8 line decoder which has for its control inputs three bits, A13 through A15, from the TSSR.

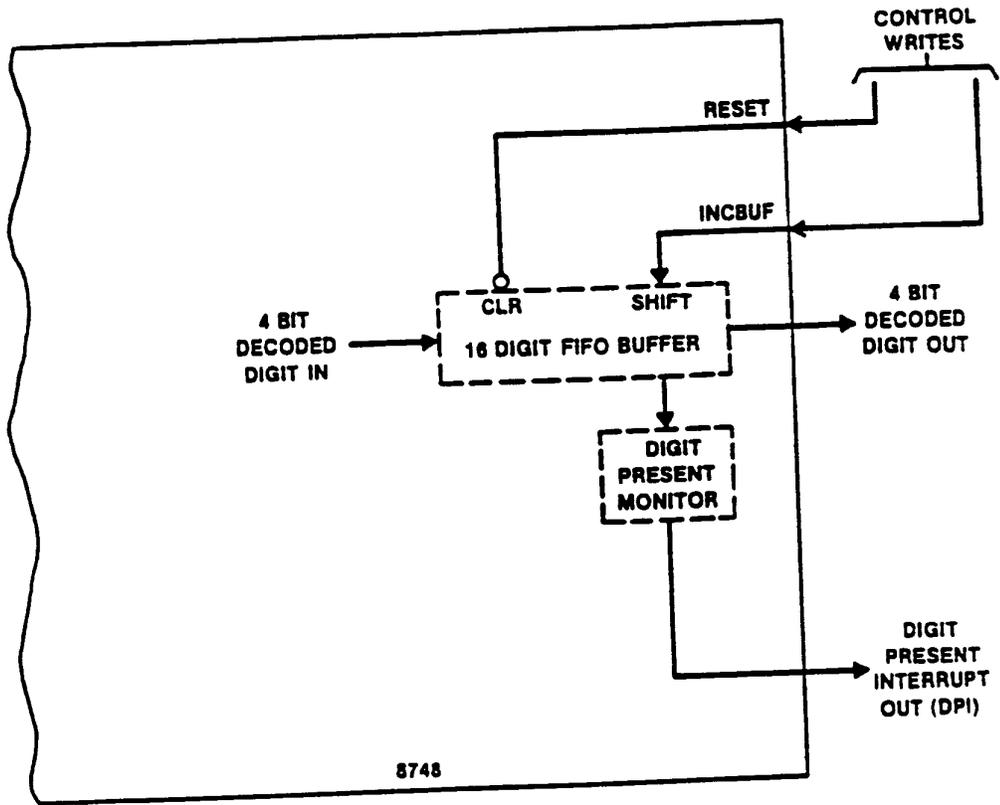
7.45 The output circuit includes the parallel input serial output register (PISO) and the parity generator.

The PISO receives the 8-bit parallel data from the EPROM/ROM parallel data bus for all time slots and converts these inputs to a 32 time slot 4 MHz, 16 bits per time slot, input for the parity generator. The time slot data format is shown below.

It should be noted that bits 0 through 7 are all 0s.

For time slots masked by the ACTTS bit in the TSSR, the output from the PISO is 16 0s.

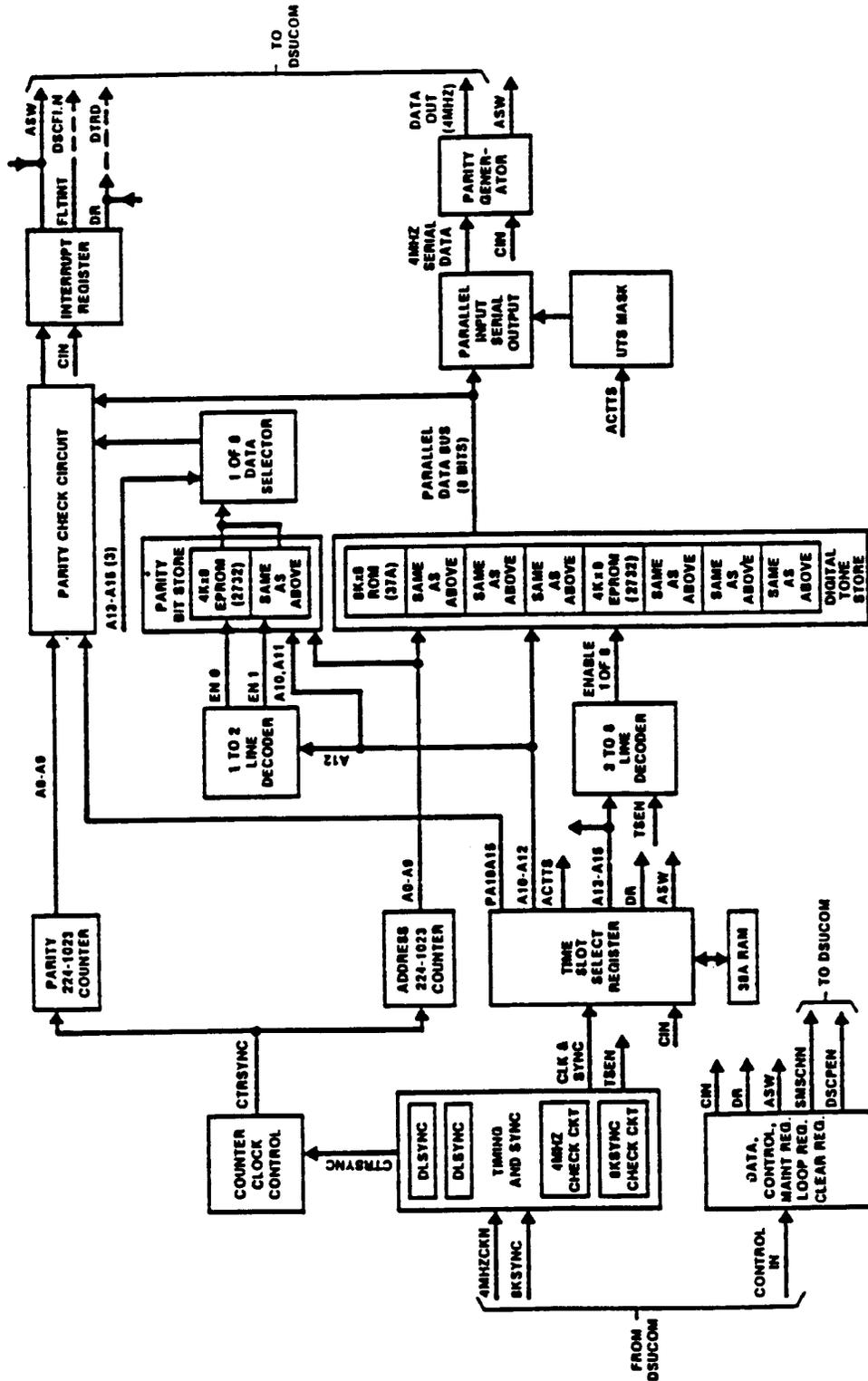
7.46 The parity generator includes two 16-bit registers with write only capability. One register addresses time slots 0 through 15. The other register



8748 Software FIFO Buffer

M14180006

Figure 11



Tone Generator Circuit Pack-TN132  
Functional Block Diagram

Figure 12

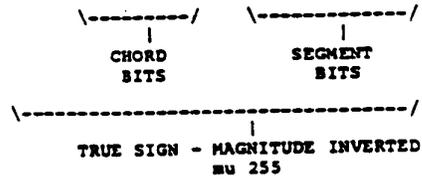
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PISO OUTPUT TIME SLOT DATA FORMAT

TIME ----->

MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S I G N	2	1	0	3	2	1	0	0	0	0	0	0	0	0	0	0



addresses time slots 16 through 31. All bits in both of these registers must be set low (0) for normal operation. For this condition, the parity generator checks the data input from the PISO and generates a parity bit to provide odd parity output on the data bit stream. That is, an odd number of 1s in each 16 bits of output per time slot. The parity bit location is shown in the UTG DATA OUTPUT FORMAT shown below.

It should be noted that bits 1 through 7 are all 0s.

Even parity can be forced on time slots 0 through 31 by writing the appropriate parity generator register time slot bit or bits to a 1. This feature is used for diagnostics.

#### L. Maintenance

7.47 Each DSC, including the UTG, has a maintenance register and an identification loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out-of-service lamp and another is looped back to the identification loopback register for control channel verification. The identification loopback register, when read, returns the looped bit and a seven bit UTG identification code. Each DSC has a unique code.

#### M. Interrupt Register

7.48 Self maintenance checks are continually performed in the UTG. The interrupt register monitors the outputs from these maintenance circuits and when a fault occurs, latches the fault into an internal register and reports to the DSUCOM that a fault has occurred. This is done autonomously and is indicated by the normal 1 level on the DSCFLN interface lead between the UTG and DSUCOM going to a 0 level. The interrupt register is an 8-bit register with both write and read capability. At this time, only 5 bits are used. The write function is used to mask interrupts. That is, writing a 1 to a particular bit position prevents an interrupt from occurring at the interrupt register FLTINT output (refer to Figure 12) even though a fault signal for that bit position has occurred at the input to the interrupt register. With the mask written for all 0s, all interrupts are enabled. If a fault occurs and is reported to the DSUCOM as previously described, a subsequent read command can be issued to the interrupt register to determine the cause of the interrupt. After a fault has been cleared, the interrupt register can be cleared by writing the CLRINT bit in the clear generate register to 1.

7.49 The 5 bits presently used on the interrupt register are utilized as follows: One bit is used to indicate the loss of 4 MHz clock at the input to the clock check circuit. One bit indicates the

loss of the 8K sync input to the sync check circuit. One bit indicates the absence of the 8K sync input to the TSSR. An interrupt also occurs at this bit position if the parity invert bit on the TSSR is set to a 1 for any time slot position. One bit indicates that a fault occurred in the parity check circuit. And, one bit indicates the loss of the 8K sync input to the parity generator gate array. Maintenance circuits in the UTG that cause interrupts as a result of the absence of 4MHz clock and 8K sync can be checked during diagnostic routines by disabling the clock and the sync signals at the output of the DSUCOM.

#### N. Parity

7.50 Extensive parity is used for fault detection in the UTG. Parity is checked across address and data for all tones. The description that follows implies the use of four 8K by 8 ROMs (37A) and four 4K by 8 EPROMs (2732) for tone data and two 4K by 8 EPROMs (2732) for parity. This is the arrangement used for the production version of the UTG.

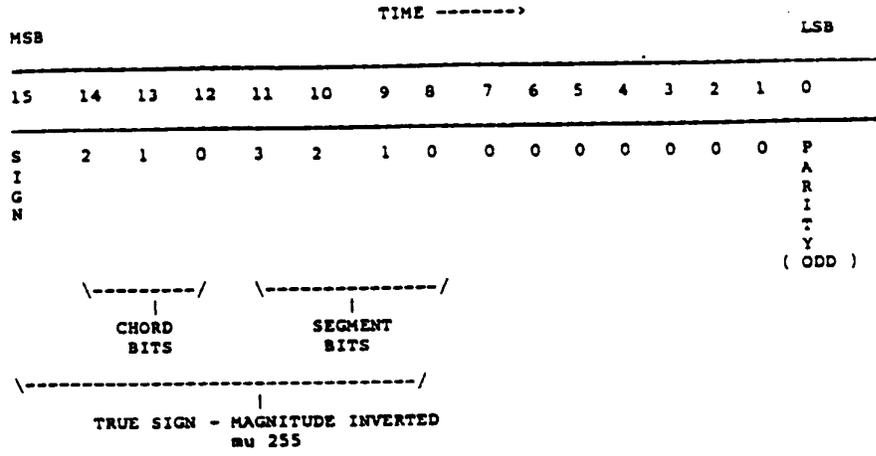
7.51 The 10 bits A0 through A9, as shown in Figure 13, provide the lower 10 bits of address (224 - 1023) for all tones. The 3 bits A10 through A12 select 1 of 8 memory address levels (1 of eight tones) in each 37A ROM, whereas A10 and A11 select 1 of 4 memory address levels (1 of four tones) in each 2732 EPROM. And, the last 3 bits A13 through A15 enable only 1 of the 8 EPROMs/ROMs which places the addressed byte of data on the parallel data bus.

7.52 A computer program has been developed to determine the correct parity bit 1 or 0 that should be loaded into the parity bit store EPROMs for each address and each byte of data addressed.

7.53 Parity bits for all tones located in levels 0 through 3 of each EPROM and ROM are stored in one EPROM while the parity bits for all tones located in levels 4 through 7 for the 37A ROMs are located in another EPROM. These bits are arranged in the parity bit store EPROMs as one bit X 800 word groups, with the lowest addressable parity bit occupying the least significant bit position of location 224 in the 0 parity EPROM.

7.54 Addressing for these parity bits is as described here. The same 10 bits A0 through A9 that addressed the EPROMs/ROMs used for storing the digital tones provide the lower 10 bits of address for all parity bits. Bits A10 and A11 select one of four memory address levels in each of the parity bit store EPROMs. The 3 to 8 line decoder, used as a 1 to 2 line decoder, is controlled by A12 and allows only one parity EPROM to be enabled at a time. The column selection of the 800-bit

UTG DATA OUTPUT FORMAT





slice of the desired parity bits is made by the 1 of 8 data selector which is connected to the eight data out leads of the parity EPROMs and is controlled by bits A13 through A15. The result is that only 1 parity bit is output for each address location.

7.55 As shown in Figure 12, the parity counter uses the same clock input as the Address counter. The two counters are synchronized through software initialization of the UTG. The 10 bits A0 through A9 from the parity counter are inputs to the parity check circuit as is the PA10A15 lead from the TSSR which represents parity across A10 through A15. In addition, the parity bit output from the 1 of 8 data selector and the 8 bits from the parallel data bus are used as inputs to the parity check circuit.

7.56 Internal to the parity check circuit, the 10 bits of address from the parity counter and the parity result across A10 through A15 from the TSSR are used as inputs to a parity generator the output of which represents the parity across the full 16 bits of address. The 8 bits of data are also used as inputs to a parity generator. The output from these two parity generators are exclusive ORed. The output from this exclusive OR circuit is parity across 16 bits of address and 8 bits of data. This signal is connected to the input of a second exclusive OR circuit which has for its other input the parity bit from the parity bit store. Here then, the parity developed across data and address is compared on a per time slot basis with the parity bits stored in the parity bit store. This output is connected to a NAND gate which has as its other input a strobe pulse which has as its other input a strobe pulse when it is stable. The output from this NAND circuit is used as an input to the interrupt register.

7.57 Normal operation results in a high-level 1 on the parity check circuit output lead connected to the interrupt register for all time slots. However, if a problem occurs in either the address or parity counters, TSSR, 3 to 8 line decoder, any bit of tone data or parity in the EPROMs/ROMs, the 1 of 2 decoder, or the 1 of 8 decoder, the output from the parity check circuit goes low 0 when strobbled and latches a PARINT fault in the interrupt register which is reported to the DSUCOM via the DSCPLN interface lead between the UTG and the DSUCOM.

#### CONFERENCE CIRCUIT - TW234

7.58 The TW234 circuit pack provides the function of conference calling for No. 3 ESS. Only three party conference calls are performed by the TW234. The present TW234 design allows two 3-port conference calls to be performed simultaneously on a single TW234 circuit pack. In addition to the 3-party calling feature, the conference circuit is used for "busy line verification," as well as, in conjunction with the "service evaluation system."

7.59 Busy line verification involves processing of the signaling bits in addition to the normal conference processing of the PCM signals. This verifies the ON- or OFF-hook status of the line in question and this requires that an interchange of the A signaling bits be performed on the incoming time slots. The following example illustrates this process.

7.60 Assume a 2-party call is in progress between parties A and B. The operator is requested to verify the A party's line to see if a call is indeed in progress. The No. 3 ESS reconfigures the call as a 3-port conference call with the operator bridged on as the C party. It is required that the A signaling bit from the A party be output on both the B and C (operator) time slots and that the A signaling bit from the B party be placed on the A party's outgoing time slot. The interchange of the signaling bits takes place in the TW234 as part of the conferencing algorithm.

7.61 It should be noted that when the line is verified, the C (operator) input time slot to the CC contains idle code (0x7F). Busy line verification calls must be configured as indicated above. That is, the A party is the line to be verified, the B party is the second party of the original call, and the C party is the operator. A, B, and C refer respectively to the first, second, and third time slots assigned to the conference connection.

#### O. Introduction

7.62 A block diagram of the conference circuit (CC) is shown in Figure 14. This circuit can be separated into two distinct groups - a functional group and a maintenance group. The functional group is the circuitry which performs the actual conferencing function. The maintenance group is additional circuitry which performs monitoring and checking and permits software access to exercise the CC hardware.

#### P. Functional

7.63 Refer to Figure 14. Timing and synchronization signals required for operation of the CC are derived from the 4MHZICM and the 8KSYNC signals which are inputs from the DSUCOM. This circuit, timing and synchronization, also supplies the clock signals required by the DSPs. These are shown in Figure 14 as 4MHZ, 4MHZ1, and 4MHZ0. 4MHZ is used to control the frequency of each DSP clock generator; 4MHZ1 is used to shift data bits into each DSP; 4MHZ0 is used to shift data bits out of each DSP. DSPSYNC, OCO and ICO are used for synchronization of the DSPs.

7.64 Proper operation of the CC is determined by control signals (CONTROL IN on Figure 14). Control signals are received from the module control unit (MCU) via the DSUCOM. The data control section serves as the distribution point for these signals shown as CIN in Figure 14. These signals are inputs to the

maintenance register, loop register, clear register, parity check register, time slot select registers (TSSAs), interrupt register, parity generator, and the DSP control and status registers.

7.65 Control signals perform either a write to or a read from a register. At the end of a write or read command to a register in the CC, an all seems well pulse (ASW in Figure 14) is returned to the MCU via the DSUCOM. This signal indicates only that a write or read was performed by the associated register. When a read command is sent to a particular register, the register clocks out the data that exists at its input. This data appears on the DTRD lead and is sent to the MCU via the DSUCOM at a 2.048 MHz rate.

7.66 It is required that the DSPs be reset prior to each new conference call. ORESET and IRESET are used to enable this function in the ODSP and IDSP respectively. These reset pulses are provided by the clear generate register. This register produces a single pulse output in the desired bit position when addressed. It is not required to remember the state of this register, since the register automatically clears after each write. The clear generate register is also used to clear the parity fault register in the parity check gate array as well as the interrupt register.

7.67 There are two time slot select registers (TSSRs) in the CC. The time slot select register gate array is a per time slot controller which is used in conjunction with a JSA memory to produce eight control outputs for every 3.906 usec time slot. The JSA is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC and DSUCOM with the TSSR operating as a memory controller. The TSSR autonomously reads the JSA memory once per time slot to fetch the eight control bits for the following time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906 usec time slot and are held valid for the remainder of the time slot to provide control functions on a per time slot basis.

7.68 The CC uses only five of the OTSSRs eight output control bits. Two bits (OISY and LISY) are used to control the data input to the 0 and 1 DSPs respectively. One bit (DSPSYNC) is used to synchronize the time-slot data inputs to each DSP with the program that presently resides in EPROMs and subsequently reside within each DSP in ROM. This bit is brought high (1) for the first active time slot associated with each DSP. This serial pulse train (two pulses maximum) is used as an input to the timing and sync circuit. The outputs from the timing and sync circuit as a result of the DSPSYNC are OCO and ICO which are inputs to the 0 and 1 DSPs respectively. The DSPs remain in a suspended state (the program does not continue) until a CO pulse is received.

These pulses are timed (1 per frame) to occur at the time the data for the first of the three time slots associated with a DSP is loaded into the DSP input buffer. One bit (EMASK) is used on a per time-slot basis to prevent parity faults that are detected in the parity check circuit from being latched into the 32-bit parity fault register in the parity check circuit. This bit also prevents these same parity fault signals from occurring on the DSCFEN interface lead between the CC and the DSUCOM. Another bit (IMASK) is also used on a per time slot basis and allows parity faults, that are detected in the parity check circuit, to be latched into the 32 bit parity fault register in the parity check circuit, but prevents these faults from being reported to the DSUCOM on the DSCFEN signal lead.

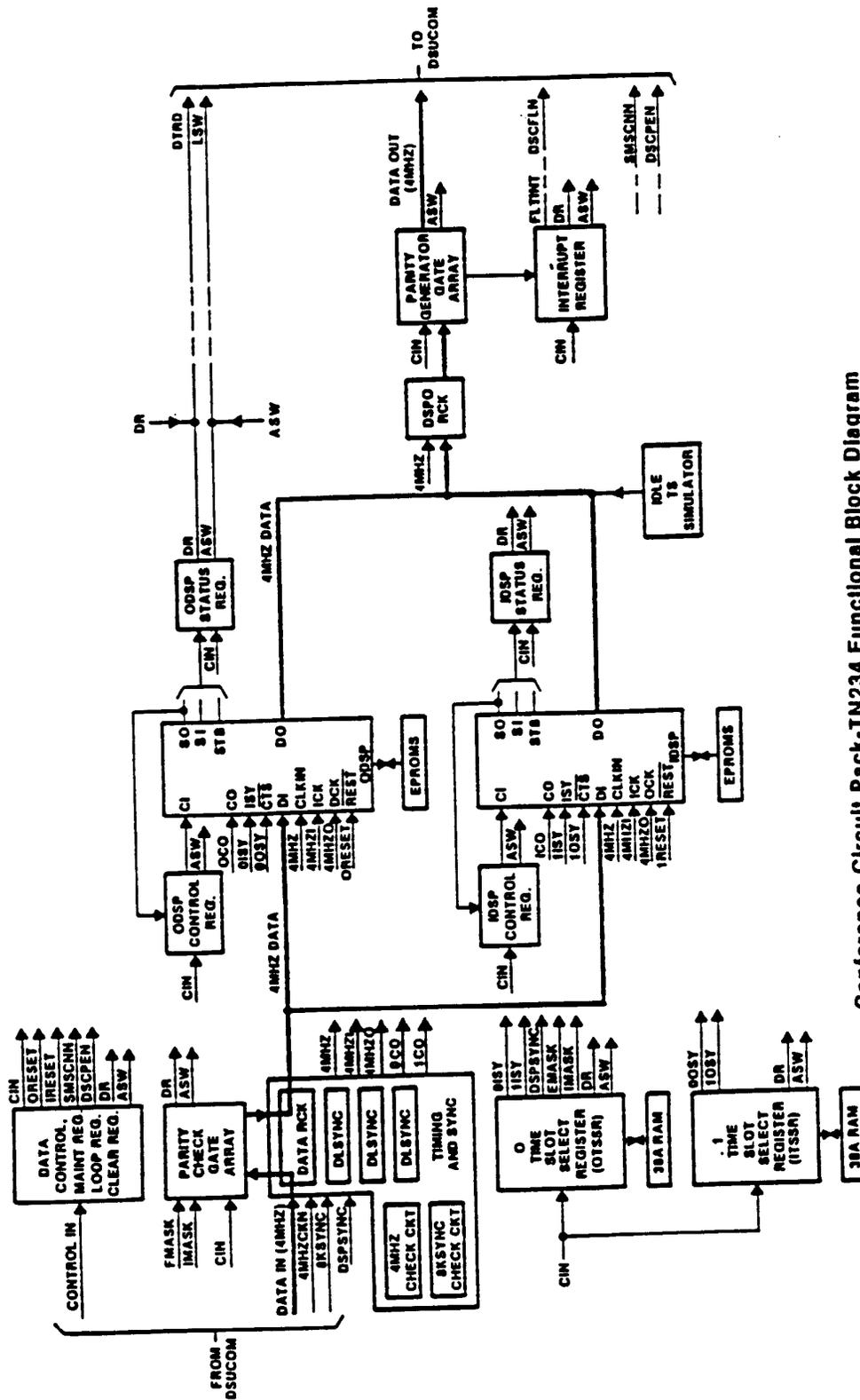
7.69 The CC uses only two of the ITSSR's eight output control bits. These two bits (OOSY and LOSY) are used to control the data output from the 0 and 1 DSPs respectively. These bits are set high (1) for the same time slots selected for the OISY and LISY bits in the OTSSR.

Input data to the CC is from the Time Slot Interchange Unit (TSIU) via the DSUCOM. This input is a 4.096 MHz, 32 time slot, 16 bits per time slot, serial bit stream.

The input time slot data format is shown below.

7.70 The 32 time slots of data are reclocked and then used as an input to the parity check circuit. The parity check circuit includes two 16-bit registers with read only capability. One register reads parity input errors for time slots 0 through 15. The other register reads parity errors for time slots 16 through 31. Internal to the parity check circuit, the data input (16 bits) for each time slot is checked for odd parity. If bad (even) parity is detected for any time slot, the error for that time slot is latched into the corresponding time slot position in the related register. In addition to latching the parity error into the register, the error is also reported to the DSUCOM via the DSCFEN signal lead. If a parity error occurs, and is reported to the DSUCOM as previously described, a subsequent read command can be issued to the parity check circuit to determine the time slot that caused the fault. After a fault has been cleared, the parity check circuit registers can be cleared by writing the CLRCHK bit in the clear register to 1. Two mask bits (EMASK and IMASK) are provided in the OTSSR for inhibiting the parity check parity errors. These bits were described previously.

7.71 The PCHKPI bit in the maintenance register can be used to force even parity on the data output from the parity check circuit. This affects the parity on all time slots. Forcing even parity with PCHKPI does not cause a fault in the parity checker in the parity check circuit. Also,

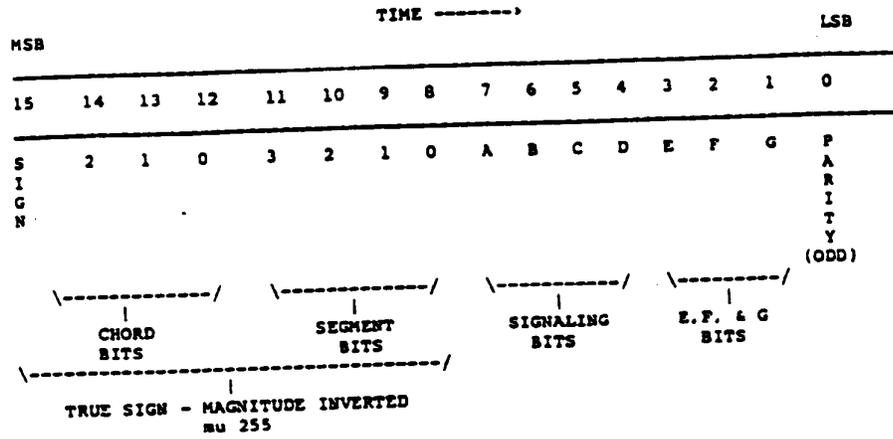


Conference Circuit Pack-TN234 Functional Block Diagram

Figure 14

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CC INPUT TIME SLOT DATA FORMAT



the absence of the 8K sync input to the parity check circuit causes the PCSYNCE interrupt bit in the interrupt register to be set.

7.72 Figure 15 shows the time slot assignment format required by the CC. As shown, up to 30 time slots are available for a CC. The reserved time slots can be even or odd as shown. The 30 time slots are divided into 10 groups of three each. Each group consists of every tenth time slot, e.g., time slots 0, 10, and 20 for the first group. Any of the DSPs can be assigned to any of the 10 groups. The assignment of the first time slot in the first group is not restricted to time slot 0 as shown, but can range from 0 through 31. However, it is required that every tenth time slot format be maintained. That is, if the first group is selected to be time slots 1, 11, and 21, the tenth group of time slots would be 10, 20, and 30.

7.73 The DSP is a programmable digital signal processor. The program for each DSP is presently contained in external EPROMs. The frequency of the DSP is controlled by the 4MHz clock which is derived from the system clock.

7.74 The task for each DSP in the CC is as follows:

- (a) Input 3 time slots of 16-bit data (8PCM bits and the A through G bits plus the parity bit).
- (b) Perform a 3-port conference algorithm on the 8 PCM bits contained in the 3 time slots.
- (c) Perform a time-slot interchange on the A through G bits for the 3 time slots.
- (d) Combine the PCM output bits for each time slot with the proper A through G bits.
- (e) Generate an odd parity bit over the output PCM bits and the A through G bits for each time slot. And, affix this parity bit 1 or 0 to the parity bit position of the data output.
- (f) Provide a means for forcing bad (even) parity on the data output under external program control using the C1 control bit on the DSP.
- (g) Additional functions can be performed by S0, S1, and STB.

7.75 A brief functional description of the DSP I/O leads shown in Figure 14 are given below.

7.76 DI receives the serial data from the parity check circuit and DO transmits serial data to the parity generator. ISY indicates the start of a data transfer to the input buffer and ICK is used to shift bits into the input buffer via DI. CTSO enables the start of a data transfer from

the output buffer and OCK is used to shift bits out of the output buffer via DO.

7.77 Control input CO is tested by the DSP program. This input synchronizes the DSP program with the input of the first of the three time slots associated with the particular DSP. C1, S0, S1, and STB are used in conjunction with the DSP control and status registers.

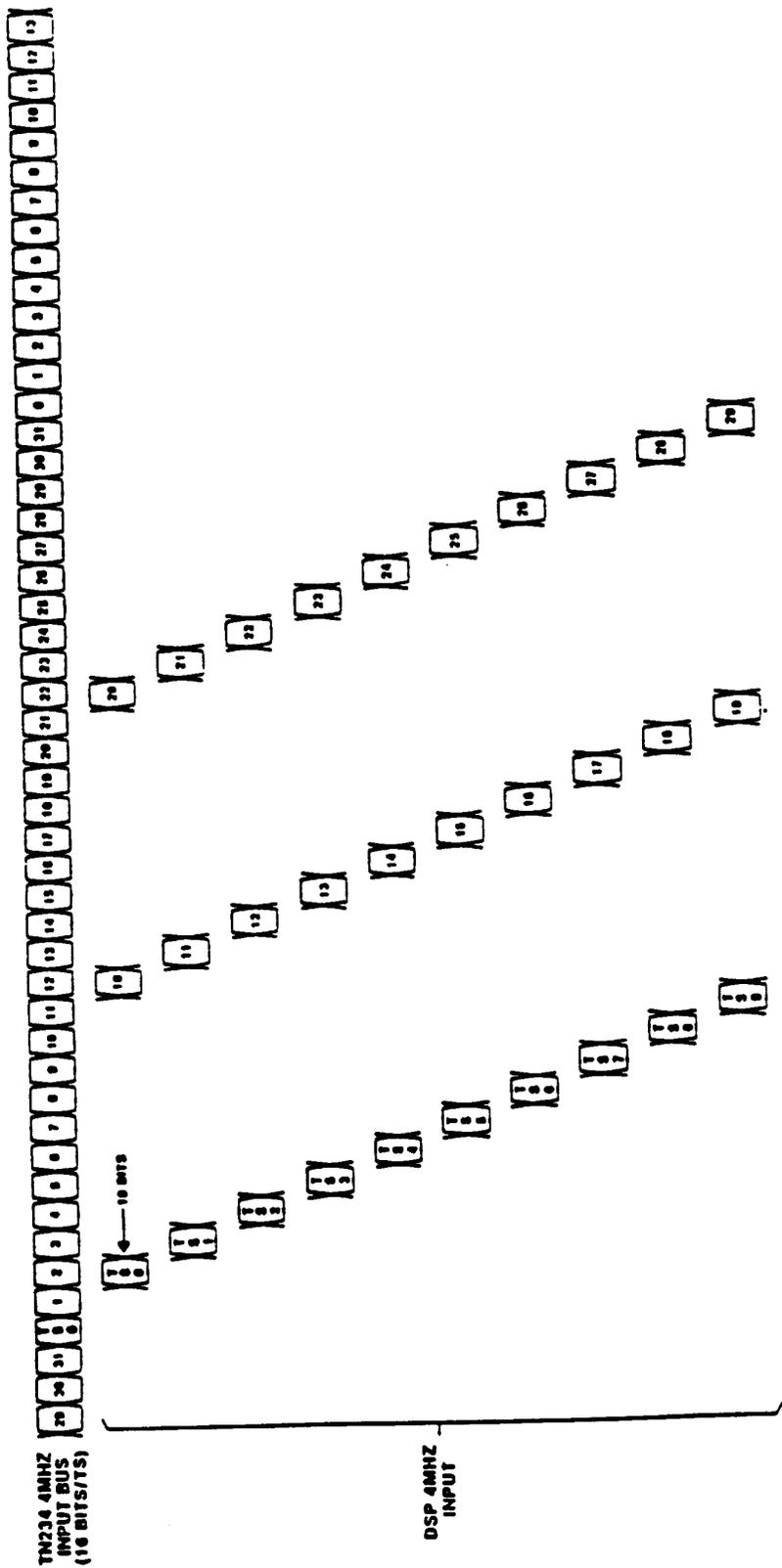
7.78 Data output from each active DSP consists of three time slots of 4.096 MHz, 16 bits per time slot, data with odd parity. The latter is true providing that the associated DSP control register has the least significant bit written to a 1. The other bits are don't cares. Writing the least significant bit of this register to a 0 results in bad (even) parity on the data output for the third time slot associated with the conference call and sets the PGPERR in the interrupt register. The outputs from the DSPs and the outputs from an idle time slot simulator are multiplexed to form 32 time slots of 4.096 MHz, 16 bits per time slot, data. The format for the active time slots is shown below.

7.79 Idle time slots are filled with 15 0s and a 1 in the parity bit position to provide odd parity. The output data is reclocked and then used as the input to the parity generator.

7.80 Internal to the parity generator, the data input (16 bits) for each time slot is checked for odd parity. If bad (even) parity is detected for any time slot as indicated previously, the error is latched into the PGPERR bit position of the interrupt register and is reported to the DSUCOM via the DSCFLN signal lead.

7.81 The parity generator includes two 16-bit registers with write only capability. One register addresses time slots 0 through 15. The other register addresses time slots 16 through 31. All bits in both of these registers must be set low (0) for normal operation. For this condition, the parity generator checks the data input and generates a parity bit to provide odd parity output for each time slot. This is done even though a parity bit error has already been detected and reported to the DSUCOM as previously described.

7.82 The parity generator data output format is the same as that shown above except that it is delayed in time. It should be noted that idle time slots are filled with 15 0s and a 1 in the parity bit position. Also, the A through G bits have been slot interchanged as described previously. Even parity can be forced on time slots 0 through 31 by writing the appropriate parity generator register time slot bit or bits to a 1. This feature is used for diagnostics.

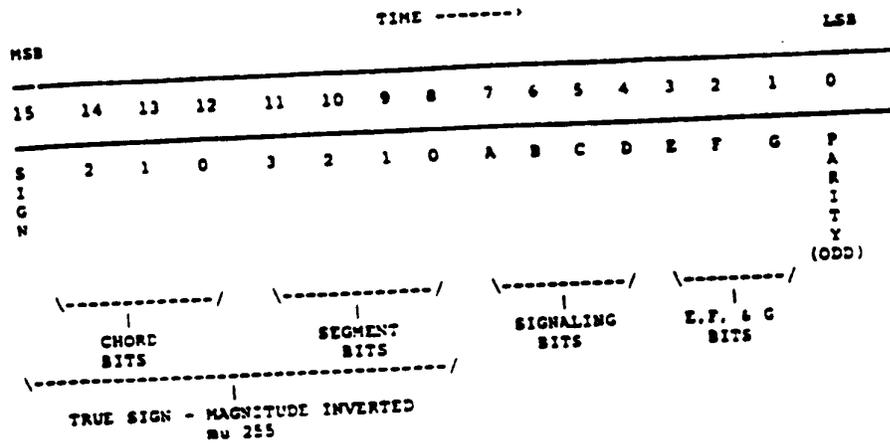


Conference Circuit Pack-TN234 Time Slot Assignment Format

Figure 15

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TIME SLOT DATA FORMAT



**O. Maintenance**

7.83 Each DSC, including the CC, has a maintenance register and an identification loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out of service lamp and another is looped back to the identification loopback register for control channel verification. The identification loopback register, when read, returns the looped bit and a seven bit CC identification code. Each DSC has a unique code. Finally, one bit of the maintenance register is provided to force bad (even) parity output from the parity check gate array.

**R. Interrupt Register**

7.84 Self maintenance checks are continually performed in the CC. The interrupt register monitors the outputs from these maintenance circuits and when a fault occurs, latches the fault into an internal register and reports to the DSUCOM that a fault has occurred. This is done autonomously and is indicated by the normal 1 level on the DSCFLN interface lead between the CC and DSUCOM going to a 0 level. The interrupt register is an 8-bit register with both write and read capability. At this time, only seven bits are used. The write function is used to mask interrupts. That is, writing a 1 to a

particular bit position prevents an interrupt from occurring at the interrupt register FLTINT output even though a fault signal for that bit position has occurred at the input to the interrupt register. With the mask written for all 0s, all interrupts are enabled. If a fault occurs, and is reported to the DSUCOM as previously described, a subsequent read command can be issued to the interrupt register to determine the cause of the interrupt. After a fault has been cleared, the interrupt register can be cleared by writing the CLRINT bit in the clear generate register to 1. The 7 bits presently used on the interrupt register are utilized as follows:

One bit is used to indicate the loss of 4 MHz clock at the input to the clock check circuit. One bit indicates the loss of the 8K sync input to the sync check circuit. One bit indicates the absence of the 8K sync input to the OTSSR. An interrupt also occurs at this bit position. If the parity invert bit (PINV) on the OTSSR is set to a 1 for any time slot position. Another bit provides the same function for the ITSSR. One bit indicates the loss of the 8K sync input to the parity generator gate array. One bit indicates the absence of the 8K sync input to the parity check gate array. And, one bit indicates that a parity error has been detected on the data input to the parity generator.

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