5ESS™ SWITCHING EQUIPMENT
TIME MULTIPLEXED SWITCH CONTROL UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Information is provided for the TN1575 circuit pack which is required when O.R.M. feature is provided on CM1.

Note 302 - Feature or option table has added options x (for the TN267 pack) and w (for TN1575 pack).

Note 303 is updated in accordance with changes in Note 302.

Note 304 is updated to show microcode for the TN1575 pack.

D.2 App. Fig. 1 is changed to show new options x and w for circuit packs TN267 and TN1575, respectively.

D.3 FS3 is changed to show that the TN267 circuit pack is used with option x only, and the TN1575 pack is used with the option w.

AT&T BELL LABORATORIES

DEPT 11NW527280-REG-DFH

5ESS™ SWITCHING EQUIPMENT
TIME MULTIPLEXED SWITCH CONTROL UNIT
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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Time Multiplexed Switch Control Unit (TMCU) performs five basic functions.

a. The TMCU controls the operation of two (one odd, one even) Time Multiplexed Switch Units.

b. The TMCU provides an interface between the Network Control and Timing (NCT) link from the Message Interface and Clock Unit (MICU) and the TMS Switching fabric. Control messages between the Switch Modules (SMs) and the Central Processor (CP) flow through this interface.

c. The TMCU collects and reports to the CP all errors that occur in itself and the TMSUs.

d. The TMCU contains a test board which provides data patterns for diagnostics of the TMSU. It is also the source of idle code on all time slots for the TMS.

e. The TMCU contains a clock board which generates all clocks needed in the TMS.

The TMCU contains six logic circuit packs: TN268 (TMS Controller), TN269 (TMS Interface), TN265 (TMS Maintenance), TN270 (TMS Clock Interface), TN267 (Test Board), and TN252 (Message Link Interface).

SECTION II - DETAILED DESCRIPTION

1. TMS CONTROLLER - TN268

1.01 The TMS Controller (TN268) is an 8086 microprocessor based system that performs the following functions in the TMS.

a. Translates control messages for setting up fabric paths into fabric memory addresses and fabric memory data.

b. Provides periodic reinitialization of the LI boards (Link Interface) link error threshold counters.

c. Handles maintenance messages requiring read/write access to microprocessor memory or I/O devices.

d. Monitors maintenance functions and errors.

e. Provides a software mechanism for error filtering.

f. Initiates an error message to the Central Processor (CP) when error thresholds are exceeded.

g. Triggers an error lead to the MICU when the sanity timer goes off.

h. Executes diagnostic messages sent from the CP.

2. TMS MAINTENANCE BOARD - TN265

2.01 The TMS Maintenance Board provides a central collection point to register all errors that have occurred in the TMS. The Summary Error Register (SESR) represents errors reported from lower levels of the error hierarchy. The Control Error Summary Register (CESR) represents errors attributable to the control structure of the TMS. Both error registers are maskable by the bit.

The Maintenance Board contains a programmable interval timer. This IC contains three counters, one of which is used as the sanity timer. The other two are cascaded together to provide a Link Interface (LI) reinitialization timer.

Also, on the Maintenance Board is a universal interrupt controller chip. This device is used to latch and prioritize interrupts for the microprocessor on the TN268.

3. TMS INTERFACE BOARD - TN269

3.01 The TMS Interface Board (TN269) manages all I/O communications of the TMS controller. The controller is composed of the microprocessor based TMS control bard (TN268), the TMS maintenance board (TN265), and the TMS interface board (TN269).

The TMS Interface Board communicates with the Message Interface and Clock Unit (MICU) through the Control and Diagnostic Access Link (CDAL). Forty-bit control messages travel serially at 2 MHz rates over the CDAL.

Two types of messages that pass through TN269, those that allow the Foundation Peripheral Controller (FPC) access (via the MICU) to TMS switch units without microprocessor intervention and those that require microprocessor intervention.

Control messages are converted to parallel from the CDAL data stream to decode that destination portion of the message. Depending upon results, the message is transmitted over parallel bus to the microprocessor (or TMS Maintenance Board) or the data is converted back to serial stream for transmission to the selected shelf interface, test board or message link interface.

4. TEST BOARD - TN267

4.01 The Test Board (TN267) is a circuit pack which resides in the TMCU. It has two main functions. During normal frame operation it is the source of idle code on all time slots for the TMS. During maintenance, it provides a series of data word patterns which are used by the TMS diagnostic to exercise the fabric, fanout, and link interface circuit packs. The Test Board receives its control messages over a 40-bit, 2 MHz serial control bus from the TMS interface board.

5. TMS CLOCK INTERFACE BOARD - TN270

5.01 The TMS Clock Interface circuit pack (TN270), generates four clock frequencies required by the Time Multiplexed Switch (TMS) and the network clock system synchronization is accomplished by phase locking the local Voltage Controlled Oscillates (VCO) to a reference 8 kHz signal supplied by the network clock.

Clock distribution to both TMSUs and the TMCU is accomplished using ECL balanced line drivers. A 16 MHz clock and an 8 kHz sync pulse are distributed to the TN243 (link interface), TN242

(fabric board), TN267 (test board), and TN252 (MLI), circuit packs within the TMS. The 16 MHz is also used by the LN74 (fanout board). A 2 MHz clock is distributed to the TN244 (shelf interface) in the TMSUs and the TN269 (TMS Interface) and TN265 (TMS Maintenance) circuit packs in the TMCU. Finally an 8 kHz square wave is sent to the network clock. All clocks are derived by dividing down the 32 MHz local VCO.

6. MESSAGE LINK INTERFACE - TN252

6.01 The Message Link Interface (TN252) provides an interface between the NCT link from the MICU and the TMS switching fabric. TN252 terminates one NCT link and performs the function of synchronizing messages from the link with the internal TMS clock for a transmission through the fabric during the proper time slot. An elastic buffer stores control messages in RAM until the proper time for their transmissions through the fabric. Transfer of control messages between the CP and the SMs is accomplished this way.

The TN252 has an error source register to record transmission errors and a maintenance register to control various checking circuits and maintenance functions.

SECTION III - REFERENCE DATA

1.01 See the individual circuit pack CDs.

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