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5ESS™ SWITCHING EQUIPMENT
TIME MULTIPLEXED SWITCH UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus (Components)

Superseded

Superseded By

982CG,CF Fiber Optic RCV/TRANS connectors in FIG. 2-17 "F" option	982TA,WY Fiber Optic RCV/TRANS connectors in FIG. 2-17 "E" option
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D. Description of Changes

D.1 Fiber Optic connectors are introduced to provide for TRM (TRANSMISSIONLESS REMOTE MODULE). FS 2, CADs 6 and 7, APP FIG. 2-17 and Feature Table are changed to show 982CG,CF designated "F" Option and APP 982TA,WY per "E" Option.

D.2 In CADs 6, 7, and FS 2, reference is added to a new connecting circuit for O.R.M. - Transmission Rate Converter Unit, SD-5D086-01.

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AT&T-T DEPT 11NW527280-REG-EBH

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SESSTM SWITCHING EQUIPMENT
TIME MULTIPLEXED SWITCH UNIT
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SECTION I - GENERAL DESCRIPTION1. PURPOSE OF UNIT

1.01 The function of the Time Multiplexed Switch Unit (TMSU) is to provide switched connections for data transfer between Switch Modules (SMs). Control information from the Control Processor (CP) to any SM is also transferred through the TMSU fabric.

1.02 The TMSU fabric is equipped as needed. It can grow to a 32 by 32 matrix for a fully equipped unit. A fully equipped unit will handle communication between 30 SMs, communication from CP to any SM, and diagnostic test access to the fabric itself.

1.03 The connections through the TMSU fabric are reconfigured 256 times during one data frame (of 256 time slots). Configuration information for the fabric during each of the 256 time slots is supplied by the Time Multiplexed Switch Control Unit (TMCU). Configuration of the fabric is different for each of 256 time slots, therefore, the connection configuration information is stored in a 256 byte RAM by the TMSU and is cycled through by the TMS clock.

1.04 Data enters and leaves the TMSU serially at a 32 Mb rate by way of Network Control and Timing Links (NCTs). Physically, NCT links are optical fibers. Each SM requires two NCT links to connect to the two

(even and odd) TMSUs needed for simplex operation.

SECTION II - DETAILED DESCRIPTION1. SHELF INTERFACE (TN244)

1.01 TN244 is the Shelf Interface (SI) circuit pack. The SI distributes control messages received from the TMS interface to each 32 by 4 fabric board and Link Interface (LI) board on its shelf. The SI receives a 40-bit message from the TMS interface, 5 bits of which are compared to a hardwired address corresponding to the shelf ID upon which the SI pack resides.

1.02 The SI has two error source registers. Error source register 1 contains the error status of each 32 by 4 fabric board and each LI board located on that shelf. Error source register 2 contains the errors attributed to hardware on the SI and incoming data parity errors. Each bit of the error source registers can be marked to inhibit error reporting via a command from the TMS interface. A TMSU has two SIs (TN244s), one for each shelf.

2. LINK INTERFACE (TN243)

2.01 The TN243, LI provides an interface between the NCT links and the switching fabric. Each LI pack terminates two NCT links and performs the general function of synchronizing the data from the NCT link with the

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internal TMS clock for transmission through the fabric. The latter is accomplished by an elastic buffer implemented with RAM. Control instructions for the LI are sent from the SI as 4 byte messages.

2.02 Another function of the LI is to split data for easier passage through the fabric. Serial data from the 32 Mb NCT links is divided into two 16 Mb data streams for input to the fabric. Two 16 Mb serial outputs from the fabric are combined for 32 Mb NCT link transmission. A TN243 pack can then transmit and receive all even or all odd time slots for two SMs.

3. FANOUT BOARD (UN74)

3.01 The fanout board (UN74) provides distribution of clock signals and data within the TMSU. There is one fanout board per shelf.

4. FABRIC BOARD (TN242)

4.01 The fabric board (TN242) provides a switched connection for data

flow from transmitting to receiving LIs. This is accomplished by utilizing dual 32 by 4 multiplexers, allowing each fabric board to handle four output links. The duality arises because the LI board transmitting data to the fabric has split the 32 Mb data stream into two 16 Mb data streams. Data enters the fabric from an LI and is output to another LI.

4.02 Control information is sent to the fabric boards by the SI on the same shelf. Received control (configuration) information is stored in a 256 byte RAM and is used to provide a new set of connections for each time slot.

SECTION III - REFERENCE DATA

1.01 See the individual circuit pack CDs.

SECTION IV - REASON FOR REISSUE

1.01 To correct previous issues of this CD.

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