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5ESS* SWITCHING EQUIPMENT TIME SLOT INTERCHANGER UNIT, MODEL 2 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This document is a circuit description of the Time Slot Interchange Unit Model 2 (TSIU2). The TSIU2 has been developed for cost reduction purposes. Cost reduction is achieved by increasing the level of hardware integration using LSI technology.

2. GENERAL DESCRIPTION OF OPERATION

CIRCUIT ORGANIZATION

2.01 5ESS Electronic Switching System is a digital time division switch with a time-space-time architecture. The Time Multiplexed Switch (TMS) provides the central space division switching function and connects to various Switching Modules (SMs) which perform the time division switching function and interface to the transmission facilities. The interface between the TMS and SMs is via optical fibers called Network Control and Timing (NCT) links.

2.02 An SM contains a Switching Module Processor Unit (SMPU) to provide control, a Time Slot Interchanger Unit Model 2 (TSIU2) to perform the time division switch and related functions, and various Peripheral Units[1]. The TSIU2 and SMPU are common to all IMs and the Peripheral Units are equipped as needed.

2.03 The TSIU2 in the SM provides the following functions:

1. Provides a time division switch under control of the SMPU;
2. Performs preprocessing on the signaling and control bits of the time slot data and provides the SMPU access to them;
3. Provides the interface to the NCT links;
4. Provides an interface to the Peripheral Units for control information from the SMPU;
5. Provides an interface to the Peripheral Units for PCM data;
6. Provides the SMPU with an interface to the Message Time Slots of the NCT links.

TIME SLOT INTERCHANGE UNIT MODEL 2 (TSIU2)

2.04 The following sections deal with the previously mentioned TSIU2 functions in more detail. The basic interfaces and functions are retained from the 5E1.1 design (SD-5D041-01).

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1. Digital Service Unit, Metallic Service Unit, Digital Line and Trunk Unit, Line Unit, Trunk Unit, etc.

Cost reduction is the sole reason for introduction of the TSIU2.

2.05 The TSIU2 is a duplicated unit. The mate (or nonactive) side is updated by the active SMPU in order to provide the ability to switch from side to side. Under no fault conditions, this switch to the mate side is done without introducing errors. Error checking circuitry and diagnostic aids are used extensively in order to facilitate maintenance of the TSIU2.

2.06 The following is a description of the functional operation of each of these units.

A. Time Division Switch

2.07 The TSIU2 contains a time division switch that is capable of switching 512 time slots per 125 usec frame in both directions, i.e., from Peripheral Units to the TMS and from the TMS to Peripheral Units. This time division switch is under the control of the SMPU. It also provides the ability to connect peripheral time slots to peripheral time slots (for intramodule calls) and to connect TMS time slots to TMS time slots (for maintenance purposes). The time division switch also provides parity checking on time slot data and reports detected errors to the SMPU. Access to time slot information is available to the SMPU.

2.08 The SMPU has the ability to source A, B, C, D, E, F, G bits for time slots sent to the periphery. The time division switch also provides SMPU access to the A, B, C, D, E, F, G bits in time slots coming from the periphery. "Hit" timing is done on these bits and state changes are reported to the SMPU.

B. NCT Link Interface

2.09 The TSIU2 provides an interface to four optical fiber link pairs (two per each side of the TMS, four total) which provide the connection from the TMS (MICU in a single module office) to the TSIU2. Each NCT link carries data at a 32.768 megabit/second rate. This data is organized into 256, 16-bit time slots per 125 usec frame. One time slot of each NCT link (designated the Message Time Slot) is used to carry control information to and from the SM.

2.10 The NCT link is the source of office timing information for the SM. The TSIU2 extracts this timing information in order for the SM to operate in synchronization with the system. The TSIU2 is able to select any one of the four links as the "master", i.e., the reference timing source.

2.11 There is a one frame buffer on the incoming NCT link data from the TMS in order to compensate for phase shifts and frequency jitter on the NCT links. These buffers are controlled such that nominally they provide 1/4 frame delay, i.e., the buffers are 1/4 full.

2.12 The interface to the NCT links is included in the same failure group as the TMS. This necessitates cross coupling of all control and data leads between the duplicated NCT link interfaces and the duplex SMPU-TSIU2.

2.13 In addition to providing the interface between the time division switch and NCT links, this interface extracts and inserts the message time slot information which is transmitted to and received from the SMPU. A method of selecting one of the 256 time slots as the Message Time Slot on each NCT link must be provided.

C. Peripheral Data Interface

2.14 The TSIU2 provides 32 Peripheral Interface Data Busses (PIDBs) which provide the data interface to the TSIU2 for the various 5ESS Peripheral Units. They carry 4.096 megabit/second data organized as thirty-two, 16-bit time slots per 125 microsecond frame to and from the various Peripheral Units. The cable consists of twisted pairs differentially driven in order to provide common mode noise rejection. Since a total of 1024 time slots are made available to the Peripheral Units, a 2:1 concentration is done on peripheral time slots in order to provide the time division switch with 512 active time slots.

2.15 Cable length of the PIDB cable may vary but has a maximum limit of 20 feet. These cables utilize Berg type connectors which attach directly to TSIU2 backplane pins.

2.16 An additional data port is provided to the Local Digital Service Unit (LDSU) from the time division switch such that the LDSU has access to data necessary to do tone decoding, tone generation, digit collection, and other LDSU functions.

D. Peripheral Control Interface

2.17 The TSIU2 provides up to 46 Peripheral Interface Control Busses (PICBs). These busses carry asynchronous control information to the various Peripheral Units at a 2.048 megabit/second rate.

2.18 The control interface to the peripheral units provides the SMPU with the ability to do 16-bit read and write operations to registers in the Peripheral Units. This interface also receives the service requests from the Peripheral Units and makes them available to the SMPU.

SECTION II - DETAILED DESCRIPTION

1. FUNCTIONAL DESIGNATIONS

1.01 The TSIU2 has five subfunctions, namely, the Time Slot Interchanger (TSI), the Signal Processor (SP), the Dual Link Interface (DLI), the Data Interface (DI), and the Control Interface (CI).

A. Time Slot Interchanger (TSI)

1.02 The TSI is the time division switch. It contains two 512 x 512 time slot interchangers, one for data from the TMS to the Peripheral Units and one for data from the Peripheral Units to the TMS. The two 512 x 512 switches are connected such that time slots may be looped, thereby providing the capability to connect peripheral time slots (for intramodule calls). The TSI also provides a data port to the local DSU.

B. Signal Processor (SP)

1.03 The Signal Processor (SP) does the bit timing and processing on the signaling and control bits (A-G) from peripheral time slots. It provides the SMPU access to these bits and provides a First In First Out (FIFO) type queue to report state changes of these bits. It also allows the SMPU to source these bits to the Peripheral Units.

C. Dual Link Interface (DLI)

1.04 The Dual Link interface (DLI) is the interface to the NCT links. It recovers timing information from these links in order to provide timing for the SMPU-TSIU2. The DLI contains the transmit and receive circuitry needed to interface to the optic links. It also provides the SMPU an interface to the Message Time Slot on each NCT link.

D. Data Interface (DI)

1.05 The date interface (DI) provides the data interface to Peripheral Units. It reformats time slot information and does a 2:1 concentration on peripheral time slots. Two DIs are connected to the TSI, each providing the TSI with 256 time slots per frame. Each DI provides 16 PIDBs for connection to Peripheral Units.

E. Control Interface (CI)

1.06 The Control Interface (CI) provides the interface between the SMPU and the various Peripheral Units for control information. Each CI provides 23 PICBs for these connections. The TSIU2 may be equipped with two CIs (per side) to provide a total of 46 PICBs.

1.07 The TSI, SP, and CI connect to the SMPU via the SMPU Subunit Interface Bus. The data connections between the TSI and the SP, DI, and DLI circuits are via 4-wire "nibble" busses, each operating at an 8.192 megabit/second data rate. Since these connections are bidirectional, two nibble busses are required, one for each direction.

1.08 Since the DLI is in the same failure group as the TMS, cross coupling is necessary for all connections between the DLIs and the duplex TSIU2. The DLI selects one of the two NCT links connected to it or the mate DLI as a reference timing source and the TSI selects one of the two DLIs as a clock source. The TSI then distributes this clock to the rest of the SMPU-TSIU2.

2. FUNCTIONS

A. Time Slot Interchanger - FS 3,4

2.01 The Time Slot Interchanger in the TSIU2 is identical to the design used in the 5E1.1 version TSIU. The TSI consists of five circuit packs (TN865, TN127, TN887, TN315, and TN866). An overview of the TSI operation is presented here.

B. Primary Data Path

2.02 The primary data path delivers 512 peripheral time slots from the DIs to the Receive TSI RAM to be stored in consecutive order. Time slots are then translated from the Receive RAM and can be delivered to both DLIs on any of the 512 network time slots. In the opposite direction 512 network time slots from the DLIs are written consecutively into the Transmit TSI RAM. Time slots are then translated from the Transmit RAM on chosen peripheral time slots as instructed under software control and delivered to the DIs. Any peripheral time slot written into the Receive TSI RAM can be read out onto multiple (up to all) network time slots toward the DLIs. The same fanout capability is provided by the Transmit TSI RAM. A maximum delay in each direction of one frame (125 usec) can be introduced by the Time Slot Interchange.

2.03 Two DIs are connected to the TSI. One DI is dedicated to even TSI time slots and one is dedicated to odd TSI time slots. Each DI provides 256 time slots to the Receive TSI RAM. Sixteen bit time slots in nibble format are sent to the TSI by the DIs (PCM, A-G, and parity). The seven signaling and control bits, A-G, are transmitted with the PCM bits through the Receive TSI RAM and are also sent to the SP.

2.04 The TSI transmits 16-bit time slots in nibble format to the

DIs. Of the A-G bits sent to the DIs, the E-G bits are always sourced from the SP. The A, B, C, and D bits can either be sourced from the SP or passed through from the Transmit TSI RAM. All PCM data sent to the DIs passes through the Attenuation ROM. The Attenuation ROM allows one of 32 values of digital loss to be inserted in the PCM data path on a per time slot basis. The loss values are 0dB through 15.5dB in .5dB increments. The integrity of the data path (TSI to Peripheral unit to TSI) is protected by a walking parity scheme administrated by the TSI which inverts the parity sense of every ninth TSI time slot.

2.05 The TSI receives 512 time slots from the DLI via two 256 time slot nibble busses. The TSI selects which DLI (e.g., DLI0 or DLI1) is the source of time slots to the TSI.

2.06 The TSI transmits 512 time slots toward both DLIs in the TSIU2. The time slots consist of 16 bits in nibble format. The E bit of each time slot sent to the DLIs is set on a per time slot basis via a TSI control RAM written by the SMPU. The A-D bits of each time slot sent toward the DLIs are either passed through from the Receive TSI RAM or sourced from a TSI control RAM.

2.07 Two forms of connections are possible between the transmit and receive RAMs. The first connection allows intramodule paths to be set up by looping time slots on the DLI side of the TSI memories. A connection of this type will block an incoming time slot from the DLIs. The other connection allows intra-DLI connections to be made. A connection of this type will block an incoming peripheral time slot from reaching the Receive TSI RAM, but the blocked peripheral time slots will still have access to the SP and local DSU.

C. Alternate Data RAM (ADR)

2.08 The Alternate Data RAM (ADR) provides the SMPU and local DSU with access to the contents of all 512 time slots. Via the ADR, the SMPU can write constants (e.g., idle code) to be sent to the DIs and DLIs, and sample time slots at various points within the TSI. The ADR also provides SMPU access to the E bits received from the DLI. Parity errors on time slots received by the TSI from the DIs are reported to the SMPU via the ADR. Data stored in the ADR (e.g., tones from the DSU) can be sent to the DIs, sent to the Receive TSI RAM, or sent to the Transmit TSI RAM. The TSI time slots written to the ADR can be sourced on a per time slot basis from four different locations in the TSI. This permits maintenance access and allows time slots from both DIs and DLIs to be sent to the local DSU.

D. Signal Processor - FS 13,14

2.09 The Signal Processor (SP) for the TSIU2 is identical to the SP used in the 5E1.1 version of the MCU. The same three circuit pack codes (TN212, TN213, TN214) are used.

E. Hit Timing

2.10 The SP performs hit timing on all signaling and control bits received from the TSI. This hit timing is performed by scanning the data at a 3 ms rate. A time slot is considered to have changed to a new state only if the bit persists in that state for two consecutive scans. This represents only a very low level of filtering. The SMPU will perform additional hit timing to filter false originations, split pulses, etc.

2.11 Hit timing is accomplished by comparing data in the Input Data Buffer (IDB) with data contained in the Last Look RAM (LLR). The LLR contains

the values of the signaling and control bits contained in the IDB during the previous 3 ms scan. Every 3 ms all 512 time slots are read sequentially from the IDB and the LLR. Both 8-bit words are converted to serial and compared in an Exclusive-OR circuit, bit by bit. If a bit has remained the same for two consecutive 3 ms scans it passes the hit timing algorithm.

F. Access to Received Data

2.12 The state of all signaling and control bits received by the SP from the TSI is stored after hit timing in an Immediate Access RAM (IAR). The IAR has the same data as the Last Report RAM (LRR). Through the IAR, the SMPU has access to the most recent hit timed state of all signaling and control bits of all time slots received by the TSI from the peripheral units.

G. Change Calculations

2.13 The SP is capable of storing (in an SMPU readable FIFO) all signaling and control bits whose state, after hit timing, has changed. The SMPU must specify on a per time slot basis which signaling and control bits of which time slot this change report is to be made. This allows the SMPU to ignore changes on certain bits of certain time slots.

2.14 State change calculations are based on the result of the hit timing circuit, the Ignore RAM, and the LRR. The Ignore RAM, set by the SMPU, indicates on which bits of which time slot state change reports should be made. The LRR contains the previously calculated states of all signaling and control bits after hit timing. If a new time slot bit has passed the hit timing algorithm (i.e., has not changed during the last 3 ms), it is compared to the state stored in the LRR. If a change has occurred, the LRR is updated. If the bit being processed is not set to ignore in the Ignore RAM and there is a change from the state contained in the LRR, the new bit value is written into the Report FIFO. All changes for one time slot are collected before the FIFO is written. The FIFO is readable by the SMPU.

H. Sourcing Data

2.15 The signaling and control bits (A, B, C, D, E, F, and G) are transmitted to the TSI for all 512 peripheral side time slots every 125 usec. These signaling bits are read from a 512 time slot RAM designated as the M RAM. The M RAM is both writable and readable by the SMPU.

I. Dual Link Interface - FS 1,2

2.16 The Dual Link Interface (DLI) has been redesigned for the TSIU2. It is functionally the same as the DLI in the 5E1.2 version of the TSIU but has been reduced to one circuit pack (TN877) using LSI technology.

2.17 The DLI provides the interface to the Network Control and Timing (NCT) links for the SMPU-TSIU2. The DLI recovers clock and data from the incoming NCT links and distributes the resultant clocks and data to the TSIU2 and SMPU. In the opposite direction, the DLI receives outgoing data from the TSIU2 and SMPU, which is then multiplexed and sourced to outgoing NCT links. In each Interface Module (IM), there are two DLIs which operate in a master/slave (active/standby) configuration.

2.18 The DLI consists of two Link Interface (LI) circuits, a Clock circuit, and a Control circuit. Each LI interfaces with one pair of NCT links (outgoing and incoming) which provide 256 time slots to and from the IM. Of these 256 time slots, 255 time slots are for voice and data paths to and from the TSIU2 with the remaining

time slot reserved for communications between the Central Processor and the SMPU (this time slot is referred to as the Message Time Slot). The incoming 32.768 megabit/second data stream from the NCT link enters the Receive (RCV) circuitry in the LI where it passes through a Clock Recovery circuit which derives a 32.768 MHz clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the Phase Lock Loop (PLL) in the Clock circuit. The RCV circuit "frames up" on the incoming data stream via a pseudo-random sequence inserted into the data stream at the source end of the NCT link (the TMS in a multimodule office and the MICU in a single module office). The incoming data stream is then converted to time slots and written into the BUFFER circuit (a RAM capable of containing one frame of data).

2.19 The TSI Interface and Message Interface operate from clocks derived from the output of the PLL (these are the same clocks sent to the TSIU2 and SMPU by the DLI). When time slots are read from the BUFFER, parity is checked and regenerated. Normal voice and data time slots are sent to both TSIs via nibble busses operating at 8.192 megabits/second. The Message Time Slot is sent to both the active and standby sides of the SMPU via serial data links to the Synchronous Data Link Controller (SDLC). These data links operate at 48 kilobits/second.

2.20 In the return direction, data is selected from one of the TSIs at the TSI Interface and from one side of the SMPU at the Message Interface for transmission to the TMS (or MICU in a single module office) via the outgoing NCT link. These time slots are then multiplexed to provide a full frame of 256 time slots. In the Transmit (XMIT) circuit, parity is checked and regenerated. The pseudo-random framing sequence, which is generated in the Control circuit, is inserted (one framing bit per time slot). Finally, the time slots are converted to a 32.768 MHz data stream and transmitted over the outgoing NCT link.

2.21 The Clock circuit selects a clock reference from one of the two LIs (master mode) or from the mate DLI (slave mode). This selected clock is used as a reference for the PLL which, in turn, provides a reference voltage to the Voltage Controlled Crystal Oscillator (VCXO). The output of the VCXO is a 32.768 MHz clock which is divided by the Clock circuit and distributed to the remainder of the DLI, the mate DLI, the TSI, and the SMPU.

2.22 The Control circuit provides control for the various functions performed by the LIs and Clock circuit. Errors from these circuits are latched into Error Source Registers (ESRs) which reside in the Control circuit. These control registers and ESRs are accessible for writing and reading by either side of the SMPU via the SMPU-DLI Control Interface. This interface is a 1.875 MHz serial data link. The data bits which make up the commands are clocked in by a clock which is provided by the SMPU and the command is executed upon the reception of a "go" signal received over a separate lead from the SMPU. Parity over address and parity over data is checked in the Control circuit. The Control circuit provides a serial data link back to both sides of the SMPUs for read operations and an interrupt lead back to both sides of the SMPU to indicate that an error condition exists. Each bit of the ESRs can be inhibited from causing an interrupt via ESR mask registers.

2.23 The Control circuit is contained in a custom NMOS device (328B).

The Clock circuit is implemented in SSI/MSI devices, along with the PLL and VCXO daughter boards which are used in the 5E1.2 version of the DLI (TN834 and TN835).

2.24 The circuitry which composes the RCV circuit and the portions of the TSI Interface and Message Interface that send data to the TSI and SMPU, is implemented in an LS1500 Functional Logic Array (FLA), code 374C. The XMIT circuits for both LIs and their corresponding portions of the TSI Interface and Message Interface are implemented in one LS1500 FLA (374B). The DLI is contained on a single TN circuit pack (TN877). Each DLI is in a failure group separate from the rest of the IM, and is powered by a separate power converter (494LA). In an RSM environment, the DLI includes the Facility Interface Unit (FIU). The power converters will interface to an SN412/SN516 Control and Display circuit pack.

J. Data Interface - FS 5,6,7,8

2.25 The Data Interface function has been reduced to a single TN circuit pack for the TSIU2. Cost reduction has been achieved by developing a custom bipolar LSI integrated circuit (358A). Two of these custom devices are used on the TN876 to realize the same function as the TN836/TN837 circuit packs. The operation of the Cost Reduced DI is identical to that of the previous design.

2.26 The Data Interface (DI) interfaces the TSI to the various Peripheral Units that may be attached to the IM. In the incoming direction, it performs a multiplexing function by combining the time slot traffic of several Peripheral Units onto a single bus for the TSI, and in the outgoing direction, demultiplexes a single bus from the TSI to the various Peripheral Units.

2.27 The DI communicates with each Peripheral Unit over a Peripheral Interface Data Bus (PIDB). Each of these busses consists of four signals; serial data in, serial data out, a 4.096 MHz clock, and an 8 KHz sync. The data in and out operate at 4.096 megabits/second, carrying 32 time slots per frame, with 16 bits per time slot. Up to 16 PIDBs may be connected to the DI, with each PIDB carrying traffic to a service group in one of the Peripheral Units.

2.28 The DI passes data to and from the TSI over nibble busses. These busses operate at 8.192 megabits/second carrying 256 time slots per 125 usec frame (two DIs, each connecting 256 TSI time slots, are needed to carry traffic for the 512 time slot TSI). With 512 peripheral side time slots (16 PIDBs x 32 time slots) and 256 TSI side time slots, the DI can perform a 2:1 concentration function.

2.29 All PIDBs operate in synchronization, and in the time of a single PIDB time slot, eight time slots are sent and received from the TSI. After a single time slot from all 16 PIDBs has been clocked into the DI, up to eight of those are chosen, via control information received from the TSI, to be inserted into the eight time slots to the TSI. The time slots not selected are blocked and lost. If less than eight are chosen, "1s" are sent on the nibble bus to the TSI in the time slots for which no PIDB time slot was connected.

2.30 In the outgoing direction, the TSI provides eight time slots to the DI during a single PIDB time slot period. These eight time slots are connected, again using control

information received from the TSI, to eight of the 16 PIDBs. PIDBs not selected to receive TSI data transmit idle code to the peripheral units.

2.31 All eight TSI time slots need not be connected to a PIDB time slot. If less than eight are to be connected to PIDBs, the control information from the TSI associated with the "unused" TSI time slots informs the DI to ignore that incoming time slot. All unselected PIDBs transmit idle code. In this case, more than eight will do so.

2.32 In addition to the nibble bus in and out of the DI from the TSI, the DI also receives from the TSI an 8.192 MHz clock, an 8 KHz sync pulse, four address leads, a board select lead, and two leads used for diagnostics. The 8.192 MHz clock provides all the timing for processes internal to the DI, and also is used to generate the 4.096 MHz clock for the Peripheral Units. The 8 KHz sync pulse is used to properly synchronize the DI to the network and to generate the sync pulse to the Peripheral Units. The address leads indicate, on a per time slot basis, to which PIDB a given TSI time slot is to connect. The address is used by the DI both for the TSI to PIDB demultiplex function, and for the PIDB to TSI multiplex operation. The board select lead informs the DI, again on a per time slot basis, whether to connect the TSI time slot to the PIDB as determined by the address, or to ignore that time slot and make no connection to it. The diagnostic leads are used to loop data received from the TSI through the DI circuit and back to the TSI. These leads also provide the capability to have the DI loop idle code back to the TSI rather than the received TSI data. Maintenance of the DI, as well as the PIDB and parts of the Peripheral Units, is performed by the TSI via the walking parity scheme.

K. Control Interface - FS 9,10,11,12

2.33 The Control Interface (CI) has been redesigned for the TSIU2. Development of a single NMOS custom integrated circuit (327N) has made it possible to implement the CI function with a single circuit pack (UN71). The UN71 realizes the same function as the TN117/TN119.

2.34 The CI provides the control interface between the SMPU and the various Peripheral Units. This interface is used for control information to and from the SMPU. The peripheral interface is a Peripheral Interface Control Bus (PICB). Up to 23 PICBs are available with each CI. Either one or two CIs may be equipped in the TSIU2 providing a maximum of 46 PICBs. Each PICB contains five twisted wire pairs that carry clock, output data, input data, SMPU select information, and Peripheral Unit service requests.

2.35 The interface to the SMPU is via the SMPU Subunit Interface Bus. This bus is a parallel 16-bit bidirectional data bus with a 6-bit address bus. The CI contains a number of registers which are accessible by the SMPU via this bus.

2.36 The CI performs four functions for the SMPU:

1. Permits the SMPU to write 16 bits of information to a Peripheral Unit register (maximum of 256 destination registers)

2. Permits the SMPU to read 16 bits of information from a Peripheral Unit register (maximum of 256 source registers)

3. Receives, latches, and reports service requests from Peripheral Units

4. Detects and reports CI operational errors.

2.37 The CI reads and writes peripheral registers via an exchange of serial messages over the PICB. A distribute operation writes 16 bits of data into a Peripheral Unit destination register. A scan operation reads 16 bits of data from a Peripheral Unit source register.

2.38 The SMPU will initiate all scan and distribute operations. In all scan and distribute operations the Peripheral Unit will send a reply message back to the CI. In the reply message three is a 3-bit ASW code. These bits are used to report errors detected by the Peripheral Unit. If errors are detected during a scan or distribute order by either the CI or a Peripheral Unit, the error will be reported by latching a bit in the Error Source Register. The interrupt lead to the SMPU will become active if an error occurs. The ability to inhibit this interrupt on a per PICB basis is provided.

2.39 In addition to performing scan and distribute orders, the CI reports Peripheral Unit service requests by latching an active state on the PICB interrupt lead into the Interrupt Source Registers. Inhibit registers (Remote Interrupt Inhibit Registers) are provided such that these service requests may be handled by interrupts or polling.

3. INTERFACES

EXTERNAL INTERFACES

A. SMPU Subunit Interface Bus

3.01 The SMPU Subunit Interface Bus is used as the control interface to the TSI, SP, and CI from the SMPU. It utilizes a 16-bit bidirectional data bus and a 6-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two parity leads (bidirectional also), one each for the low byte and high byte of data. The parity is computed such that the sum of bits set to a logic one in each byte (including the parity bit) is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

3.02 There are five control leads to each subunit. Two of these, the Read and Write signals, are shared by all subunits. These two signals are used to distinguish between read and write operations to a subunit and are used by the selected subunit to gate the data to/from the data bus. The other three controls are Board Select, Ready, and Interrupt. Each individual subunit has separate Board Select, Ready, and Interrupt leads. The Board Select enables the desired subunit, the Ready lead is used by the subunit to extend the SMPU bus cycle for subunits with slower response time, and the Interrupt lead is used by the subunit to interrupt the SMPU.

3.03 In addition, the CIs receive a lead called NAE which is used to force the Select wire pair in the PICB on the nonactive side to a nonconductive state.

B. NCT Link Interface

3.04 The serial data received and transmitted over the NCT links is at a 32.768 MHz rate. The DLI will track the received serial data up to ± 1 KHz of the nominal frequency (± 32 PPM). Each frame consists of 256 16-bit time slots. Bits 0 through 7 are PCM data bits in the 255 voice and data time slots. Bits A through E are signaling bits. The G bit is the bit position into which the pseudo-random

framing sequence is inserted. The F bit is toggled at the beginning of each frame and is used for fault detection in the DLI/TMS interface (in a multi-module office) or the DLI/MICU interface (in a single module office). The P bit is such that the 16 bits of the time slot have odd parity. In the Message Time Slot, bits 0 through 5 are the data bits which contain data to/from the SMPU and bit 7 is the Central Processor Intervention (CPI) bit.

C. SMPU Message Interface

3.05 After the Message Time Slot has been extracted from the normal data path through the LI, parity is checked and generated over the six bits that will be sent over the 48 KHz data links to the SDLCs in both sides of the SMPU. The generated parity is also sent to the SDLCs in both sides of the SMPU over separate data leads. At the same time, the CPI bit is sent to the CPI gate arrays in both sides of the SMPU. Two clocks are sent to both sides of the SMPU from the Clock circuit in the DLI. These clocks are used by the SMPU to clock the received Message Time Slot data and parity into the SDLCs. In the return direction, the SMPU uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each LI contains a Message Interface to and from both sides of the duplex SMPU.

D. SMPU-DLI Control Interface

3.06 The SMPU-DLI Control Interface is composed of three signal leads and one clock lead from each side of the SMPU to the DLI and two signal leads from the DLI to each side of the SMPU. A control lead originates from each side of the SMPU to indicate which side is sending commands to the DLI. Another control lead comes from each SMPU side to control when a read or write command is executed by the DLI. A 1.875 MHz clock is sent by each SMPU side along with the data which specifies the command to be executed. The entire write operation is specified in a serial 16-bit command in which the first eight bits contain the data to be written, followed by a spare bit and a parity bit for the eight bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four address bits which specify the register to be written. During a read operation, only six bits are sent by the SMPU to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits which determine the register to be read. Following the execution of the read command as initiated by the MPGO signal, eight bits of data plus one parity bit (parity over the data) are sent back to both sides of the SMPU on separate signal leads with the results of the read operation. Interrupt leads that indicate error conditions exist in the ESRs of the DLI are also a part of the SMPU-DLI Control Interface. These signals are asynchronous to the SMPU and have no specified timing relationship.

E. Peripheral Interface Data Bus

3.07 A Peripheral Interface Data Bus (PIDB) provides the physical link for traffic between the DI of the IM and any Peripheral Unit connecting to the DI. It consists of four balanced, differentially driven, RS422[2] compatible twisted wire pairs.

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2. EIA (Electronic Industries Association) RS-422 standards for balanced voltage digital interfaces.

3.08 The PIDB carries a 4.096 megabit/second serial data from the DI to the Peripheral Units, a 4.096 MHz clock and 8 KHz sync to the Peripheral Units, and 4.096 megabit/second serial data to the DI from the Peripheral Units. The twisted pair carrying data from the periphery is terminated at the DI. The PIDB cable may vary in length but has a maximum limit of 20 feet.

3.09 The 4.096 MHz clock has a 244 ns period. The low or high portion of the 4.096 MHz clock may change ±20 ns for a single cycle at any time due to a DLI clock reference switch at the TSI. The duty cycle of the clock, excluding this ±20 ns is 50% ± 5%. The 8 KHz sync is a normally high signal ("1" state) that pulses low for one 4.096 MHz clock period every 125 us. If the clock switch occurs during the 8 KHz sync pulse, the duration of the pulse may also change ±20 ns.

3.10 The Peripheral Units should clock PIDB data in from the DI on the falling edge of the 4.096 MHz clock, and clock data out onto the PIDB on the rising edge of that clock.

3.11 During the sync pulse, the peripheral should clock PIDB time slot No. 29, bit 7 in from the PIDB on the negative edge of the 4.096 MHz clock and clock out PIDB time slot No. 31, bit 15 onto the PIDB using the positive edge of the clock. Note the 2 1/2 time slot skew between incoming and outgoing information - this is due to the skew required by the TSI and DI to perform their functions.

3.12 A Peripheral Unit service group will receive a PIDB from each side of the duplex TSIU2. In a fully operational IM, data will flow over both PIDBs. Using control information received from the SMPU via the CI, the peripheral unit will select only one PIDB to receive information from. However, it will transmit the same data back over both PIDBs. The skew of the two PIDB clocks received from the duplex IM can be up to ±80 ns.

F. Local Digital Service Unit (LDSU) Interface

3.13 The TSIU2 communicates to the Local Digital Service Unit (LDSU) over two dedicated serial ports connected to the TSI. The TSI transmits and receives 32 serial time slots to and from each of two service groups in the LDSU. Any of these 64 time slots can be selected as a source of PCM data for any time slot going to the DLIs or DIs. Similarly, the TSI can send the 16-bit word of any time slot received from the DLIs or DIs out on any of the 64 time slots to the LDSU. The data format and timing of the LDSU interface is of the PIDB type consisting of four balanced, differentially driven, RS-422 compatible twisted pair wires. Signals provided by this interface are a 4.096 MHz clock out, an 8 KHz sync pulse out, 32 time slot serial output data, and 32 time slot serial input data.

3.14 The twisted pairs carrying data from the LDSU to the TSI are terminated with a discrete resistor providing a differential mode termination of 220 ohms and a common mode termination of 55 ohms. The 8 KHz sync pulse is normally "high", and goes "low" for one clock period (244 nsec) every frame (125 usec). The clock period can change ±20 nsec for one period during a DLI clock reference switch by the TSI. Both data and sync (if sync is coincident) will reflect the period change of the clock switch.

3.15 In a normally functioning Interface Module each service group in the LDSU will receive two of the PIDB like interfaces described above, one from each side of the duplex

TSI, with only one active at any given time. Identical data will be present on both busses to a given service group.

G. Peripheral Interface Control Bus (PICB)

3.16 A PICB cable consists of 5-wire pairs which are used for balanced data transmission and signaling. The Clock pair carries a 2.048 MHz gated clock signal to the Peripheral Units, the Data Out pair carries serial information to the Peripheral Units from the CI, the Data In pair carries serial data from the Peripheral Units to the CI, the Select lead carries signaling information which is used to select the active side CI, and the Interrupt pair is used to transmit service requests from the Peripheral Units.

3.17 The cable length of the PICB may vary but has a maximum limit of 20 feet.

3.18 Data is to be gated in and out of the Peripheral Unit on the negative edge of the clock. The reply must be received by the CI within 21.5 usecs from the first clock pulse to avoid a timeout error.

INTERNAL INTERFACES

A. Time Slot Interchanger - Data Link (TSI-DLI) Interface

3.19 The TSI transmits the 512 DLI time slots to both DLIs in the TSIU2. In the opposite direction, the TSI provides a switch, set under SMPU control, to select the 512 DLI time slots from one of the two DLIs. This provision allows the TSI to be configured to receive its time slots from the active DLI, and under normal (no fault) conditions, switch between the two DLIs, on a per time slot basis, without introducing data errors. The interface consists of two 256 time slot busses to and from each DLI. Each bus transmits 16-bit words made up of four consecutive 4-bit nibbles. The parity bit is set such the sum of bits (including parity) set to a logic one is odd. Each DLI supplies the TSI with an 8.192 MHz clock, an 8 KHz sync pulse, and a 6 msec sync pulse in addition to data. The TSI is required to perform an error free switch when selecting a DLI timing source. To accomplish this switch the maximum DLI clock skew between the duplicated DLIs can not exceed 20 nsec.

B. Time Slot Interchanger - Signal Processor (TSI-SP) Interface

3.20 The TSI sends the seven signaling bits (A-G) of all 512 time slots received from the DIs to the Signal Processor. The time slots consist of two consecutive 4-bit nibbles and are accompanied by an 8.192 MHz clock and a 6 msec sync pulse. In the opposite direction, the TSI receives the seven signaling bits (A-G) from the SP for all 512 outgoing peripheral time slots. Of these seven bits received, the E, F, and G are always sent toward the DIs. The A through D bits are selectable as a group. They can either be passed through the TSI from the DLI or can be selected to be sourced by the SP. Even parity is used on the even time slot bytes and odd parity is used on the odd time slot bytes.

C. Time Slot Interchanger - Data Interface (TSI-DI) Interface

3.21 The interface between the TSI and the DI consists of a nibble bus in each direction carrying call traffic, control information from the TSI to the DI, clock, and sync.

3.22 Two DIs may be connected to the TSI (1 even, 1 odd), each supplying 256 time slots in nibble format.

3.23 The nibble busses carry a time slot on four consecutive nibbles, and operate at 8.192 megabits/second. Two hundred and fifty-six time slots per frame are transmitted in each direction to each DI. These busses employ a walking parity scheme for fault detection. In this scheme the parity is normally odd but in every ninth time slot the parity is even.

3.24 The control information includes a 4-bit PIDB address that selects the source and destination for the 512 time slots associated with the DIs. Also, in the control information is a DI board select lead. This lead informs the DI to connect the TSI time slot with which it is associated to the specified PIDB, or to ignore the time slot and make no PIDB connection to it.

3.25 Two additional leads are used to diagnose the DI. One of these leads informs the DI to loop the TSI data received on that time slot through itself and back to the TSI on the same time slot of the next frame. The other has the DI replace the received TSI data with PIDB idle code.

3.26 The clock lead nominally is an 8.192 MHz clock (122 ns period). The 8 KHz sync is a normally "high" signal with an active "low" pulse of one 8.192 MHz period in duration occurring every 125 us (once per frame).

UNIT LAYOUT

3.27 A 150 watt, 2-inch, 495FB BELLPAC power converter is used to provide +5 volt power to all circuits except the DLIs. The DLIs will use a 5 volt - 50 watt, 12 volt - 5 watt 1-inch, 494LA BELLPAC power converter. A spare slot has been provided in the lower shelf for possible test access in the future, and a spare slot on each side of the top shelf is also available for future use. A slot on each side is also reserved for an SDLC link monitor.

3.28 In its fully equipped state the CRTSIU will contain the following:

TSIU2

Pack Code	Quantity	Description
TN315/TN315B	2	Time Slot Interchange
TN866	2	Time Slot Interchange
TN887	2	Time Slot Interchange
TN127/TN127B	2	Time Slot Interchange
TN865	2	Time Slot Interchange
TN214	2	Signal Processor
TN213	2	Signal Processor
TN212	2	Signal Processor
TN876/TN1129	4	Data Interface
SN412/SN516	4	Control and Display
TN887	2	Dual Link Interface
UN71/UN71B	4	Control Interface
495FB	2	2" Power Converter
494LA	2	1" Power Converter

Note:

1. For Revertive Pulsing Capabilities, replace TN127 and TN315 circuit packs with TN127B and TN315B respectively.

2. In setups requiring A-law, replace circuit packs TN315 and TN876 with TN315B and TN1129 respectively.

3. SN 516 is a replacement for the SN412 Control and Display circuit pack.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

A. Voltages

1.01

a. +5±0.5 volts

b. +12±1.2 volts

B. Ambient Temperature

1.02

a. 0% to 70% Centigrade (at circuit pack).

b. 0% to 50% Centigrade (office aisle ambient).

C. Growth

1.03 Each side of the TSIU2 comes equipped with 36 PIDBs and 23 PICBs. The unit may be expanded by adding another Control Interface to each side, for a total of 46 PICBs per side.

2. FUNCTIONAL DESIGNATIONS

FDESIG	MEANING
0CI0	Side 0, Control Interface 0
0CI1	Side 0, Control Interface 1
1CI0	Side 1, Control Interface 0
1CI1	Side 1, Control Interface 1
0DI0	Side 0, Data Interface 0
0DI1	Side 0, Data Interface 1
1DI0	Side 1, Data Interface 0
1DI1	Side 1, Data Interface 1
DLI0	Side 0, Dual Link Interface
DLI1	Side 1, Dual Link Interface
OPTRCV	Receive Fiber Link to DLI
OPTXMIT	Transmit Fiber Link from DLI
SP0	Side 0, Signal Processor
SP1	Side 1, Signal Processor
TSI0	Side 0, Time Slot Interchange
TSI1	Side 1, Time Slot Interchange
0C/P	Side 0, Control and Power
1C/P	Side 1, Control and Power
0DLIC/P	Side 0, DLI Control and Power
1DLIC/P	Side 1, DLI Control and Power
0TSSDLIA	Side 0, Time Slot Switch for DLI Link A
0TSSDLIB	Side 0, Time Slot Switch for DLI Link B
1TSSDLIA	Side 1, Time Slot Switch for DLI Link A
1TSSDLIB	Side 1, Time Slot Switch for DLI Link B

3. FUNCTIONS

3.01 Provides a time division switch under control of the SMPU.

3.02 Performs preprocessing on the signaling and control bits of the time slot data and provides the SMPU access to them.

3.03 Provides the interface to the NCT links.

3.04 Provides an interface to the Peripheral Units for control information from the SMPU.

3.05 Provides an interface to the Peripheral Units for PCM data.

3.06 Provides the SMPU with an interface to the Message Time Slots of the NCT links.

4. CONNECTING CIRCUITS

4.01 Switching Module Processor Unit - SD-5D129

4.02 Time Multiplexed Switch Unit - SD-5D043

4.03 Peripheral Units

1. Line Unit - SD-5D051
2. Trunk Unit - SD-5D300
3. Digital Line and Trunk Unit - SD-5D201
4. Metallic Service Unit - SD-5D033
5. Digital Service Unit - SD-5D035

5. MANUFACTURING TESTING REQUIREMENTS

See DS5U 1.04.01.00 Cost Reduced Time Slot Interchanger Unit, Hardware Unit Test Plan, Design Specification Case 40288-600 Issue 1, L. K. Temple, IX 55617, 55617-821215.01DS

SECTION IV - REASON FOR REISSUE

B. Changes in Apparatus

B.01 Revertive Pulsing -- replaced circuit packs TN127 and TN315 with TN127B and TN315B respectively, as per apparatus Figure 2.

B.02 A-law -- replaced circuit packs TN315 and TN876 with TN315B and TN1129 respectively, as per apparatus Figure 2.

D. Description of Changes

D.01 Changed LDI WIM from class D to class AC to accelerate the change from 495G1 and 494L1 prototypes to 495FB and 494LA production converters.

D.02 Added the FIU to the DLI service group in an RSM. This adds a terminal field and a 2x12 cable to the FIU. This SN412 in the DLI service group also controls the FIU power converter in this environment. Options V (standard wiring) and T (RSM application) are added.

D.03 Eliminated problems in fault recovery and maintenance associated with the SN412 RQ1P and OSS lamps and insured the compatibility of future 495FB power converters with TSIU2.

D.04 Updated CADs to show true destinations instead of "to connecting circuit."

D.05 Added new options for U-law circuitry with Revertive Pulsing (Option N) 5E2(1) generic. Standard U-law wiring is Option P. A-law wiring without Revertive Pulsing is Option M.

D.06 Added optional wiring to accommodate SN516 Control and Display circuit pack replacement of SN412. Option E-Basic unit equipage with SN516. Option J-Unit wiring for non-RSM SN516. Option G-unit wiring for RSM SN516.

D.07 Removed the optional A-law circuitry and Revertive Pulsing 5EE1 generic specified in LDI 1B.

D.08 Corrected errors in the feature and option table, terminal numbers, and net names. Renamed the information notes.

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