5ESS® SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

B. Changes in Apparatus

The following changes are documented for International features:

1. The SMP12 Split Memory wiring option with added 8Mbyte memory pack TN1409.
2. The SMP23 Split Memory wiring option with added 8Mbyte memory pack TN1409.
3. The SMP23X Split Memory wiring option with added 16Mbyte memory pack TN1419.
4. Introduction of the Terminator Paddle Boards for the SMP23 with Split Memory.

D. Description of Change

1. Change B.1 transmits wiring information to rewire seven 2Mbyte board selects to the two memory slots which are reserved for the TN1409. The TN1409 is used in emulate mode as 4x TN56. This change increases the memory of the SMP12 unit with the TN1527 memory controller from 16Mbyte to 32Mbyte with 8x TN56 and 2x TN1409.
2. Change B.2 transmits wiring information to add address lead A22I1 and the 8MB0 board indicator for the TN1409. The TN1409 is used in the normal 8Mbyte select mode. To support the TN56 and TN1409 split mode the A19202II0 address multiple is removed from memory locations above 16Mbyte and a new switchable A2021I0 address lead is added. (A20I0 for TN56 and A21I0 for TN2012/TN1409) The address leads A02IB1 and A02IB0 have also to be rewired for the memory locations above 16Mbyte to the nets A02I1 and A02I0, respectively. These two nets are reused by the TN1408 for A22I1 and 8MB0 due to a lack of spare pins on the TN1408. This change increases the memory of the SMP23 unit with the TN1408 memory controller from 16Mbyte to 32Mbyte with 8x TN56 and 2x TN1409.
3. Change B.3 transmits wiring information to extend the address lead A22I1 and to rewire three 8Mbyte select leads to the two memory slots which are reserved for the TN1419. The TN1419 is used in emulate mode as 2x TN1409. This change increases the memory of the SMP23X unit with the TN1408B memory controller from 32Mbyte to 64Mbyte with 8x TN56, 2x TN1409 and 2x TN1419.
4. Change B.4 provides an AC-terminating of the address and control signals with Terminator Paddle Boards in the MEU. The TN1370 with DC-terminators and the Terminating Paddle Boards are mutually exclusive.

F. Changes in CD Sections

1. Add after paragraph 1.03
   TN1409 - 8 MBYTE DYNAMIC MEMORY

This memory pack is used in the SMP12 and SMP23[X] unit with Split Memory option. It provides 8Mbyte of Dynamic Memory with 80x 1Mbit DRAM chips. When selected the memory array permits memory read/write access or refresh cycles. A selected array returns 32 bit data, 8 bit parity/hamming code and a generated row/column address parity bit.
Besides the normal addressing mode the TN1409 is capable to emulate 2x TN2012 or 4x TN56.

2. Add after paragraph 1.03
TN1419 - 16 MBYTE DYNAMIC MEMORY

This memory pack is used in the SMP23[X] unit with Split Memory option. It provides 16Mbyte of Dynamic Memory with 40x 4Mbit DRAM chips. When selected the memory array permits memory read/write access or refresh cycles. A selected array returns 32 bit data, 8 bit parity/hamming code and a generated row/column address parity bit.
Besides the normal addressing mode the TN1419 is capable to emulate 2x TN1409 or 4x TN2012.

AT&T

DEPT NSI04018-JDV-SD

5ESS® SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 This change documents the wiring changes required for the SMP23 option in the MEU.

D. Description of Change

D.1 Both the GOIC and GOID terminations to the TN1370 pack have been removed and the A02I1 address lead have been added.

AT&T BELL LABORATORIES

DEPT NANW960570-CPP-MG

5ESS® SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 This change creates a backplane wiring option "ZB" in APP FIG. 1, and a minimum equipage option "ZC" in APP FIG. 2.

D. Description of Change

D.1 Options "ZB" and "ZC" are required in all MEUs to correct an unsatisfactory operating condition. APP FIG. 2, option "ZC", adds two TN1370 circuit packs in the unit; whereas APP FIG. 1, option "ZB", adds four wires associated with the added circuit packs. TN1370 is equipped in spare memory slots at locations 04-082 and 04-100. The TN1370 is used to terminate backplane signals.

AT&T BELL LABORATORIES

DEPT 55613-KTK-JCB

5ESS® SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 This change transmits circuit information required to allow the TN2012 4 Mbyte memory circuit pack into the unit. A total of 3 TN2012 circuit packs, per side, can now be equipped in the unit.

B.2 This change also transmits circuit information required for the expanded application of the TN56 circuit pack. A total of 7 TN56 circuit packs, per side, can now be equipped in the unit.

D. Description of Changes

D.1 This change expands the use of the Memory Expansion Unit. In the MEU, the TN56 circuit pack can expand the Switch Module Processor's memory from its current size of 16M to a total of 24M. In the MEU, the TN2012 circuit pack can expand the Switch Module Processor's memory from its current size of 20M to a total of 32M.

AT&T BELL LABORATORIES

DEPT 55613-KTK-JCB

CD-5D048-01
ISSUE 2A
APPENDIX 1AC
DRAWING ISSUE 3AC
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added five wires to each of sides 0 and 1 of the MEU (memory expansion unit). This wiring change facilitates interconnection between the MEU and MCTU (module controller and time slot interchange unit).

D.2 Added apparatus options to accommodate the TN56 memory planes.

D.3 Removed Options W through Q since only three memory packs can be added per memory controller.

D.4 Revised CADs 006 and 007 to show cabling between the MEU and MCTU (Option J), and between the MEU and the SMPU2 (Option K). (The SMPU2 is the switching module processing unit, Model 2.)

F. Changes in Description of Operation

F.1 In the last line of paragraph 1.04, Page 1, change "120 volts" to read: 120 watts.

AT&T BELL LABORATORIES

DEPT 55613-CAH-JCB

CD-5D048-01
ISSUE 2A
DWG ISSUE 2A
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT
MEMORY EXPANSION UNIT
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The memory expansion unit (MEU) is a duplex unit which provides the interface module processor - model 2 (IMPU2) with an extended data bus to support more memory. It is located in the interface module of the 5ESS™ switching system.

2. GENERAL DESCRIPTION OF OPERATION

The MEU's function is to provide up to six additional megabytes of memory to the IMPU2 when equipped with the TN28 memory planes. When equipped with the TN56 memory plane, the MEU can be used to provide a maximum of up to 16 megabytes of memory for the IMPU2.

SECTION II - DETAILED DESCRIPTION

1. Functional Designations

1.01 The MEU has only one function, the extension of the memory bus. There are two FS numbers associated with the MEU. FS 1 is side 0 of the MEU, and FS 2 is side 1 of the MEU.

A. Functions

1.02 The function of the MEU can be divided into two subfunctions; the memory planes and the power converter.

1.03 Memory Planes - The memory used is either the TN28 memory plane or the TN56 memory plane. The TN28 memory plane is 1024K bytes, and the TN56 memory plane is 2048K bytes. The data on the memory planes is organized into 4-byte words with an additional 8 bits of hamming and parity associated with each work.

1.04 Power Converter - The power converter used is a 495FB power converter. The purpose of the converter is to provide a means of converting nominal -48 volt input to a well regulated and isolated +5 volt output for applications in the memory planes of the MEU. The power unit is pulse-width controlled for regulation, self-oscillating, and operated at a fixed frequency. The unit is also self protected by several types of alarms. The 495FB provides +5 volts @ 120 volts.

2. Interfaces

2.01 External Interfaces - All input and output points to the unit are listed in CAD 1. They are grouped by function and then alphabetized by net name.

2.02 Memory Data, Address, and Control (CAD 2, 3, 5, 6) - This bus connects all the memory planes of the MEU to the IMPU2's dynamic memory controller (TN875). It consists of the following:

(a) 40 bidirectional data leads. This is composed of 32 data bits (4 bytes) plus 8 bits of hamming and parity.

(b) When the MEU is equipped with the TN28 memory plane, it has 20 bidirectional address lines plus two parity leads. There are 8-row address leads, 8-column address leads, a row parity and column parity lead, and four array selects to select a 64K array.

(c) When the MEU is equipped with the TN56 memory planes, it has 20-bidirectional address lines plus two parity leads. There are 9-row address leads, 9-column address leads, a row parity and column parity lead, and two array selects to select a 1M array.

(d) 14-memory control signals used for selecting memory boards, initiating memory cycles, controlling memory data bus direction, indicating refresh operations, strobing data into memory, and to provide upward compatibility with future memory board designs.

2.03 Control and Display Interface - The control and display scan points are connected to the MEU through an interface cable which runs between the time-slot interchange unit, the IMPU2 and the MEU.

2.04 Controller Power (CAD 8) - All controller power converters are connected to the fuse block via a hot lead -48V and a ground potential lead 48RTN.

2.05 Unit Layout - The MEU consists of a single shelf of circuit packs. The shelf is divided into duplicated halves, right and left side. The right half is an exact duplicate of the left, with the only exception the physical location. The physical location of each circuit pack is a mirror image of the other half, rather than maintaining the same physical relationship between circuit packs.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltages
-48 +4.5 -6.25 volts.

1.02 Ambient Temperature

0° to 70° centigrade (at circuit pack).

0° to 50° centigrade (office aisle ambient).

2. FUNCTIONAL DESIGNATIONS

FDESG	MEANING
0MSM09	Side 0, Main Store Memory Array board 1
0MSM12	Side 0, Main Store Memory Array board 2
0MSM15	Side 0, Main Store Memory Array board 3
0PC06	Side 0, Power converter
1MSM48	Side 1, Main Store Memory Array board 1
1MSM51	Side 1, Main Store Memory Array board 2
1MSM54	Side 1, Main Store Memory Array board 3
1PC81	Side 1, Power Converter

3. FUNCTIONS

3.01 The function of this unit is described in Section 1 of the Circuit Description.

4. CONNECTING CIRCUITS

4.01 Interface Module Processor Model 2 - SD5D129

4.02 Time-Slot Interchange Unit Model 2 - SD5D145

4.03 Fuse Panel - SD5D034

REFERENCES: Circuit Description,
Interface Module Processor
Unit Model 2 - SD-5D129-01

AT&T BELL LABORATORIES

DEPT 55614-DEH-CEJ