5ESS® SWITCHING EQUIPMENT
COMMUNICATION MODULE
CONTROL UNIT
CIRCUIT

Description of Changes

SD5D060-01 issue 14M replaces the SN516B circuit pack with the SN516C and adds associated cabling between the CMCU and all TMSUs. This change provides a method of applying and removing power to the CMCU and all TMSUs simultaneously, thereby ensuring Auto Power Recovery, and provides the alarm function for TMSUs through the CMCU for offices equipped with APR. The SN516C is located in the same position as the SN516B, and is ONLY downward compatible with the SN516B in offices that are NOT equipped with APR. The SN516C is a redesign of the SN516B to provide Auto Power Recovery and design out legacy components. Change includes update of company name to Lucent Technologies, Inc. The text in the circuit description is affected by this issue.

Lucent Technologies Inc

DEPT JC21B40A0-PMR-RJP

5ESS® SWITCHING EQUIPMENT
COMMUNICATIONS MODULE CONTROL UNIT
CIRCUIT

Description of Changes

SD5D060-01 issue 13M corrects documentation errors in the SD. It does not affect the text of the Circuit Description.

AT&T

DEPT NQ9250100-RMW-DWM

5ESS® SWITCHING SYSTEMS
COMMUNICATIONS MODULE CONTROL UNIT
CIRCUIT

Description of Changes

SD5D060-01 issue 12B adds two new NCLK2 packs to the CMCU for 64Kb/s applications. The TN1850 reference interface pack and the TN1851 NCLK2 controller. Sections 2.01, 2.09, 2.10, and 2.13 were updated and section 2.04.1 was added to include details on the new packs. Auto power recovery (APR) capability was also added to the CMCU. This allows the control and display pack to automatically power up the power converter if -48 volts to the unit is lost and then restored.

2.01 The NCLK2 consists of three fundamental circuit pack types: a controller (TN1276 or TN1851 for 64Kb/s applications), an oscillator (TN1283B, TN1284B, TN1285B, or TN1286B), and a reference interface (TN1274B, TN1275B, or TN1850 for 64Kb/s applications). Actually, two TN1275B circuit packs may be used if two analog references or more than four digital references are needed.

2.04.1 The reference interface circuit pack (TN1850) is required for 64Kb/s composite digital reference. One TN1850 provides two 64Kb/s digital references. A maximum of one TN1850 may be used in each CMCU.

NCLK2 CONTROLLER (TN1276 or TN1851)

2.09 The TN1276 circuit pack used for 30-channel and 24-channel reference applications or the TN1851 circuit pack used for 64Kb/s reference applications perform several NCLK2 functions. Being the controller for the NCLK2, the TN1276 or TN1851 handles communication with the FPC. It also contains a digital phase locked loop (DPLL) and performs calculations to vary the output frequency of the clock. The controller also diagnoses NCLK2 functions under control of the FPC.

2.10 The TN1276 or TN1851 compares one external reference to the signal from the NCLK2 oscillator. The controller then calculates a frequency difference. This difference information is then used to control the DPLL. By keeping the DPLL locked to the very stable NCLK2 oscillator and not directly to the external reference, high degrees of NCLK2 stability are possible.

NCLK2 REFERENCE INTERFACE (TN1274B, TN1275B, or TN1850)

2.13 As previously stated, the NCLK2 locks to external reference signals connected to the TN1274B, TN1275B, or TN1850 circuit packs. Timing information is extracted from the reference signal and is sent to the DPLL on the controller circuit pack.

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5ESS® SWITCHING EQUIPMENT
COMMUNICATIONS MODULE CONTROL UNIT
CIRCUIT

Description of Changes

SD5D060-01 issue 11B adds the TN1406 circuit pack as an option for the CMCU. The TN1406 is located in the same position as the TN881, and is downward compatible with the TN881. The TN1406 provides a 2.048 Mhz G703 75 ohm (CCITT) standard output signal on the CMCU backplane. This signal can be used to allow non-5ESS® equipment to synchronize on the 5ESS® clock.

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DEPT ND9250100-RMW-DWM

CD-5D060-01
ISSUE 2
APPENDIX 1B
DWG ISSUE 10B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT
COMMUNICATION MODULE CONTROL UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus

Replaced TN884C, TN1275B, TN1286B, TN1285B, TN1284B, TN1283B and SN516B circuit packs.

D. Description of Changes

The TN1275B, TN1286B, TN1285B, TN1284B, and TN1283B circuit packs provide additional circuitry for CEPT compliance. the TN884C circuit pack provides additional functionality for the feature switching module 2000 (SM2000). The SN516B circuit pack provides additional functionality for the auto power recovery feature.

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DEPT NA5360100-CEH-DJS

5ESS™ SWITCHING EQUIPMENT COMMUNICATION MODULE CONTROL UNIT CIRCUIT

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Communication Module Control Unit (CMCU) is divided into three main components: the Dual Message Interface, the Network Clock Model 2 and the Time Multiplexed Switch Controller.

1.02 The CMCU is only provided in the two basic cabinets (5 and 6). Unit 0 is located in cabinet 5 and unit 1 in cabinet 6. In the growth cabinets, the EBUS is used to provide the metallic path for the CMCU to communicate to every TMSU2.

2. GENERAL DESCRIPTION OF OPERATION

DUAL MESSAGE INTERFACE

2.01 The Dual Message Interface (DMI) provides a Control and Diagnostic Access Link (CDAL) from either Foundational Peripheral Controller (FPC) to the DMI, the Network Clock (NCLK2), and the Time Multiplexed Switch (TMS) Controller. This CDAL link enables the Administration Module (AM) to control and diagnose the DMI, NCLK, and TMS. The DMI also provides a metallic link into the TMS Fabric. This link is a bi-directional link that transfers the control time slot messages from/to the message switch to/from the Switching Modules (SMs).

NETWORK CLOCK, MODEL 2

2.02 The Network Clock, Model 2 (NCLK2) provides timing and synchronization signals to the 5ESS™ Switch network. NCLK2 features, not included in NCLK1, are: high-stability operation, multiple references, analog references, and 30-channel digital references. The Network Clock is a duplex circuit, that is, it is fully duplicated in each Communication Module Control Unit (CMCU) with some signals cross-coupled between the major and minor sides.

TMS CONTROLLER

2.03 The main purpose of the TMS Controller is to provide timing, control, and receive and transmit data to the TMSU2. The TMS Controller (TMC) consists of five circuit packs: TN884 (Controller), UN183 or UN321 (TMS2 Interface), TN881 (Clock Interface), TN882 (Control Interface Bus), and UN310 (Transmit Data).

2.04 TN884, UN183 (UN321 for single fabric growth bay) and TN882 provide the control interface and environment necessary for the TMS2 firmware to execute call processing. These boards also handle maintenance orders from the Central Processor (CP) and TMS2 internal operations (error and reporting, initialization, reinitialization).

2.05 The clock interface pack TN881 provides transmit clock signals and sync pulses to the fabric control (KBN2) packs on each TMSU2. It also provides receive clock signals to the UN182 Shelf Utility Board (SUB pack) on the TMSU2.

2.06 The UN310 Transmit Data pack transmits data time slots between the UN182 SUB board and KBN1 Fabric board.

SECTION II - DETAILED DESCRIPTION

1. DUAL MESSAGE INTERFACE HARDWARE DESCRIPTION

GENERAL HARDWARE DESCRIPTION

1.01 The Dual Message Interface consists of three codes of circuit packs: the transfer pack UN186, the receive pack TN1034, and the control pack UN187. There are two different configurations that the DMI can be used with: the single fabric configuration (UN186, TN1034, UN187) and the dual fabric configuration (2-UN186, 2-TN1034, UN187). For the single fabric case, a maximum of 256 control time slots are transferred on one metallic link. For dual fabric, a maximum of 512 control time slots are transferred on two metallic links (256 per link). In both cases, the UN187 controls the operation of the DMI.

DUAL MESSAGE INTERFACE 1 (UN186)

1.02 The UN186 is the transfer pack in the DMI functions; it sends clock, synchronization, and data from the TMS Fabric to the MSGS. The UN186 demultiplexes a 32MHz data stream to eight 4MHz data streams for the Message Module Processors (MMPs) in the MSGS. It has control and error source registers that control and detect errors on the board.

DUAL MESSAGE INTERFACE 2 (TN1034)

1.03 The TN1034 (DMI2) supplies (via a 32MHz serial metallic link) the TMS2 with data from eight cross-coupled communities of MMPs in the MSGS. DMI2 receives balanced serial data from the MMPs via the Message Interface Bus (MIB).

1.04 The DMI2 has 16 serial input buses. Two buses are associated with each MIB. Eight of these buses are associated with MMPs on the same MSG side and eight are associated with MMPs on the cross-coupled MSG side.

1.05 DMI2 has the capability to detect input parity errors from the MMPs and can force incorrect parity to the TMS. The DMI2 can also force errors, via control registers and detect them via ESRs. This allows the DMI2 to verify its error detection circuitry.

DUAL MESSAGE INTERFACE 3 (UN187)

1.06 The UN187 (DMI3) is the control interface for the DMI complex. It provides the serial interface to the Control and Diagnostic Access Link, which supplies a communication channel with either side of the Foundation Peripheral Controller (FPC) in the MSGS. The UN187 uses its time slot switching memory to configure the data paths received from the Module Message Processors (MMPs). It also can insert Central Processor Intervention (CPI) in one or all time slots.

2. NETWORK CLOCK MODEL 2 HARDWARE DESCRIPTION

GENERAL HARDWARE DESCRIPTION

2.01 The Network Clock - Model 2 consists of three fundamental circuit pack types: a Controller (TN1276), an Oscillator (TN1283, TN1284, TN1285, or TN1286), and a Synchronizer (TN1274B or TN1275). Actually, two TN1275 circuit packs may be used if two analog references or more than four digital references are needed.

2.02 One NCLK2 oscillator circuit pack is required in each CMCU, as follows:

a. TN1283 - export, high-stability, for gateway switches.

b. TN1284 - domestic, high-stability, stratum 2, for toll switches.

c. TN1285 - export, medium-stability, for local switches.

d. TN1286 - domestic, medium-stability, stratum 3, for local switches.

2.03 The synchronizer circuit pack (TN1274B) is required for 24-channel digital carrier (DS-1) synchronization. This provides a maximum of one analog input and two digital inputs in any combination. A maximum of one TN1274B may be used in each CMCU.

2.04 The synchronizer circuit pack (TN1275) is required for 30-channel digital carrier export synchronization. One TN1275 provides one analog input and four digital inputs with the restriction that a maximum of four of the five inputs be used simultaneously. A second TN1275 may be provided to add one additional analog input and four digital inputs with the same restriction that a maximum of four total inputs be used on each TN1275.

2.05 Analog references are restricted as follows:

a. TN1274B - Basic Synchronization Reference Frequency (BSRF) of 2.048MHz* with an input level of -27 dbm* to +10 dbm* into 75 ohms.

b. TN1275 - Frequency of 2.048MHz* with an input level of -13 dbm* to +10 dbm* into 75 ohms.

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* Input frequency is determined by both hardware and firmware. Input level is dependent only on the hardware and is independent of firmware.

NCLK2 OSCILLATOR (TN1283, TN1284, TN1285, OR TN1286)

2.06 The NCLK2 architecture uses a fixed frequency time base to perform its function of locking to the external references. The oscillator is oven enclosed in order to provide high stability. Four different codes of oscillator circuit packs are provided for various combinations of domestic, export, high-stability, and medium-stability as described in 2.02 of this section. Each NCLK2 oscillator is a unique failure group with independent power and alarms separate from other components in the CMCU.

2.07 Each NCLK2 oscillator output (one in each CMCU) connects to both NCLK2 Controllers (one in each CMCU). The Digital Phase Locked Loop (DPLL), on the Controller circuit pack, is instructed via the maintenance software as to which clock to use as its time base.

2.08 For stand-alone applications, the NCLK2 will not be synchronized to any external reference facilities. Instead, the NCLK2 will serve as the master timing reference for the 5ESS Switch. The stand-alone options are only provided for medium-stability applications.

NCLK2 CONTROLLER (TN1276)

2.09 The TN1276 circuit pack performs several NCLK2 functions. Being the Controller for the NCLK2, TN1276 handles communication with the Foundation Peripheral Controller (FPC). It also contains a Digital Phase Locked Loop (DPLL) and performs calculations to vary the output frequency of the clock. The Controller also diagnoses NCLK2 functions under control of the FPC.

2.10 The TN1276 compares one external reference to the signal from the NCLK2 Oscillator. The Controller then calculates a frequency difference. This difference information is then used to control the DPLL. By keeping the DPLL locked to the very stable NCLK2 Oscillator and not directly to the external reference, high degrees of NCLK2 stability are possible.

2.11 The DPLL provides the clock signal from which all Time Multiplexed Switch (TMS) timing pulses are derived. It also provides a cross-coupled output to the NCLK2 on the opposite side. Normal operation is for one NCLK2 to be active-major providing timing signals to the TMS and associated Quad Link Interfaces (QLI). The other NCLK2 is active-minor and is synchronized to the active-major side via cross-coupling, preventing errors in the 5ESS Switch network when active-major and active-minor clocks are switched.

2.12 The DPLL can be operated in four different modes: normal, fast, holdover, and free run. In the normal mode, the DPLL attempts to track the external references using the normal time constants for that particular application. In the fast mode, time constants are reduced to achieve a fast lock condition in the NCLK2. The holdover mode is entered whenever problems with the external references are detected. Here, the DPLL is no longer locked to the external references; instead, its signal is based on the last known good reference. In the free run mode, DPLL is instructed to free run in the center of its range. This is normally used only when the NCLK2 is initialized with no external references or for stand-alone operation.

NCLK2 SYNCHRONIZER (TN1274B OR TN1275)

2.13 As previously stated, the NCLK2 locks to external reference signals connected to the TN1274B or TN1275 circuit packs. Timing information is extracted from the reference signal and is sent to the DPLL on the Controller circuit pack.

2.14 The DPLL then generates the required 8KHz timing signal (locked to the reference) for use by

the TMS and QLI. For a master/slave network, where several references are used, the DPLL will lock to one of the external references. If that reference fails, the DPLL will be told to use the backup reference. If all external references are corrupted or lost, the DPLL will continue to provide the 8KHz to the TMS and QLI. In this holdover mode, the phase of the output signal is based on the last known good state of the reference. The stability of the clock during holdover will depend on the stability of the local NCLK2 oscillator.

3. TMS CONTROLLER HARDWARE DESCRIPTION

GENERAL HARDWARE DESCRIPTION

3.01 The TMS Controller consists of three fundamental circuit packs: TN884 Controller, UN183 (or UN321) TMS2 Interface Circuit, and TN882 Control Interface Bus. Two additional circuit packs are the TN881 Clock Interface and UN310 Transmit Data (used in this frame only when growth cabinets with EBUS are not implemented).

TN884 CONTROLLER

3.02 The TN884 Controller operates as a microprocessor-based core to maintain and set up the TMSC (TMS Control) and TMSU (TMS Switch Units) for the functions described in 2.03 of SECTION I.

3.03 The TN884 consists of a 68000 microprocessor supported by 48 kbytes of static RAM, 64 kbytes of EPROM, a D71054 programmable timer, a 9519A programmable interrupt controller, maintenance and error source registers, and other circuitry for address decoding, data flow, and other lower level functions.

3.04 The EPROM stores TMS firmware, including a bootstrap program that initializes the TMSC in response to a reset. The RAM stores these TMS firmware program variables and the TMS diagnostic program and its variables. Part of the RAM is dedicated to other diagnostic programs delivered from the Message Switch (MSGS).

3.05 The D71054 programmable timer provides a timing for regular interrupts to the 68000 processor and serves as its sanity timer.

3.06 The 9519A programmable interrupt controller provides a way of prioritizing and allowing or disallowing TMS internal interrupt sources.

3.07 The error source registers provide maintenance and control functions on- and off-board.

3.08 The TN884 connects to the UN183 (or UN321) and TN882 over a common parallel address, data and control bus. The TN884 connects to the TMSUs via the TN882.

UN183 (OR UN321) TMS2 INTERFACE

3.09 The purpose of the UN183 (UN321) is to provide the actual hardware communication link between the TMSC and the TMS Switch Units (TMSUs).

3.10 For the single fabric growth bay configuration only, the UN183 is replaced by the UN321 board in the base bay.

TN882 CONTROL INTERFACE BUS

3.11 The TN882 Control Interface Bus (CIB) provides one end of the serial link that allows the Communication Module Control Unit (CMCU) to communicate with the Time Multiplexed Switch Unit (TMSU). The key component on the CIB board is the Control Interface Chip (CIC). This chip provides a transparent extension of the Motorola 68000 bus by converting the parallel address, data, and control leads of the microprocessor into two serial streams and sending them to a peripheral board in the TMSU. In the similar way, the serial stream from the TMSU peripheral board is converted back into parallel and put on the microprocessor's own bus.

3.12 The TN882 board also provides translation between the TTL microprocessor and the ECL Control Interface Chip, buffering, and bi-directional control for the shared data bus.

TN881 CLOCK INTERFACE

3.13 The TN881 provides system timing for the TMS2 through the generation of the various clocks and synchronization pulses, which are distributed throughout the CMCU and associated TMSUs. System synchronization is accomplished by phase locking the oscillator on the TN881 to an 8KHz reference signal. All errors detected by the TN881 are reported to the TMS Controller.

UN310 TRANSMIT DATA

3.14 The UN310 Transmit Data pack taps the data Time Slots from the UN182 Shelf Utility Board and distributes them to a KBN1 Fabric board.

3.15 The UN310 is only provided when there are no CM2 growth cabinets.

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SECTION III - REFERENCE DATA

1. WORKING LIMITS

TEMPERATURE RANGE

- 0 to 50 degrees C office aisle ambient.
- 0 to 65 degrees C at NCLK2 Circuit Pack.
- 0 to 70 degrees C at all other Circuit Packs.

VOLTAGE LIMITS

- -41.75 to -52.5 volts static.
- -41.75 to -60.0 volts transient.

NETWORK CLOCK CABLING

- Maximum distance from DSX to NCLK2 is 655 feet (CAD 12).
- Maximum distance from NCLK2 cross-couple is 35 feet