5ESS® SWITCHING EQUIPMENT
TIME MULTIPLEXED SWITCH UNIT
MODEL 2
CIRCUIT

CONTENTS

LIST OF FIGURES

1. GENERAL DESCRIPTION

This section provides a high-level view of the time multiplexed switch unit model 2 (TMSU2).

1.1 PURPOSE OF CIRCUIT

The TMSU2 provides the physical paths which carry data and control messages between the switching modules (SMs) and the administrative module (AM). Major functions of the TMSU2 are to:

1. Provide a fixed control path between the AM and its associated SMs.
2. Provide switched data paths between the SMs connected to the time multiplexed switch (TMS).
3. Provide for clock distribution to the SMs by transmitting data timed from a clock which is derived from a reference clock.
4. If equipped with a quad link packet switch (QLPS), provide for inter-SM2000 communication on variable size pipes.

1.2 GENERAL DESCRIPTION OF OPERATION

The TMSU2 is connected to the SMs (either SM-2000s or non-SM-2000s) through the network control and timing (NCT or NCT2) links which terminate on the foundation link interface (FLI) board or quad link interface (QLI) boards, in the case of the NCT links, or quad link interface 2 boards (QLI2) in the case of NCT2 links. For the purpose of clarity, the FLI, QLI, and QLI2 circuit packs will be referred to here as link interface (LI) boards. Data from the SMs is buffered by the LIs before being sent to the shelf utility board (SUB) where it is multiplexed up to a 64Mbit rate and placed on the emitter coupled logic bus (E-bus). The E-Bus distributes clock and data signals to/from all switch units in the TMS.

Data received from the E-Bus is switched through the fabric board multiplexers and routed back to the appropriate link interface board. The LI checks the data for errors and sends it out to a receiving SM through the NCT/NCT2 links.

2. DETAILED DESCRIPTION

The TMSU2 is wired to accept the following circuit packs:

CIRCUIT PACK	DESIGNATION	QNTY.
SN516B	CONTROL & DISPLAY	1
495MA	-2 VOLT POWER	1
410AA	-5 VOLT POWER	2
TN883	FOUNDATION LINK INTERFACE	1/0
TN888	QUAD LINK INTERFACE	7/8
TN1681	QUAD LINK INTERFACE 2	7/8
TN1682	QUAD LINK PACKET SWITCH	0/1/2/3/4
UN182	SHELF UTILITY BOARD	1
KBN4	FABRIC	3
KBN2	FABRIC CONTROL	2

The circuit pack layout is shown in Figure 1.

The TMSU2 is divided into 4 circuit elements with the control paths described in Element A. Element B details the clock distribution. Data distribution is explained in Element C and power distribution in Element D. The QLPS is described in Element E.

2.1 ELEMENT A: CONTROL

2.1.1 COMMUNICATIONS

The control structure of the TMSU2 is illustrated in Figure 2. The TMS controller resides in the CMCU and interacts with each TMSU2 through the SUB board (UN182). Communications with the switch unit are accomplished through the use of a control interface chip (CIC) which converts the parallel address and data buses from the processor to serial address and data streams. These serial streams are distributed through the E-Bus to the SUB boards located in each TMSU2.

The SUB is responsible for distributing the serial address and data to the switch unit. Serial data returning from the switch unit flows in exactly the opposite direction with the SUB board collecting the serial streams from each circuit pack before sending data back to the controller. A multiplexer on the SUB selects which serial stream from all the various circuit packs is to be sent back to the controller. Control for the SUB multiplexer originates at the TMS controller and is derived from the address that the controller wishes to read.

2.1.2 ERROR REPORTING

Error reporting of TMSU2 is accomplished asynchronously through a pyramid error reporting architecture where errors are reported to the controller in the form of an error summary lead. Each circuit pack in the switch unit produces a collection center for these summary errors and produces a *switch unit error summary* used to interrupt the TMS controller and invoke its error handling routines. When an error is detected, the TMS firmware will search through the error reporting hierarchy in hopes of finding the source of the interrupt.

2.1.3 FABRIC CONTROL

Control for the TMS fabric multiplexers is not provided directly by the TMS controller, but rather the KBN2 circuit pack. The TMS controller sends connection information to the KBN2 board, which in turn configures the fabric multiplexers located on the fabric and LI circuit packs on a per time-slot basis. The distribution of this control is illustrated in Figure 2.

2.1.4 SHELF SELECT

Since a fully grown TMS contains 12 TMSU2s, a shelf select bus is used to identify the address range of each shelf. The bus is tied to all of the circuit packs on the shelf that perform address decoding and allows for the high-level decoding to be dependent on the state of the leads in the shelf select bus. A programming paddle-board located behind the last KBN2 pack determines the state of the shelf select bus and thus determines the shelf identification. With the high-level address decoding performed by the shelf, and not by the circuit pack, TMS circuit packs can be moved between shelves while only maintaining their "base" addresses.

2.2 ELEMENT B: CLOCK

All clocks used in the TMSU2 originate from the E-Bus. The clocks themselves are designated as either "receive" or "transmit", depending upon whether they are being used to clock data onto or from the E-Bus. Clock distribution throughout the TMSU2 is shown in Figure 3.

Receive clocks are used by the LIs to send received data from the SMs to the SUB and onto the E-Bus. As with the case of serial address and data, the LIs acquire their receive clocks from the SUB board, which serves as a distribution point. A secondary function of the receive clock is to clock the incoming serial address and data streams from the TMS controller. It is for this reason that the KBN2 boards are also supplied with versions of the receive clock.

The transmit clock and sync pulses are used to recover data from the E-Bus and send it through the fabric and LIs toward the designated SM. Each fabric board receives a transmit clock directly from the E-Bus, as do the fabric control boards. The fabric control boards relay the transmit clock and sync to the LIs.

2.3 ELEMENT C: DATA

Data is also divided into groups of receive and transmit, depending upon whether the data is moving towards or from the E-Bus. Receive data flow is illustrated in Figure 4.

Data from the SMs is received at the LI circuit packs from the NCT/NCT2 links. The link interface receiver (LIR) function (which resides in a custom device) buffers the incoming data before it is sent across the backplane to the SUB board. The SUB contains a 2:1 data multiplexer (*not to be confused with the previously mentioned control multiplexer*) which combines LIR data streams before distribution on the E-Bus.

The E-Bus distributes the data (*as well as clock and sync*) throughout the TMS so that all switch units have access to the received data. Once the TMS fabric has received the data from the E-Bus, it is then deemed *transmit* data.

Transmit data, as seen in Figure 5, is routed through the fabric board multiplexers and is sent to an LI. Data switched through fabric chip 0 on each fabric board is destined for LI 0. Likewise, data switched through

fabric chip 1 is destined for LI 1, and so on. A final stage of switching is performed on the LI fabric chip which is configured as a quad 4:1 multiplexer. (*Note that this fabric chip also receives its control information from the KBN2 circuit pack.*) The data is then checked for errors by the QLT function (which resides in a custom device) before being sent to the corresponding SM.

2.4 ELEMENT D: POWER

The emitter-coupled logic (ECL) used in the TMSU2 necessitates that -5 volt and -2 volt power be available throughout the shelf. Also, due to the large power draw by each circuit pack (*approximately 40 watts*) two -5 volt supplies are needed. Power distribution, shown in Figure 6, is implemented using two power groups allowing a minimal equipage of the switch unit to require only one -5 volt supply. Power Group A operates up to 4 LIs (*equivalent to 14 SMs*) before requiring the second 410AA power supply.

Minus two volts is available from a single 495MA supply capable of driving the entire shelf. Although the 495MA is a 2-inch wide supply, if a future 1-inch version is made available, the TMSU2 backplane is segmented so as to include a third 410AA supply configured to provide +5 volts to all but the KBN4 circuit packs. This feature provides the added flexibility for supporting future switch unit applications.

2.5 ELEMENT E: QLPS

The QLPS is a special case of data transport. Functionally, it provides a message pipe for SM-2000 to SM-2000 communication. Together with the quad link gateway processor (QGP) it also provides for SM-2000 to AM, and SM-2000 to classic SM communication. The QLPS has the same link interface to the TMSU2 as do the LI boards, and can reside in any QLI/QLI2 slot. In addition, it has 4 QGP ports which are cabled to the CMCU and to the appropriate QGP(s). QLPS is an optional feature and either 0, 1, 2, 3, or 4 boards may be equipped in a unit depending on switch configuration.

Inter-SM-2000 data comes into the TMS through NCT2 links connected to QLI2s. This data leaves the QLI2 and is routed through the fabric to a QLPS. The QLPS transfers this transmit data to a receive clock and then routes it according to the destination field in the data frame. The frame leaves the QLPS and is routed once again through the fabric to the QLI2 which connects to the destination SM-2000. SM-2000 to AM or non-SM-2000 communication goes from the SM-2000 to the QLPS as described above and is then routed to one of the four QGP ports on the QLPS. The QGP then sends the packet to the AM/SM through the Message Switch (see MSCU CD).

3. ADDENDUM

Up to this point, the TMSU2 has been described on a functional basis. To supplement this presentation, Figures 7 through 10 have been included to illustrate circuit pack relationships with the backplane and to summarize the input/output characteristics of each pack.

FIGURE	DESCRIPTION	CODE
7	QLI/FLI	TN888/883
8	SUB	UN182
9	FABRIC	KBN4
10	FABRIC CONTROL	KBN2

4. REFERENCE DATA

4.1 WORKING LIMITS

None.

4.2 FUNCTIONAL DESIGNATIONS

DESIGNATION	MEANING
AM	Administrative module
CMCU	Communication module control unit
CPF	Circuit pack function
CPS	Circuit pack schematic
E-Bus	Emitter coupled logic bus
NCT	Network control and timing
TMS	Time multiplexed switch
TMSU2	Time multiplexed switch unit model 2
SM	Switching module
QGP	Quad link gateway processor

4.3 CONNECTING CIRCUITS

3.01 The circuits connected directly in the TMSU2 are as follows:

E-Bus
* Shelf utility board
* Fabric boards
* Fabric control boards

TSIU
* Quad link interface boards
* Foundation link interface boards
* Quad link interface 2 boards

CMCU
* Foundation link interface
* Shelf utility board
* Control and display pack

CMPU
* Quad link packet switch boards

4.4 ACRONYMS

CIC - Control Interface Chip
ECL - Emitter-Coupled Logic
FLI - Foundation Link Interface
LI - Link Interface
LIR - Link Interface Receiver
MSCU CD - Message Switch Control Unit Circuit Description

SUB - Shelf Utility Board
QLI - Quad Link Interface
QLPS - Quad Link Packet Switch
QLT - Quad Link Transmit

5. REASON FOR REISSUE

To include the detailed description of the TMSU2 including QLI2 and QLPS.

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Note 1: For this slot any of the following boards can be equipped: TN888 (QLI), TN1681 (QLI2), TN1682 (QLPS).

Note 2: For this slot any board in Note 1 can be equipped, except for base bays 5 & 6 TMSUs where a TN883 (FLI) is equipped.

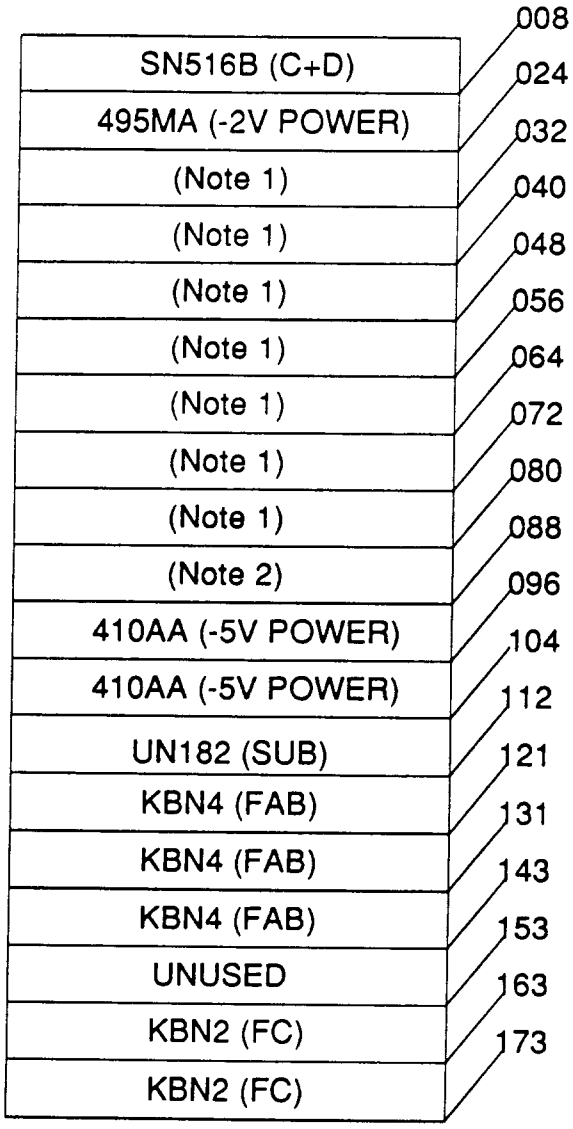

Figure 1. Time Multiplexed Switch Unit Model 2 (TMSU2)

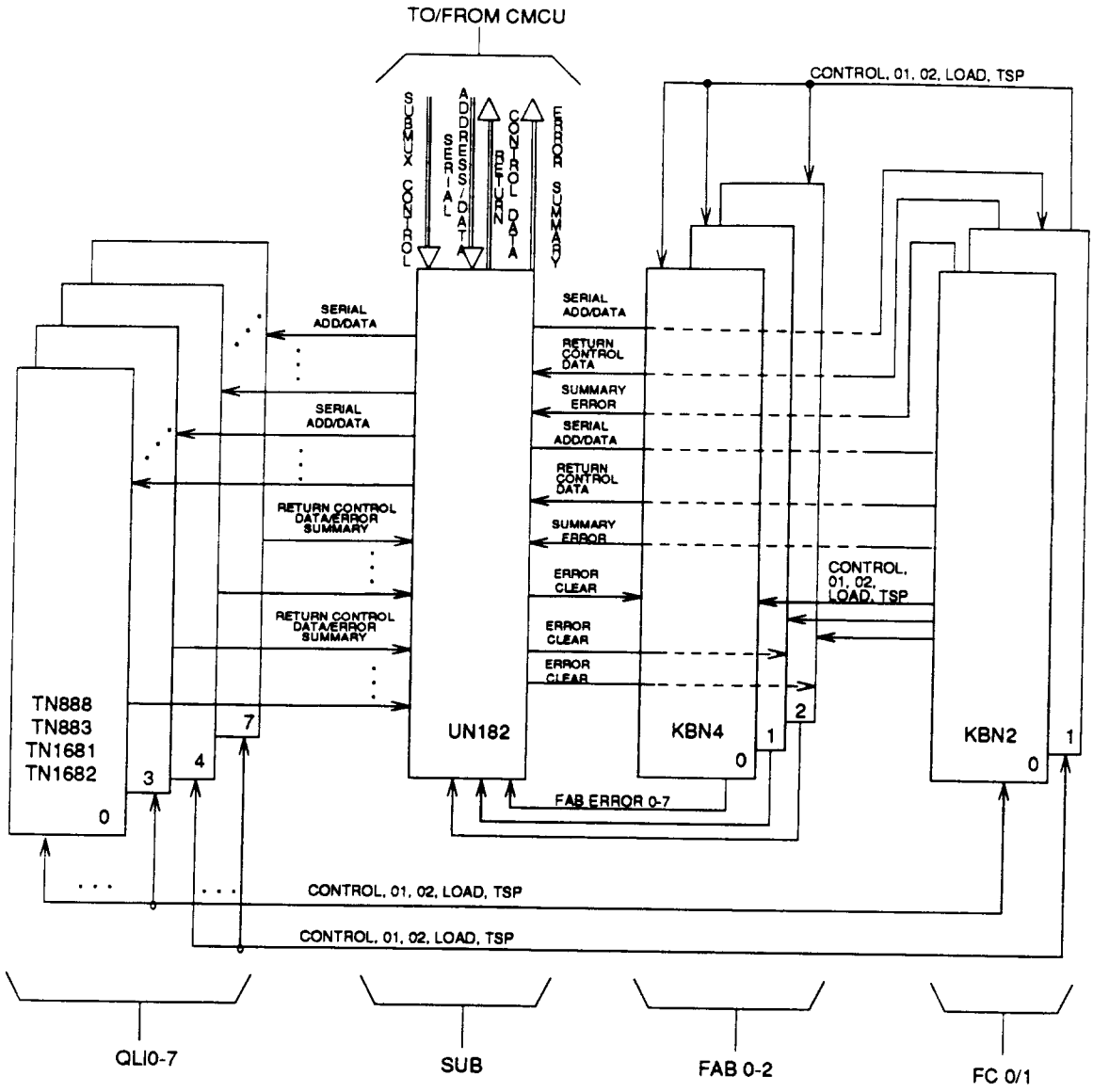

Figure 2. TMSU2 Element A: Control Distribution

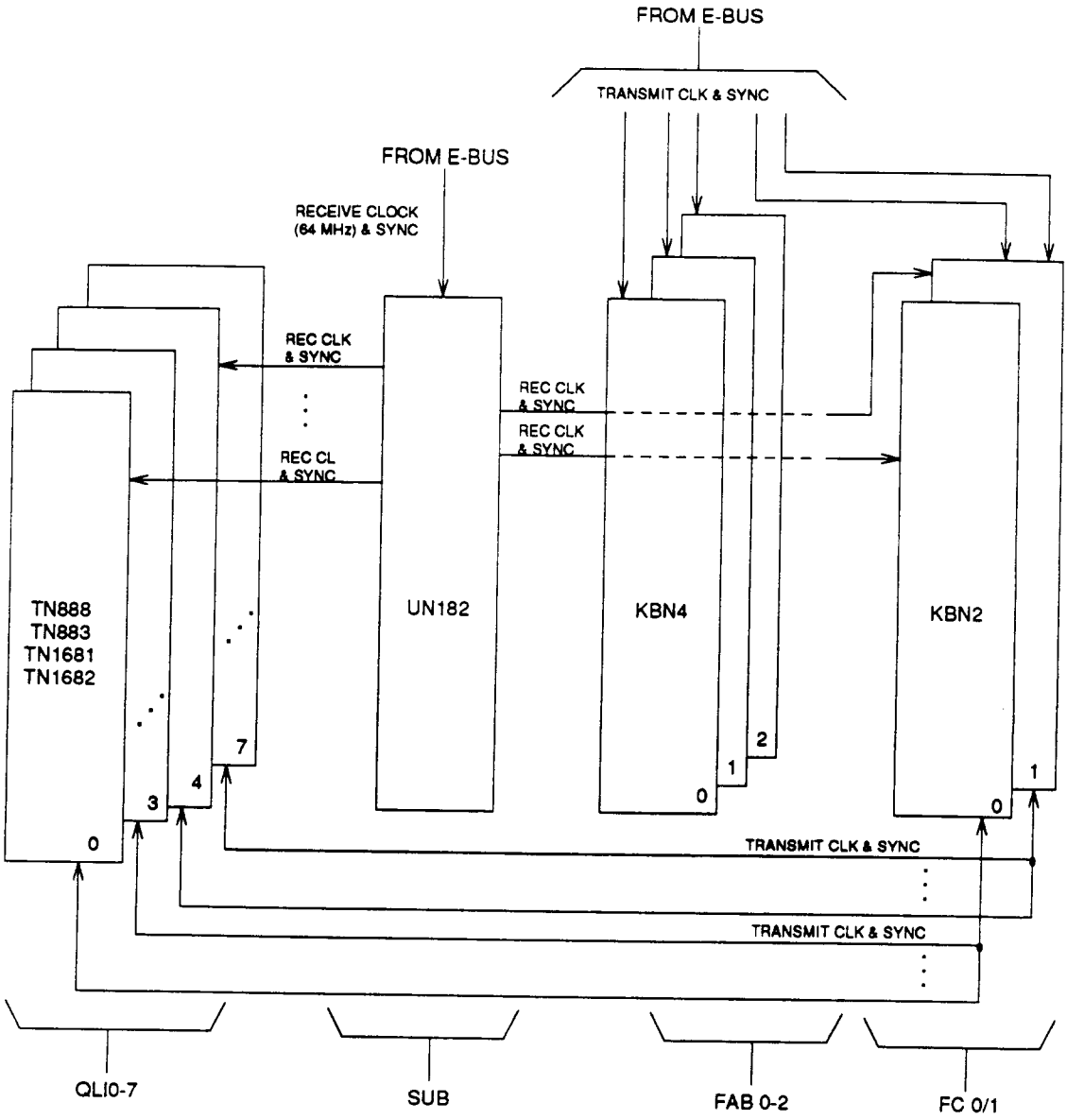

Figure 3. TMSU2 Element B: Control Distribution

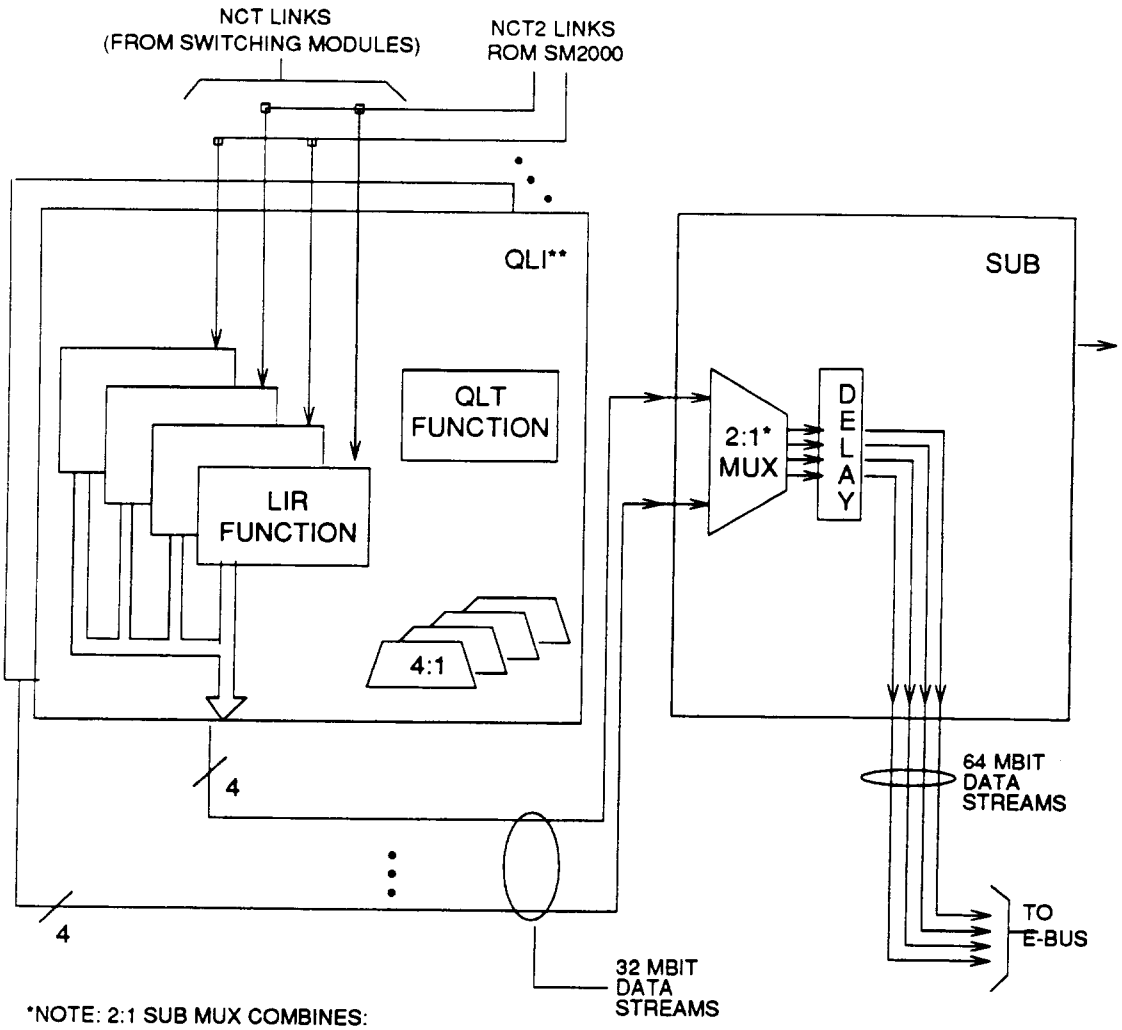

Figure 4. Part One of TMSU Element C: Receive Data

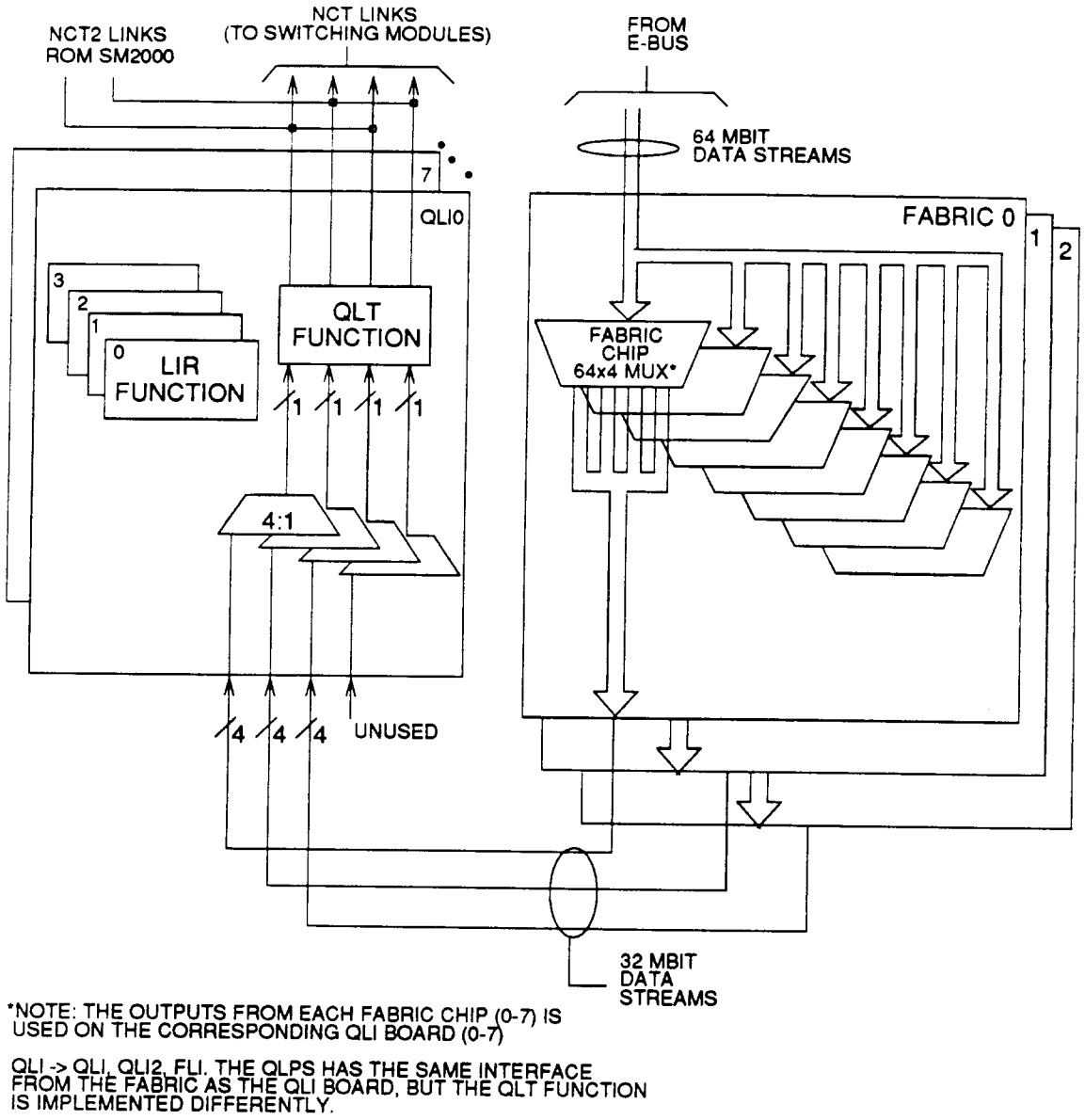

Figure 5. Part Two of TMSU Element C: Transmit Data

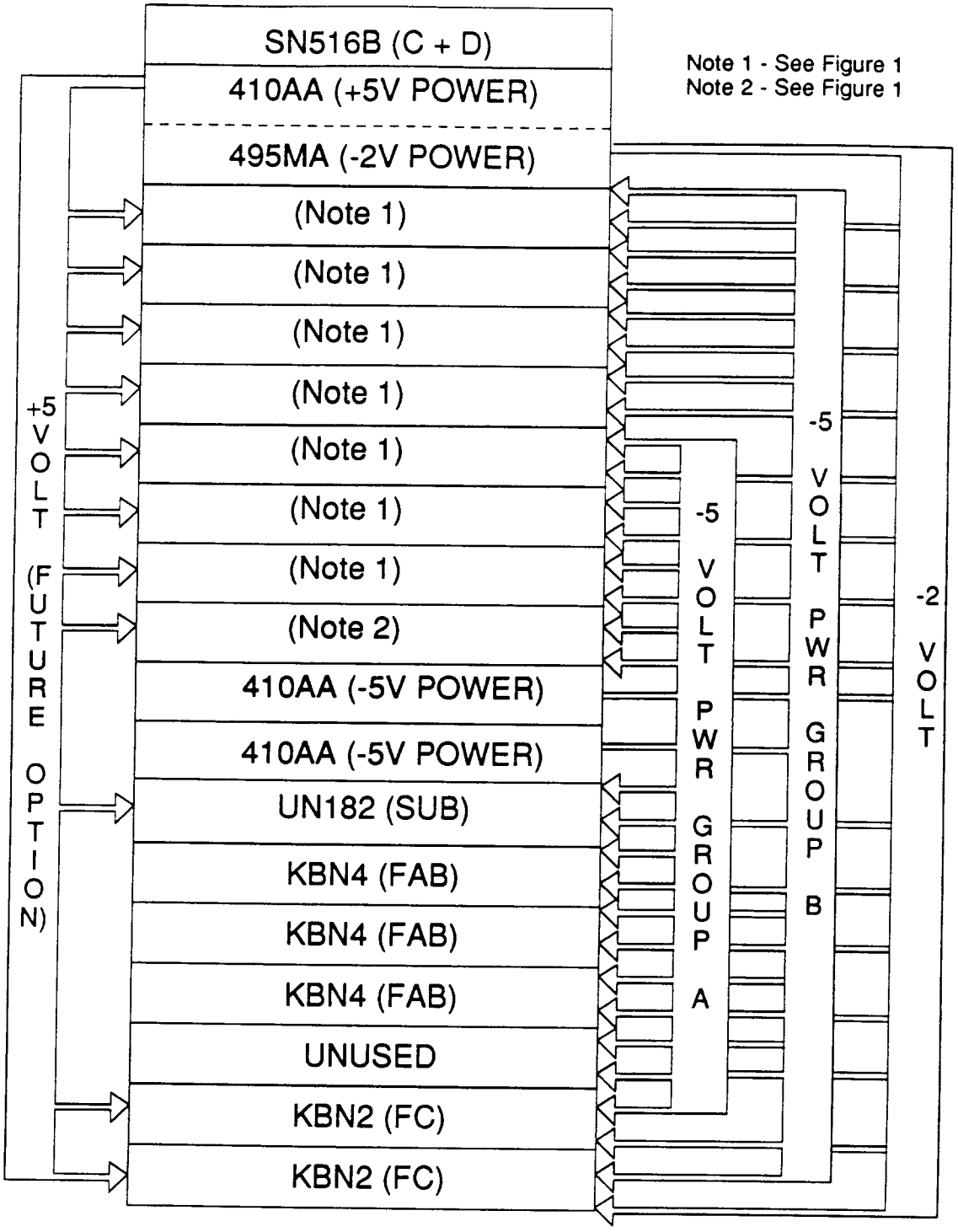

Figure 6. TMSU Element D: Power Distribution

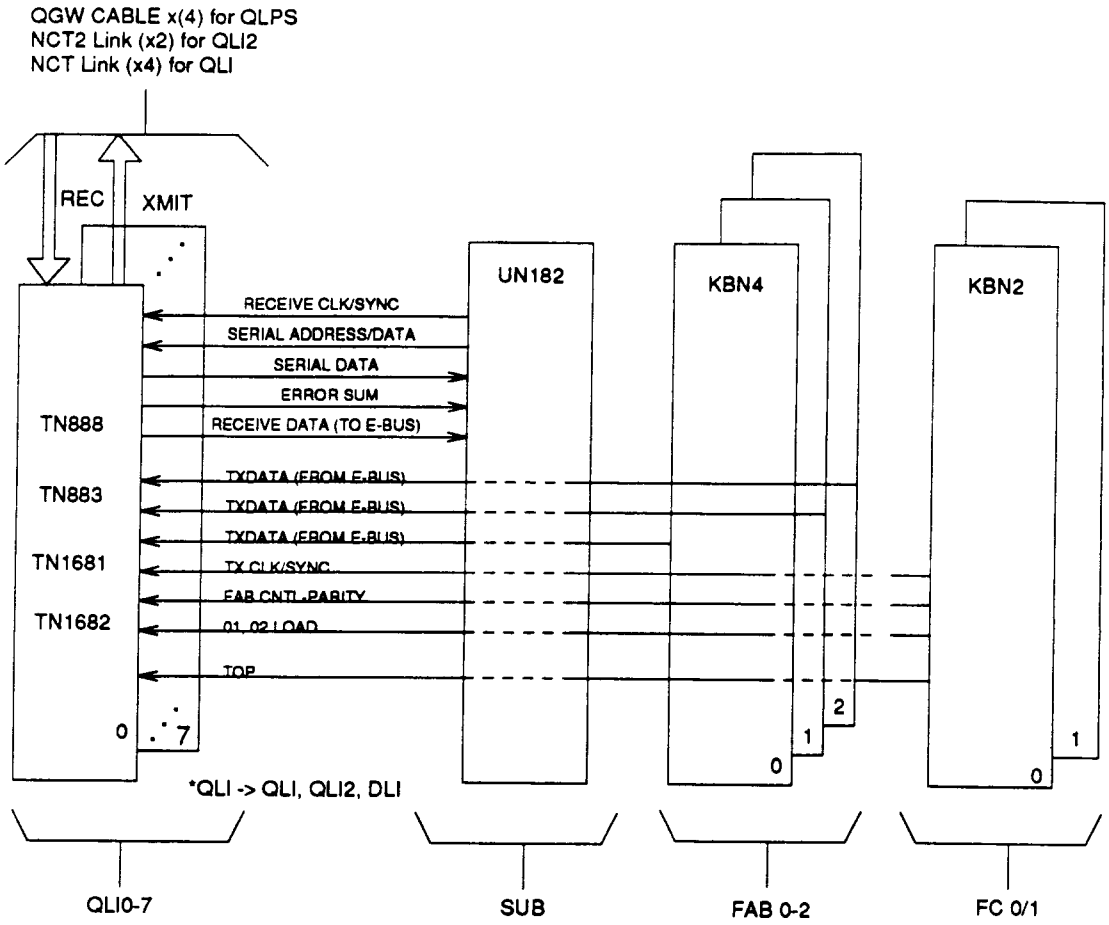

Figure 7. QLI*/QLPS I/O

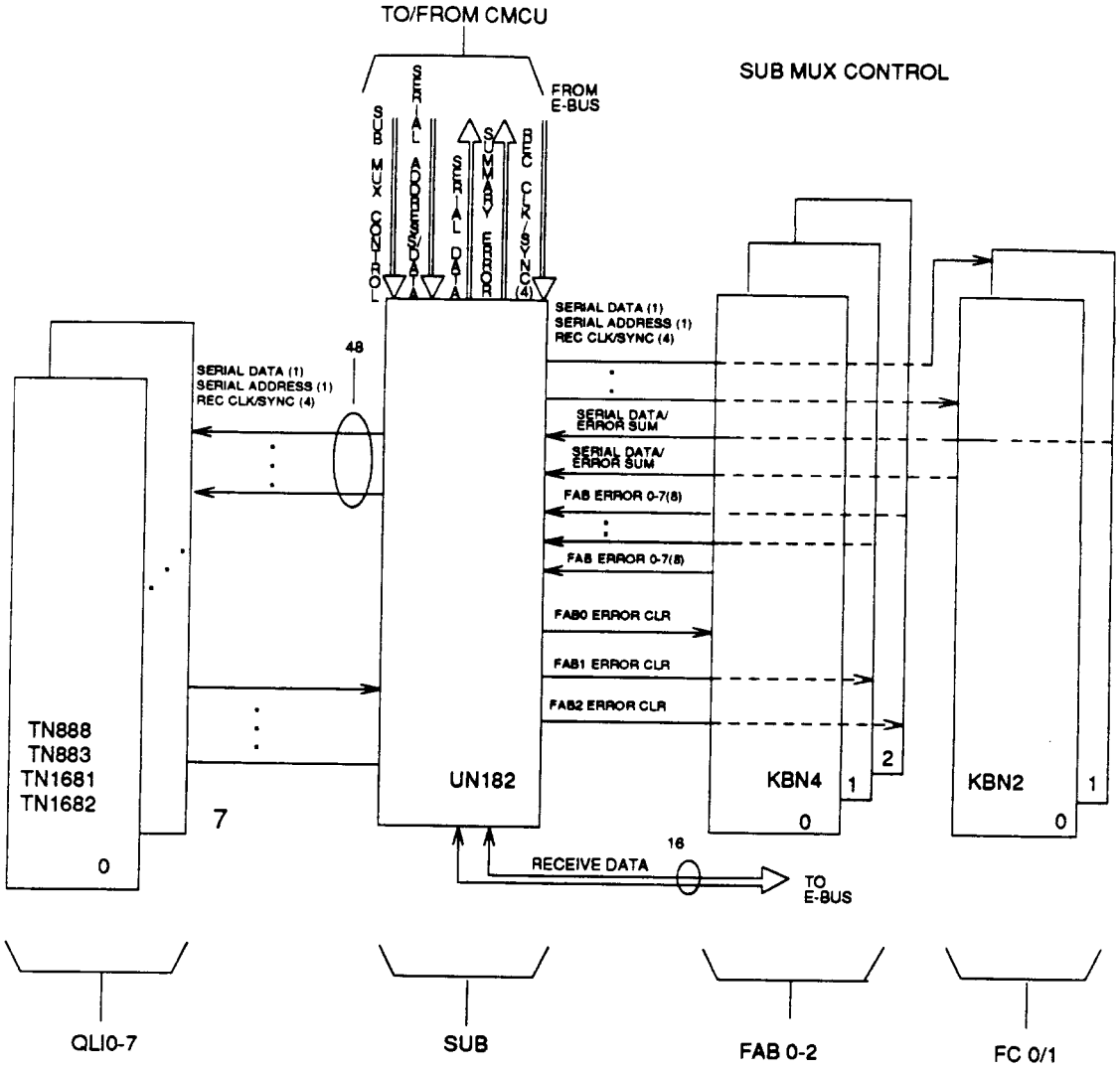

Figure 8. SUB BOARD (UN182) I/O

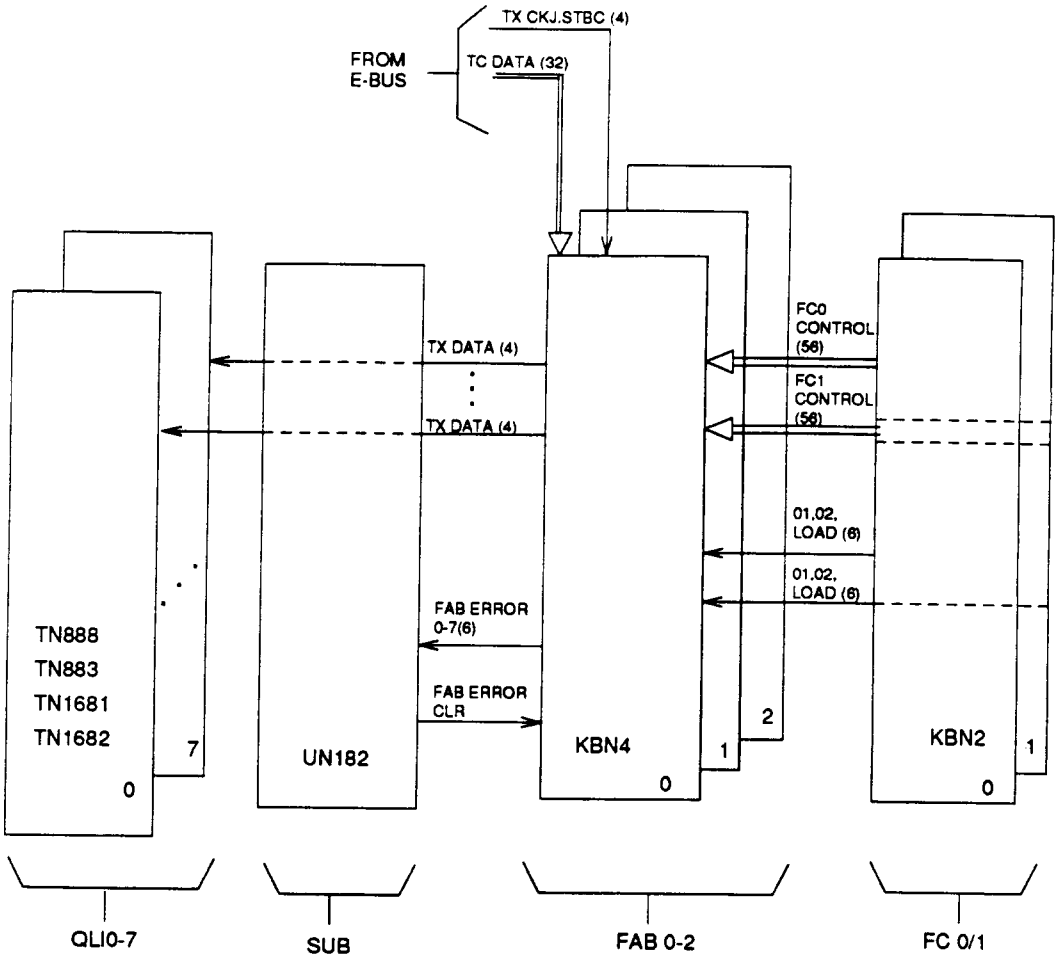

Figure 9. Fabric Control (KBN1) I/O

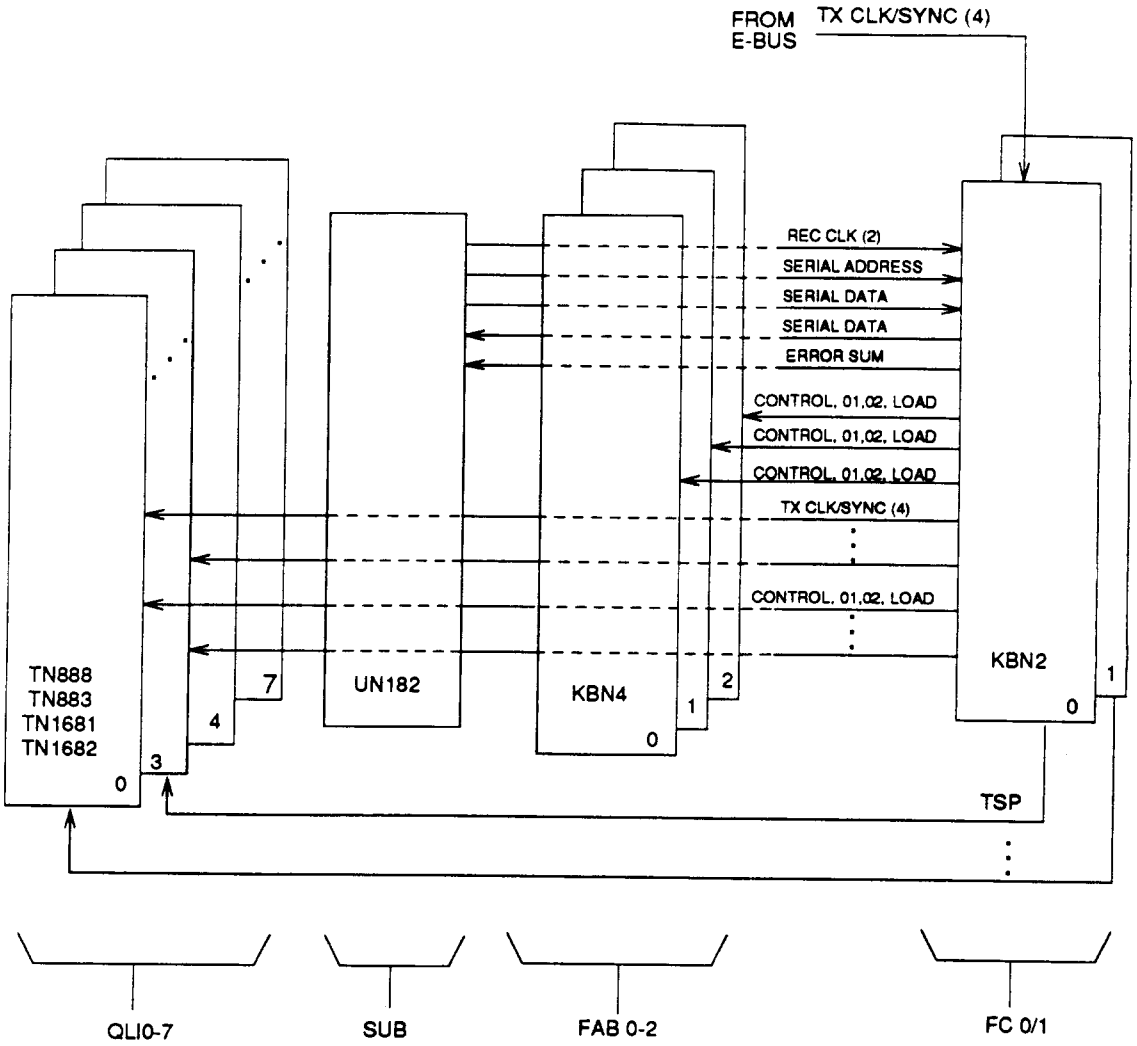

Figure 10. Fabric Control (KBN2) I/O

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TIME MULTIPLEXED SWITCH UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes In Apparatus

B.1 Replaced the 1A transceiver with the 982TT.

D. Description of Changes

D.1 Cost-reduced the 1A transceiver (982FH), and replaced it with the 982TT.

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TIME MULTIPLEXED SWITCH UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes In Apparatus

B.1 Changed TMSU-2 equipage for KBN-4 boards.

D. Description of Changes

D.1 Changed dual fabric TMSU-2 equipage for KBN-4 boards.

D.2 Added information to the features and option table for the new cost-reduced dual fabric.

D.3 Renamed the existing dual-fabric double dual fabric' and rated it A&M.

D.4 Changed single fabric as follows:

A. Existing CM-2 offices with 22 SM's or less, no change is required.

B. Existing CM-2 offices with more than 22 SM's or when an office grows to more than 22 SM's, replace KBN1's with KBN4's.

C. All new CM-2 factory production use KBN4's.

D.5 Added Option ZC and ZD.

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TIME MULTIPLEXED SWITCH UNIT, MODEL 2
CIRCUIT

CHANGES

B. Changes In Apparatus

B.1 Add fiber optics for the two-mile optically remote module (TRM).

D. Description of Changes

D.1 Add options B, E, F, G, J, K, M, N and 2B to APP Fig 4-13. These options are required for the two-mile optically remote module (TRM). These options replace the 1A transceiver with a 982 TH connector when the two-mile optically remote modules are connected to the switch. Single fabric requires one 982 TH equipped for each TRM. Dual fabric requires two 982 THs equipped for every two TRMs connected to the switch.

D.2 Add note table in the D section power down before removing packs.

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5ESS™ SWITCHING EQUIPMENT

TIME MULTIPLEXED SWITCH UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes In Apparatus

B.1 None.

D. Description of Changes

D.1 Reconfigure feature & option table to work with double-dual fabric and KBN1 Derating. Remove KBN2 from App Fig. 10 and generate App Fig. 19 for the 2nd KBN2.

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5ESS™ SWITCHING EQUIPMENT

TIME MULTIPLEXED SWITCH UNIT MODEL 2 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

This section provides a high-level view of the Time Multiplexed Switch Unit Model 2 (TMSU2).

1. PURPOSE OF CIRCUIT

1.01 The TMSU2 provides the physical paths which carry data and control messages between the switching modules (SMs) and the administrative module (AM). Major functions of the TMSU2 are to:

1. Provide a fixed control path between the AM and its associated SMs.

2. Provide switched data paths between the SMs connected to the time multiplexed switch (TMS).

3. Provide for clock distribution to the SMs by transmitting data timed from a clock which is derived from a Bell System Reference Clock.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The TMSU2 is connected to the SMs via the network control and timing (NCT) links which terminate on the foundation link interface (FLI) board or the quad link interface (QLI) boards. For the purpose of clarity, the FLI and QLI circuit packs will be

referred to here as link interface (LI) boards. Data from the SMs is buffered by the LIs before being sent to the shelf utility board (SUB) where it is multiplexed up to a 64Mbit rate and placed on the emitter coupled logic bus (E-Bus). The E-Bus distributes clock and data signals to/from all switch units in the TMS.

2.02 Data received from the E-Bus is switched through the fabric board multiplexers and routed back to the appropriate link interface board. The LI checks the data for errors and sends it out to a receiving SM via the NCT links.

SECTION II - DETAILED DESCRIPTION

The TMSU2 is wired to accept the following circuit packs:

CIRCUIT PACK	DESIGNATION	QNTY.
SN516	CONTROL & DISPLAY	1
495MA	-2 VOLT POWER	1
410AA	-5 VOLT POWER	2
TN883	FOUNDATION LINK INTERFACE	1/0
TN888	QUAD LINK INTERFACE	7/8
UN182	SHELF UTILITY BOARD	1
KBN1	FABRIC	4
KBN2	FABRIC CONTROL	2

The circuit pack layout is shown in figure 1.

The TMSU2 is divided into 4 circuit elements with the control paths described in Element A. Element B details the clock distribution. Data distribution is explained in Element C and power distribution in Element D.

1. ELEMENT A: CONTROL

COMMUNICATIONS

1.01 The control structure of the TMSU2 is illustrated in figure 2. The TMS controller resides in the CMCU and interacts with each TMSU2 via the SUB board (UN182). Communications with the switch unit are accomplished through the use of a control interface chip (CIC) which converts the parallel address and data buses from the processor to serial address and data streams. These serial streams are distributed via the E-Bus to the SUB boards located in each TMSU2.

1.02 The SUB assumes the responsibility of distributing the serial address and data to the switch unit. Serial data returning from the switch unit flows in exactly the opposite direction with the SUB board collecting the serial streams from each circuit pack before sending data back to the controller. A multiplexer on the SUB selects which serial stream from all the various circuit packs is to be sent back to the controller. Control for the SUB multiplexer originates at the TMS controller and is derived from the address that the controller wishes to read.

ERROR REPORTING

1.03 Error reporting of TMSU2 is accomplished asynchronously through a pyramid error reporting architecture where errors are reported to the controller in the form of an error summary lead. Each circuit pack in the switch unit produces a summary of its error source registers. The SUB board serves as the collection center for these summary errors and produces a switch unit error summary used to

interrupt the TMS controller and invoke its error handling routines. When an error is detected, the TMS firmware will search through the error reporting hierarchy in hopes of finding the source of the interrupt.

FABRIC CONTROL

1.04 Control for the TMS fabric multiplexers is not provided directly by the TMS controller, but rather the KBN2 circuit pack. The TMS controller sends connection information to the KBN2 board, which in turn configures the fabric multiplexers located on the fabric and LI circuit packs on a per time-slot basis. The distribution of this control is illustrated in figure 2.

SHELF SELECT

1.05 Since a fully grown TMS contains 12 TMSU2s, a shelf select bus is used to identify the address range of each shelf. The bus is tied to all of the circuit packs on the shelf that perform address decoding and allows for the high-level decoding to be dependent on the state of the leads in the shelf select bus. A programming paddle-board located behind the last KBN2 pack determines the state of the shelf select bus and thus determines the shelf identification. With the high-level address decoding performed by the shelf, and not by the circuit pack, TMS circuit packs can be moved between shelves while only maintaining their "base" addresses.

2. ELEMENT B: CLOCK

2.01 All clocks used in the TMSU2 originate from the E-Bus. The clocks themselves are designated as either "receive" or "transmit", depending upon whether they are being used to clock data onto or from the E-Bus. Clock distribution throughout the TMSU2 is shown in figure 3.

2.02 Receive clocks are used by the LIs to send received data from the SMs to the SUB and onto the E-Bus. As with the case of serial address and data, the LIs acquire their receive clocks from the SUB board, which serves as a distribution point. A secondary function of the receive clock is to clock the incoming serial address and data streams from the TMS controller. It is for this reason that the KBN2 boards are also supplied with versions of the receive clock.

2.03 The transmit clock and sync pulses are used to recover data from the E-Bus and send it through the fabric and LIs toward the designated SM. Each fabric board receives a transmit clock directly from the E-Bus, as do the fabric control boards. The fabric control boards relay the transmit clock and sync to the LIs.

3. ELEMENT C: DATA

3.01 Data is also divided into groups of receive and transmit, depending upon whether the data is moving towards or from the E-Bus. Receive data flow is illustrated in figure 4.

3.02 Data from the SMs is received at the LI circuit packs from the NCT links. A link interface receiver chip (LIR) buffers the incoming data before it is sent across the backplane to the SUB board. The SUB contains a 2:1 data multiplexer (not to be confused with the previously mentioned control multiplexer) which combines LIR data streams before distribution on the E-Bus.

3.03 The E-Bus distributes the data (as well as clock and sync) throughout the TMS so that all switch units have access to the received data. Once the TMS fabric has received the data from the E-Bus, it is then deemed transmit data.

3.04 Transmit data, as seen in figure 5, is routed through the fabric board multiplexers and is sent to an LI. Data switched through fabric chip 0 on each fabric board is destined for LI 0. Likewise, data switched through fabric chip 1 is destined for LI 1, and so on. A final stage of switching is performed on the LI fabric chip which is configured as a quad 4:1 multiplexer. (Note that this fabric chip also receives its control information from the KBN2 circuit pack.) The data is then checked for errors by the QLT chip before being sent to the corresponding SM.

4. ELEMENT D: POWER

4.01 The emitter-coupled logic (ECL) used in the TMSU2 necessitates that -5 volt and -2 volt power be available throughout the shelf. Also, due to the large power draw by each circuit pack (approximately 40 watts) two -5 volt supplies are needed. Power distribution, shown in figure 6, is implemented using two power groups allowing a minimal equipage of the switch unit to require only one -5 volt supply. Power Group A operates up to 4 LIs (equivalent to 14 SMs) before requiring the second 410AA power supply.

4.02 Minus two volts is available from a single 495MA supply capable of driving the entire shelf. Although the 495MA is a 2-inch wide supply, if a future 1-inch version is made available, the TMSU2 backplane is segmented so as to include a third 410AA supply configured to provide +5 volts to all but the KBN1 circuit packs. This feature provides the added flexibility for supporting future switch unit applications.

SECTION III - ADDENDUM

Up to this point, the TMSU2 has been described on a functional basis. To supplement this presentation, figures 7 through 10 have been included to illustrate circuit pack relationships with the backplane and summarize the input/output characteristics of each pack.

FIGURE	DESCRIPTION	CODE
7	QLI/FLI	TN888/883
8	SUB	UN182
9	FABRIC	KBN1
10	FABRIC CONTROL	KBN2

SECTION IV - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

DESIGNATION	MEANING
AM	Administrative module
CMCU	Communication module control unit
CPF	Circuit pack function
CPS	Circuit pack schematic
E-Bus	Emitter coupled logic bus
NCT	Network control and timing
TMS	Time multiplexed switch
TMSU2	Time multiplexed switch unit model 2
SM	Switching module

3. CONNECTING CIRCUITS

3.01 The circuits connected directly in the TMSU2 are as follows:

E-Bus
* Shelf utility board
* Fabric boards
* Fabric control boards

TSIU
* Quad link interface boards
* Foundation link interface boards

CMCU
* Foundation link interface
* Shelf utility board
* Control and display pack

SECTION V - REASON FOR REISSUE

To include the detailed description of the TMSU2.

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