

5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT,
MODEL 2

CHANGES

D. Description of Changes

D.1 Added the DMA (direct memory access) controller request and acknowledge leads associated with MMP2BA and BB (module message processors) (TN858), side A. This is a documentation change only. The added leads are shown below:

<u>Lead Designation</u>	<u>Symbol Nos. on FS 1</u>
AACCNACK	2,4
AADCNACK	2,4
AACCNREQ	2,4
AADCNREQ	2,4
ABCCNACK	6,8
ABDCNACK	6,8
ABCCNREQ	6,8
ABDCNREQ	6,8

AT&T BELL LABORATORIES

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Page 1
1 Page

SESS™ SWITCHING EQUIPMENT
 MESSAGE SWITCH PERIPHERAL UNIT
 MODEL 2

TABLE OF CONTENTS	PAGE	TABLE OF CONTENTS	PAGE
SECTION I - GENERAL DESCRIPTION	2	5. CADS.	6
1. PURPOSE OF CIRCUIT.	2	CAD 01.	6
2. GENERAL DESCRIPTION OF OPERATION	2	CADS 02 TO 03	6
MMP CONFIGURATION	2	CADS 04 TO 07	6
FPC/PPC CONFIGURATION	2	CADS 08 TO 011.	6
SECTION II - DETAILED DESCRIPTION	3	CADS 012 TO 013	6
1. FUNCTIONAL SCHEMATIC 1.	3	CAD 014	7
MODULE MESSAGE PROCESSOR - SIDE A.	3	CAD 015	7
FOUNDATION PERIPHERAL CONTROLLER.	4	CAD 016	7
PUMP PERIPHERAL CONTROLLER.	4	CAD 017	7
2. FUNCTIONAL SCHEMATIC 2.	5	CAD 018	7
CONTROL AND DISPLAY - SIDE A.	5	CAD 019	7
POWER CONVERTER - SIDE A.	5	CAD 020	7
3. FUNCTIONAL SCHEMATIC 3.	5	CADS 021 TO 022	7
MODULE MESSAGE PROCESSOR - SIDE B.	5	CADS 023 TO 026	7
4. FUNCTIONAL SCHEMATIC 4.	6	CADS 027 TO 028	7
CONTROL AND DISPLAY - SIDE B.	6	CAD 029	7
POWER CONVERTER - SIDE B.	6	CAD 030	7
		CAD 031	7
		CAD 032	7
		CAD 033	8

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TABLE OF CONTENTS	PAGE
CAD 034	8
CAD 035	8
SECTION III - REFERENCE DATA.	8
1. WORKING LIMITS.	8
VOLTAGES.	8
AMBIENT TEMPERATURE	8
2. CONNECTING CIRCUITS	8
MESSAGE SWITCH CONTROL UNIT - SD-5D026-01	8
MESSAGE INTERFACE AND CLOCK UNIT - SD-5D125-01.	8
FUSE FILTER PANEL - SD-5D053-01	8
INPUT OUTPUT PROCESSOR - SD-5D4C101-01	8
REFERENCES.	8
ATTACHMENTS	9

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 In a multimodule office configuration supporting a maximum of 32 Switch Modules (SMs), a simplex Message Switch (MSG) is equipped with three Message Switch Peripheral Units (MSPUs), Model 1. Each MSPU can be used to house different Peripheral Controllers (PCs), such as the Module Message Processor (MMP), Foundation Peripheral Controller (FPC), and the Pump Peripheral Controller (PPC). The addition of a Message Switch Peripheral Unit, Model 2 (MSPU2), enables an office to support a maximum of 48 SMs.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The MSPU2 provides two communities of MMPs. Each community contains a maximum of two 4-board MMPs. Figure 1 illustrates the configuration of MMP circuit packs in the unit and the number required to service increasing numbers of SMs.

2.02 The MSPU2 has been designed to also support FPC and PPC circuit packs. Figure 2 illustrates the FPC and PPC configuration.

MMP CONFIGURATION

- In the MMP configuration, an MSPU2 can support two communities of two MMPs.
- Each MMP supports up to eight fixed control time slot channels. A community equipped with two MMPs provides 16 time slot channels. Each time slot in a community is allocated to a different SM. With two time slots per SM terminating on a simplex MSG, this arrangement allows 16 additional SMs to be supported with the addition of the MSPU2.
- The MSPU2 in the MMP configuration interfaces to the Message Interface/Clock Unit (MICU) via a Message Interface Bus (MIB).
- Also, the MSPU2 in the MMP configuration interfaces to the Message Switch Control Unit (MSCU) via the Input/Output Microprocessor Interface (IOMI) bus.

FPC/PPC CONFIGURATION

- In the FPC/PPC configuration, the FPC is used to control the MICU and the Time Multiplexed Switch (TMS) via a Control and Diagnostic

Access Link (CDAL). It also interfaces to the MSCU via an IOMI bus.

In the FPC/PPC configuration, the PPC is used to load the SM with data at a high data rate (192K bytes/sec). This data is pumped from the disk in the Administrative Module (AM) through the MSCU via the IOMI bus to the PPC. The PPC then sends the data to the MICU via a MIB bus. The MICU sends it to the TMS where it is distributed to the destination SM via a NCT link.

provides for reception/transmission of serial data on either of two MIBs. Operations performed by MMP1 serve MMP2A and MMP2B. Each MMP1 performs the following functions:

- Generation of timing signals which control serial data transfer between MMP1, MMP2, and the Message Interface and Clock Unit (MICU). Other timing signals generated control serial data parity checking and generation.
- Generation of interrupt control vectors to the MSPP following interrupt requests generated on MMP1 and MMP2 circuit packs.
- Selection of the active Message Interface Bus (MIB) for clock and sync source.
- Selection of which MIB (0 or 1) each time slot is to be extracted from.
- Parity checking of serial data, parallel data, and parallel address bus.
- The UN170B is the only orderable circuit pack for the MSPU2 unit. The UN170B replaces the UN170, which does not support Remote Switching Modules (RSMs).

SECTION II - DETAILED DESCRIPTION

1. FUNCTIONAL SCHEMATIC 1

MODULE MESSAGE PROCESSOR - SIDE A

1.01 Side A of the MSPU2 unit contains one community of two 4-board MMPs. An MMP consists of three or four circuit packs: TN856B Message Switch Peripheral Processor (MSPP), UN170B Module Message Processor 1 (MMP1), and one or two TN858 Module Message Processor 2 circuit packs (MMP2A and MMP2B).

1.02 Message Switch Peripheral Processor - TN856B The MSPP is the controlling circuit pack of all message switch peripheral controller applications. The MSPP is a single-board processor with an interface through an IOMI bus to the MSCU and an interface to application boards needed for each particular function. An MSPP contains a 16-bit microprocessor, 128K bytes of dynamic random-access memory (DRAM), 8K bytes of static RAM, 16K bytes of erasable programmable read-only memory (EPROM), and clock circuits to ensure its own sanity as well as to provide needed timing to application boards.

1.03 Module Message Processor 1 - UN170B The MMP1 circuit pack

1.04 On the MIB interface, MMP1 receives clock, sync, and serial time slot data from the MICU on either side 0 or 1. The MMP1 sends serial time slot data to the MICU on both sides 0 and 1.

1.05 On the MSPP microprocessor interface, MMP1 receives address, address parity, data, data parity, and control signals. The MMP1 sends data, data parity, and control signals to the microprocessor on this bus.

1.06 On the MMP2 interface, MMP1 sends and receives the serial time slot data and various control signals such

as timing, interrupt, and parity fault indicators.

1.07 Module Message Processor 2 - TN85B The MMP2 design provides for reception/transmission of serial data on four time slots using level 2 of the BX.25 protocol. Extensive error checking facilities are included to ensure data integrity. Each MMP consists of at least one, and as many as two MMP2 circuit packs.

1.08 Each MMP2 performs the following functions:

- Demultiplexing of four control time slots received from MMP1.
- Disassembly and error checking of the received time slot frames, which correspond to the BX.25 protocol.
- Transfer of the information field of the received time slot frames to the MSPP dynamic RAM, under DMA control.
- Transfer of data from the MSPP's dynamic RAM to the information field of the transmitted time slot frames, which correspond to BX.25 protocol.
- Assembly of the transmitted time slot frames, which correspond to BX.25 protocol.
- Multiplexing of four time slots, and retransmission to MMP1.
- Parity checking of serial data, parallel data, and parallel address bus.

1.09 On the MSPP microprocessor bus interface, MMP2 sends and receives address, address parity, data, data parity, and control signals. During DMA transfers 20 address lines are used. Only the low 8 order address lines are decoded for I/O commands.

1.10 On the MMP1 interface, MMP2 sends and receives the serial time slot data and various control signals such as timing, interrupt, and fault indicators.

FOUNDATION PERIPHERAL CONTROLLER

1.11 In the FPC/PPC configuration, only Side A of the MSPU2 unit contains an FPC. The Foundation Peripheral Controller (FPC) contains a UN173 and a TN856B. The FPC provides control and diagnostic access to the Link Interface (LI), Network Clock (NCLK), Message Interface (MI), and Time Multiplex Switch (TMS).

1.12 Foundation Peripheral Controller Circuit Pack - UN173 The UN173 contains circuitry that performs the following functions:

- Serial interface to the four subdevices over the Control and Diagnostic Access Link (CDAL). This interface is accomplished with a fixed hardware protocol provided by the Control and Diagnostic Access Circuit (CDAC). A PROM sequencer is used to provide the necessary control signals associated with the protocol.
- Generation of maskable interrupt control vectors to the MSPP upon reception of error or service requests from one of the four subdevices.
- Selection of the active CDAL (0 or 1).
- Parity checking of address and data received from the MSPP. Parity generation over the data bus during data transfers to the MSPP.

1.13 On the MSPP microprocessor bus interface, UN173 receives address, address parity, data, data parity, and various control signals.

UN173 sends data, data parity, and control signals to the MSPP on this bus.

1.14 On the CDAL interface, UN173 sends and receives serial data and control signals.

PUMP PERIPHERAL CONTROLLER

1.15 In the FPC/PPC configuration, only Side A of the MSPU2 unit contains a PPC. The Pump Peripheral Controller (PPC) contains a UN886 and a TN856B circuit pack.

1.16 Pump Peripheral Controller Circuit Pack - TN886 The TN886 contains circuitry that performs the following functions:

- A pair of 4K byte buffers temporarily store blocks of data written by the MSPP.
- An 11-bit word counter generates the RAM buffer address during reads (transmissions to the Switch Module). An address multiplexer switches the source of the RAM buffer's address from the address counter to the processor's address bus.
- A data formatting circuit converts the 16-bit words read from the RAM buffer to 8-bit time slots. Each time slot contains six useful data bits, a framing bit, and a parity bit.
- An 8-bit time slot counter has two functions; the counting of the eight bits per time slot and the counting of the 32 time slots per frame.
- The output data circuit contains a multiplexer that switches idle code or data to the output. A shift register converts the parallel data to serial data which is outputted on the MIB at a 2MHZ rate.

- Time slot selection is accomplished by a 32-by-1 bit RAM. Each bit corresponds to one of the 32 time slots and is used to determine which of the 32 time slots will be used for data transmission during SM pump.

- Diagnostic circuits check data parity, address parity, data formatting, and the time slot select RAM.

1.17 Data blocks are transmitted in parallel format from the MSPP to the PPC. This interface contains a 16-bit address bus, 16-bit data bus and various control signals.

1.18 Data blocks are transmitted in serial format from the PPC to the MI on the MIB. This interface contains transmitted data, received data, and 4MHZ clock and sync signals. The maximum data transfer rate is 192K bytes/sec.

2. FUNCTIONAL SCHEMATIC 2

CONTROL AND DISPLAY - SIDE A

2.01 Side A of the MSPU2 unit contains one Control and Display circuit pack (SN412). In-service/out-of-service control and alarming of the power converters is performed by a Control and Display (C&D) circuit pack. The C&D circuit provides both manual and AM control of the MSPU2 from an in-service/out-of-service point of view. The AM monitors the C&D for fuse alarms, power alarms, and request for out-of-service.

POWER CONVERTER - SIDE A

2.02 Side A of the MSPU2 unit contains one Power Converter circuit pack (495FB). The purpose of the power converter is to provide a means of converting nominal -48 volt input to a well regulated +5 volt output for applications in the MSPU2 circuits. The power unit is pulse width

controlled for regulation, self-oscillating and operated at a fixed frequency. The 495FB provides -5 volts at 250 watts.

3. FUNCTIONAL SCHEMATIC 3

MODULE MESSAGE PROCESSOR - SIDE B

3.01 Side B of the MSPU2 unit contains one community of two 4-board MMPs.

3.02 Message Switch Peripheral Processor - TN856B The MSPP is described in 1.02.

3.03 Module Message Processor 1 - LN170B The MMP1 is described in 1.03.

3.04 Module Message Processor 2 - TN858 The MMP2 is described in 1.07.

4. FUNCTIONAL SCHEMATIC 4

CONTROL AND DISPLAY - SIDE B

4.01 Side B of the MSPU2 unit contains one Control and Display circuit pack (SN412). The SN412 is described in 2.01.

POWER CONVERTER - SIDE B

4.02 Side B of the MSPU2 unit contains one Power Converter circuit pack (495FB). The 495FB is described in 2.02.

5. CADS

CAD 01

5.01 All input and output points to the unit are listed in CAD 01. They are grouped by function and alphabetized by net name.

CADS 02 TO 03

5.02 CAD 02 (side 0) and 03 (side 1) comprise the MIB cabling used to interconnect MSPU2 side A with the two MICUs 0 and 1. Each MIB cable contains eight leads. Because a differential interface is used, positive and negative leads of a particular signal are twisted, thus forming four pairs of twisted unidirectional signals.

5.03 Three of these signals are terminated at the MSPU2; they are - received data (2MHZ rate), 4MHZ clock, and a sync pulse (125 usec). The remaining signal is transmitted data (2MHZ rate) from the MSPU2 to the MICU.

5.04 As mentioned previously, an MSPU2 can be used in one of two configurations. In both configurations CADS 02 and 03 are needed. However, the location and purpose are different.

CADS 04 TO 07

5.05 CADS 04 to 07 comprise the Input/Output Microprocessor Interface (IOMI) bus which interconnects side A of the MSPU2 and the MSCU. The interface used is TTL and all signals are unidirectional (with the exception of the data bus and the data parity bit) and paired with ground. The names of the four cables used are address, data, control, and service.

5.06 The IOMI is used in both MSPU2 configurations.

CADS 08 TO 011

5.07 CADS 08 to 011 comprise the Control and Diagnostic Access Link (CDAL) which connects the MSPU2 to the MICU allowing control and diagnostic access of the various subdevices. The interface used is differential with the positive and negative leads of a particular signal twisted together. The names of the

CADS 023 TO 026

5.18 Same function as CADS 04 to 07 but are used for side B instead of side A.

CADS 027 TO 028

5.19 Same function as CADS 08 to 09 but are used for side B instead of side A.

CAD 029

5.20 CAD 029 is unused (reserved) in this issue of MSPU2.

CAD 030

5.21 Same function as CAD 017 but is used for side B instead of side A.

CAD 031

5.22 Same function as CAD 018 but is used for side B instead of side A.

CAD 032

5.23 Same function as CAD 019 but is used for side B instead of side A.

CAD 033

5.24 Same function as CAD 020 but is used for side B instead of side A.

CAD 034

5.25 Same function as CAD 014 but is used for side B instead of side A.

CAD 035

5.26 Same function as CAD 015 but is used for side B instead of side A.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

VOLTAGES

1. -42.75 to -52.5 volts. (Nominal -48 volts)

AMBIENT TEMPERATURE

1. 0 to 70 degrees Centigrade (at circuit pack).
2. 0 to 50 degrees Centigrade (office aisle ambient).

2. CONNECTING CIRCUITS

MESSAGE SWITCH CONTROL UNIT - SD-5D026-01

MESSAGE INTERFACE AND CLOCK UNIT - SD-5D125-01

FUSE FILTER PANEL - SD-5D053-01

INPUT/OUTPUT PROCESSOR - SD-5D4C101-01

REFERENCES

1. K. E. Sallese, Module Message Processor Circuit Description, November 16, 1983, 55612-831116.01IM.
2. K. E. Sallese, Message Switch Peripheral Unit Circuit Description, June 21, 1984, 55612-840731.01IM.

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CAD 032

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CAD 033

5.24 Same function as CAD 020 but is used for side B instead of side A.

CAD 034

5.25 Same function as CAD 014 but is used for side B instead of side A.

CAD 035

5.26 Same function as CAD 015 but is used for side B instead of side A.

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FUSE FILTER PANEL - SD-5D053-01

INPUT/OUTPUT PROCESSOR - SD-5D4C101-01

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2. K. E. Sallese, Message Switch Peripheral Unit Circuit Description, June 21, 1984, 55612-840731.01IM.

ATTACHMENTS

1. Figure 1. MSPU2 in the MMP Configuration
2. Figure 2. MSPU2 in the FPC/PPC Configuration

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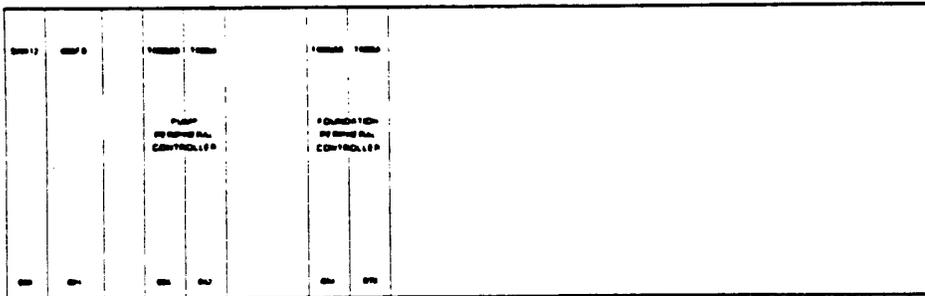


MSPU2 in the MMP Configuration

FIGURE 1

IHL42127A01

CD-5D066-01



MSPU2 in the FPC/PPC Configuration

FIGURE 2

IHL42127A01

CD-5D066-01