5ESS® SWITCHING EQUIPMENT
PACKET SWITCH UNIT
CIRCUIT

CONTENTS

1. GENERAL DESCRIPTION

1.1 OVERVIEW

The packet switch unit (PSU) is a switching module (SM) peripheral which, when used with the integrated services line unit (ISLU), will provide integrated services digital network (ISDN) capabilities in the 5ESS®. It provides a means of routing packetized data and signaling information between the SM and the ISLU (customer). The PSU can also provide common channel signaling system 7 (CCS7) signaling capabilities.

1.1.1 EXTERNAL INTERFACES

The PSU receives control commands from the modular controller time slot interchange (MCTSI) over the peripheral interface control buses (PICBs). The control fanout (CF) terminates a pair of PICB cables - one from each side of the MCTSI. The PICB interface allows the SM to send control commands to the PSU, to read back the status of the various parts of the PSU, and to be informed of error conditions present in the PSU.

The PSU (when configured for ISDN) terminates one duplexed pair of peripheral interface data buses (PIDBs) on each data fanout (DF) board. These come from both time slot interchange unit (TSIU) side 0 and side 1. The PIDBs contain the following signals: data in, data out, clock, and sync. These are differentially driven. The DF also connects to the ISLU through up to six directly connected peripheral interface data buses (DPIDBs). The DPIDBs are identical in format to the PIDB. The DF, which acts as a slave on the PIDB, acts as the master on the DPIDB interface. It sends clock and sync to the ISLU and generates and checks parity.

Signaling packets are sent to the DF from the ISLU. This information is then sent to the protocol handler (PH) over the PH data bus (PHDB), and from there to the switch module processor (SMP) through the packet fanout (PF), CF and packet interface (PI) through the packet bus (PB), packet interconnect bus (PIB), and subunit interface bus (SUIB), respectively. The SMP then sends the correct routing information to the CF, which in turn, relays it to the DF. With the correct routing established, the data can be sent between the PHs or actually between customers.

1.1.2 GENERAL FUNCTIONS

The PSU performs the function of packet switching calls in an ISDN environment between ISLUs. For an inter-SM call, the PSU works in conjunction with the TSIU over a PIDB to make the packet switched call. Multiple PIDBs can be used in a non-ISDN environment to provide CCS7 signaling. In a circuit switched ISDN call, the PSU is used to provide signaling information.

1.2 CIRCUIT PACK FUNCTIONS

The PSU circuit pack functions are to packet switch data and provide signaling information for ISDN calls and CCS7.

1.2.1 PACKET SWITCH UNIT COMMON BOARDS

The PSU common boards are the CF, PF, and DF packs, which are referred to as the PSU COMM. These packs are duplex and are used in an active/standby configuration. Their purpose is to route control and data information between the PSU and ISLU, and between the PSU and the modular controller time slot interchange unit (MCTSIU).

1.2.1.1 CONTROL FANOUT

The CF controls the PFs and the DFs and arbitrates the packet bus.

1.2.1.2 DATA FANOUT

The DF takes time slots on the PIDBs and the DPIDBs and switches them to the PHDB.

1.2.1.3 PACKET FANOUT

The PF interfaces 16 PHs to the packet bus.

1.2.2 PROTOCOL HANDLER

The PH switches the packet data through the network and provides some protocol processing on the packets.

1.3 INTERNAL INTERFACES

The CF sends out control messages and reads back status and error conditions to/from one of five packet fanouts (PFs) or data fanouts (DFs). This is accomplished using independent control interconnect bus (CIB) cables to each shelf. The CIB is a three-wire, 1-MHz bus, consisting of data in, data out, and clock. The bus between the PF and the PHs is the control bus (CB); it consists of a PH reset, side select, and an error lead. This configuration allows the SM to select which PSU control side the PH should "listen" to for resetting any PH, and to be alerted to error conditions.

The DF also provides an interface to each of 16 PH boards, the PHDB. The PHDB is identical to the DPIDB in its format; however, the PHDB signals are single-ended, rather than being driven differentially. The four signals are data in, data out, clock, and sync. Through commands received from the CF, the DF can route information between any PIDB or DPIDB time slot and any PHDB time slot.

See Appendix 1 for PSU diagram

2. DETAILED DESCRIPTION

2.1 PHYSICAL DESCRIPTION - SHELF LEVEL

The PSU shelf consists of a backplane (ED5D622) and the following base circuit pack codes:

Pack Code	Pack Name	Quantity
TN1366	Protocol Handler-1 (PH-1)	1 to 16
TN1081	Protocol Handler-2	1 to 16
TN1367	Protocol Handler-3_d	1 to 16
TN1367C	Protocol Handler-3_d	1 to 16
TN1371	Protocol Handler-3_i	1 to 16
TN1371C	Protocol Handler-3_i	1 to 16
TN1846	Protocol Handler-4	1 to 16
TN1848	Protocol Handler-6	1 to 16
TN1082	Control Fanout (CF)	2 *
TN1083	Packet Fanout (PF)	2
UN192	Data Fanout (DF)	2
UN348	Data Fanout_Multiple PIDB (DF_MP)	2
TN1042	Packet Interface (PI)	2 **

* The PSU requires only two CFs; not two per shelf.
** The PSU requires only two PIs; however, they reside in the TSIU.

2.1.1 BACKPLANE

The PSU backplane is a 12-layer, printed wiring board. The same backplane is used for all (up to five) shelves in the unit. A shelf identifier is used to determine the individual address of each PH. This shelf identifier is a 2x6 Berg connector positioned on the backplane at PH slot 15 at equipment location number (EQL) 04-178 106 for shelf 0. These connectors are numbered ED5D85-29 G24 for shelf 0 through ED5D585-29 G28 for shelf 4. The Berg connector grounds one or more of the BDADD4 - BDADD6 signals, which are pulled high on the PH boards. The -48 volt layer of the backplane is segmented to allow a robust fusing arrangement. The PH boards are broken into four groups of four PHs each. A 5 amp fuse is provided for each group of four PHs on each power bus. The power nets for the PHs are -48VA and -48PUA for the A bus and -48VB and -48PUB for the B bus. There is also a 5 amp fuse per PSU COMM per shelf. For the common boards, the signal names are -48V and -48 PU. Whether it is the A or B bus is determined by which PSU COMM it is.

2.1.2 CIRCUIT PACKS

2.1.2.1 PROTOCOL HANDLER

The protocol handler is used with n PHs in service and k PHs in spare, which is referred to as an n+k sparing arrangement. The PH board interfaces to a PB, a CB and to a PHDB. The PB is used to route packets between any two PHs or between a PH and the SM (through the PI). To transmit data over the PB, the PH issues a request to send (RTS), and must wait until the CF grants it permission to transmit by sending back a clear to send (CTS). These signals are routed by way of the PF, and muxed per shelf to the CF. The PF receives 16 PH/RTS signals and multiplexes them to the CF. Likewise, the PF receives a CTS signal from the CF, and the PF demultiplexes the CTS to the appropriate PH. The PH will then have exclusive use of the bus until it removes its RTS signal. Each packet contains an address that the PH and PIs must scan to determine if the packet is destined for them. If a PH or PI match on the address, the packet is read in; if not, it is simply ignored. The PH also interfaces with the DF through the PHDB that provides

a 32 time-slot path between the PH and the DF. Customer signal or data packets arrive at the PH from the DF over the PHDB. The PH does some protocol processing and places the packets in the dual-port random access memory (RAM). Signaling messages are sent out over the PB and routed to the PI. From the PI, the information is transferred to the SMP through the SUIB.

2.1.2.2 CONTROL FANOUT (CF)

The CF interfaces with the SM through PICBs. Each CF terminates a PICB from each MCTSIU side. These PICBs are used to send control commands, command acknowledgements, clock, and error reports between the CF and SMP. The duplex pair of CF boards on the first PSU shelf is capable of providing the control for a "fully grown" five-shelf PSU. The CF receives commands from the MCTSIU through the PICBs, interprets the commands, and relays them, through the CIB, to the appropriate PF or DF circuit pack. The CF communicates to the other shelves through an interconnect bus cable. The interconnect bus actually contains the signals for both the CIB and the PIB, which are terminated at the PF. The CF provides packet bus arbitration for the PSU. It grants permission to use the PB to any one of five PFs or to the PI. Each PF further decodes the CF's arbitration bits to decide which PH board gets the bus. These arbitration bits (PIBQA0 - PIBQD0) are sent to the PF through the PIB.

2.1.2.3 PACKET FANOUT (PF)

The PF plays the "middleman" in the communication between the CF and any one of 16 PHs. When a PH has a message to transmit, it must request use of the PB by activating its packet bus request to send (PBRTS) or RTS. The PF terminates 16 RTS leads, one from each PH, and multiplexes them into one RTS signal that is sent back to the CF. The CF polls the PFs and PIs; if it finds an RTS active, the polling is stopped, the CF issues a CTS, and control of the bus is transferred to the PF. The last step is for the PF to route that CTS to the appropriate PH, so that it may now transmit its data. Just as the PH muxes, demuxes, and routes data, it does the same for control information. Each PH has a side select and reset lead controlled by the CF through the PF. The PF has two octal latches for both the side select and the reset leads. If the CF wishes to reset all of the PHs, a command is sent to the PF to reset the PHs. The CF then writes into the two latches a bit map of which PHs are to be reset. The output of the latches is connected through the CBREN000 - CBREN150 leads to each PH. The CBSS000-CBSS150 are side select leads, sent to each of 16 PH's. They are used to tell the PH boards which is the active side of the PSU. The last of the control bus leads is the PHERR lead. The PF receives an error signal from each of the PH circuit packs. These leads are input into an error source register (ESR), and if an error is seen on any of the PH boards it is latched into the ESR, and an error message is sent to alert the CF.

2.1.2.4 DATA FANOUT (DF)

The DF is used in the PSU COMM as a means of routing data messages between any PH and the ISLU or TSIU. It receives control messages from the CF (over the CIB); these are used to set up the routing paths. This bus consists of a data in, data out, and a clock signal. It is used to send the DF commands, query it for status information, and receive error reports and command acknowledgements from the DF. The DF terminates one duplex pair of PIDBs from the TSIU and up to six DPIDBs from the ISLU. The DF also interfaces with each of 16 PHs through the PHDBs. The DF provides the ability to route data from any PIDB or DPIDB to any of the 16 PH boards. Extensive parity checking and generation is done over the entire DF data path. Any parity errors, as well as clock, sync, or TSI errors are latched into an ESR which is used to alert the CF of the error condition.

2.2 PHYSICAL DESCRIPTION - CABINET LEVEL

2.2.1 NUMBER OF SHELVES

The PSU cabinet can support anywhere from one to five PSU shelves.

2.2.2 COOLING

A six-fan unit is required, in addition to the existing six-fan unit, when the cabinet is equipped with more than three shelves.

2.2.3 POWER

The power for all of the packs in the PSU shelf is derived by on-board power modules. The PI board, which resides in the TSIU shelf, is powered by the bulk power converters on that shelf.

The power distribution to the PSU unit is -48 volts and is distributed as follows: one power feed to the cabinet is connected to side 0 of the PSU, the other power feed to the cabinet is connected to side 1 of the PSU. This is done to improve reliability on cabinets equipped with five PSU units.

2.3 INTERFACE DESCRIPTIONS

The packet interface circuit packs reside, not in the PSU shelf, but in the MCTSIU. These packs are duplex and provide the packet bus path between the CFs and the SM. The PI buffers packets sent from the SM (through the SUIB) and can relay those packets through the PB and the CF to the PHs. The CF provides the arbitration for the PB and scans the RTS signals for both the PFs and PIs in round-robin fashion. If the PI wants to transmit packets over the bus, it must activate its RTS and wait for the CF to grant permission to use it by sending the PI back a CTS. After the PI is granted permission to use the bus, it sends out its packets to the CF, which broadcasts these packets to both PIs, and all PFs. The PFs, in turn, fan the packets out to all PHs. The beginning of each packet contains a destination address that identifies which PH or PI the packet belongs to.

2.3.1 APPLICATION INFORMATION

To equip the DF with flexible time slot assignment (DF-Flex), the firmware on the DF changes from MC5D104A1 to MC5D124A1, and the firmware on the CF changes from MC5D102A1 to MC5D123A1. DF-Flex is a version of the DF that allows the allocation of time slots on a PHDB to be done in a flexible manner. Without DF-Flex firmware, a DF allocates only the even time slots on a PHDB that connects to an evenly numbered PH. Similarly, only the odd time slots are allocated on a PHDB that connects to an odd numbered PH. The DF-Flex firmware removes this restriction.

To equip the DF with enhanced B-channel packet switching (EBPS) capability, the firmware on the DF must change from MC5D124A1 to MC5D124A1B. This firmware on the DF allows for flexible time slot and on demand B-channel packet switching assignment.

The PSU DF with multiple PIDBs (DF_MP) supports an increase in the maximum number of 64 Kb/s timeslots from a TSIU to a PSU by increasing the number of PIDBs per shelf of the PSU. The DF_MP (UN348) does NOT and can NOT connect to an ISLU. The DPIDB circuitry was removed from the board to make space for the additional PIDB interface circuitry. To connect to an ISLU, use the UN192. The DF_MP would talk to the remote integrated services line unit (RISLU) indirectly through the PIDBs to the MCTSIU. The information would travel from the DF_MP through a PIDB to the MCTSIU. From there it is switched to a host digital facility interface (H-DFI) and transmitted through coaxial cable to the remote digital facility interface (R-DFI) in the digital line trunk unit (DLTU) that connects the RISLU to the host switching module (HSM). The R-DFI then provides the time slot connection to the ISLU common data (CD) pack.

To support the preventive cyclic retransmission (PCR) mode required for the CCS7 International Signaling Data Links using satellite links, microcode MD5D100A1 on PH-1 changed to MD5D100A1B.

The protocol handler 2 (PH-2) was developed to increase the number of digital subscriber lines (DSL's) that a PSU_shelf could interface with, to a maximum of 768. Prior to that, protocol handler 1 (PH-1) could interface with only 256 DSL's, extended DSL's, inter-SM packet traffic links, or 1 packet switching system (1PSS) links. The firmware for the PH-2 is MC5D115A1.

A more powerful protocol handler, PH-3_d was developed with greater speed and more memory. A higher performance PH-3, PH-3_i was introduced which allows more than one CCS7 link to be terminated on a PH. A "C" suffix version of the PH-3 circuit packs, MC5D146A1C and MC5D161A1C, was introduced to fix problems when the PH packs were used in 56KBS applications.

A Protocol Handler model 4 (PH4) was developed to support U.S. ISDN applications in the 5E10 software release.

A Protocol Handler model 6 (PH6) was developed to support the Signal Transfer Point International (STPI) mode in International CCS7 applications. This feature was introduced in software release 5EE6.2.

The following is a summary of the application firmware:

Pack Name	Pack Code	Microcode
CF	TN1082	MC5D102A1
CF	TN1082	MC5D123A1
PF	TN1083	MC5D103A1
DF	UN192	MC5D104A1
DF	UN192	MC5D124A1
DF_MP	UN348	*
PH-1	TN1366	MC5D100A1
PH-2	TN1081	MC5D115A1
PH-3_d	TN1367	MC5D146A1
PH-3_i	TN1371	MC5D160A1
PH-3_d	TN1367C	MC5D146A1C
PH-3_i	TN1371C	MC5D160A1C
PH-4	TN1846	*
PH-6	TN1848	*

* non-microcode controlled pack

See Appendix 2, Common Board Microcode Compatibility Chart.

Automatic power recovery (APR) enables the PSU to power back up after a power loss to the unit without any manual intervention. The following are the APR pack codes:

Pack Name	Pack Code
PF	TN1083C
CF	TN1082B
DF	UN192B
DF_MP	UN348B
PH-3_d	TN1367B
PH-3_i	TN1371B

PH-3_d	TN1367C
PH-3_i	TN1371C
PH-4	TN1846
PH-6	TN1848

2.3.2 WORKING LIMITS

0-49° Celsius ambient aisle temperature

The PSU will be operational at 39.5 volts, to meet the European Conference of Postal and Telecommunication Administrations (CEPT) requirements for APR.

2.3.3 MAINTENANCE/INSTALLATION CONSIDERATIONS

Before powering frame up with non-APR PHs, PHs must be disengaged from the backplane. The PHs can not be reinserted until after the frame's -48 volts has been applied.

3. REFERENCE DATA

None.

4. ACRONYMS

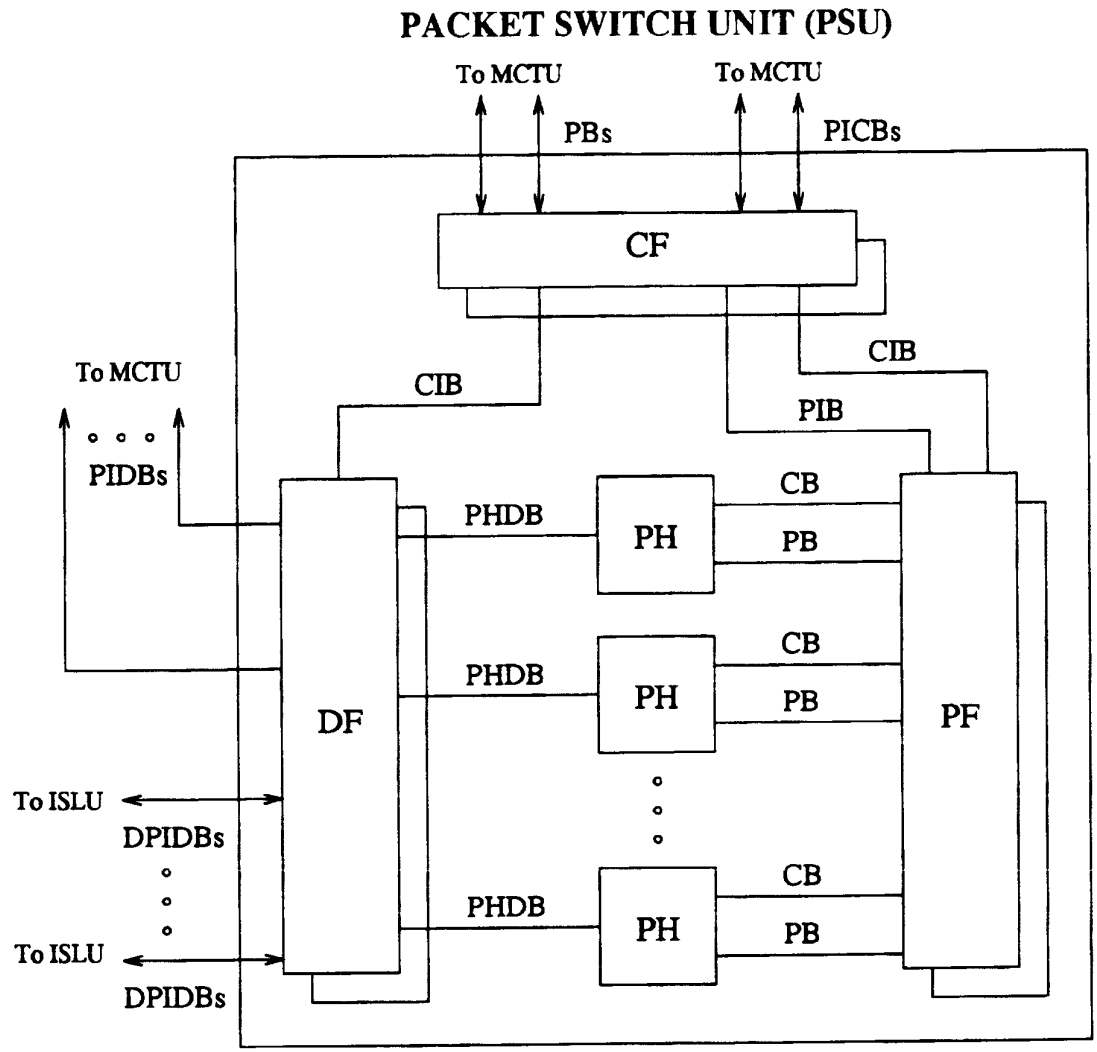
1PSS	1 Packet Switching System
APR	Automatic Power Recovery
CB	Control Bus
CCS7	Common Channel Signaling System 7
CD	Common Data
CEPT	European Conference of Postal and Telecommunication Administrations
CF	Control Fanout
CIB	Control Interconnect Bus
CTS	Clear To Send
DF	Data Fanout
DF-Flex	Data Fanout with Flexible Time Slot Assignment
DF_MP	Data Fanout with Multiple PIDB's
DLTU	Digital Line Trunk Unit
DPIDB	Directly Connected PIDB
DSL	Digital Subscriber Lines
EBPS	Enhanced B-channel Packet Switching
EQL	Equipment Location
ESR	Error Source Register
H-DFI	Host Digital Facility Interface
HSM	Host Switching Module
ISLU	Integrated Services Line Unit
ISDN	Integrated Services Digital Network
MCTSI	Modular Controller Time Slot Interchange
MCTSIU	Module Controller Time Slot Interchange Unit
PB	Packet Bus
PBRTS	Packet Bus Request To Send
PCR	Preventive Cyclic Retransmission
PF	Packet Fanout
PH	Protocol Handler
PH-3_d	Domestic Protocol Handler model 3
PH-3_i	International Protocol Handler model 3
PH-4	Protocol Handler model 4
PH-6	Protocol Handler model 6
PHDB	Protocol Handler Data Bus
PI	Packet Interface TN1042
PIB	Packet Interconnect Bus
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
PSU	Packet Switch Unit
RAM	Random Access Memory
R-DFI	Remote Digital Facility Interface
RISLU	Remote Integrated Services Line Unit
RTS	Request To Send

SM	Switching Module
SMP	Switch Module Processor
STPI	Signal Transfer Point International
SUIB	Subunit Interface Bus
TSIU	Timeslot Interchange Unit

AT&T BELL LABORATORIES

DEPT NA5360100-GPO-DJS

5. APPENDIX 1



LEGEND:

CB	Control Bus	PF	Packet Fanout
CF	Control Fanout	PH	Protocol Handler
CIB	Control Interface Bus	PHDB	Protocol Handler Data Bus
DF	Data Fanout	PIB	Packet Interface Bus
DPIDB	Directly Connected PIDB	PICB	Peripheral Interface Control Bus
MCTU	Module Control and Time Slot Interchange Unit	PIDB	Peripheral Interface Data Bus
		PB	Packet Bus

6. APPENDIX 2

Common Board Microcode Compatibility Chart:

Pack	Non-Flex	Flex	DF MP
CF	MC5D102A1	MC5D123A1	MC5D123A1
DF	MC5D104A1	MC5D124A1	-
PF	MC5D103A1	MC5D103A1	MC5D103A1