5ESS® SWITCHING EQUIPMENT
REMOTE CLOCK UNIT
CIRCUIT

CHANGES

B. Changes in Apparatus

Added option K which uses the SN516B in place of SN516 option L.

Added options G and H to reflect the microcode versions MC5D215a2 and MC5D215a1, respectively.

D. Description of Changes

Added wiring change, option J, to enable auto power restart and option L (SN516) or option K (SN516B) were added to FS1 and 2 symbol 1.

Note 102 was added for fuse information.

Note 203 was changed to add SN516B.

Note 303 was changed to show options G, H, L, and K.

Note 304 was changed to add SN516B.

Note 308 was added to describe auto power restart.

Note 309 was added to show option G (MC5D215a2) and option H (MC5D215a1).

Apparatus figures were changed to show options L and K.

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DEPT NA5301700-WFG-SDS

5ESS® SWITCHING EQUIPMENT
REMOTE CLOCK UNIT
CIRCUIT

CHANGES

B. Changes In Apparatus

B.1 Added options M and N, which use the TN1285B and TN1286B in place of TN1285 and TN1286 circuit packs.

D. Description of Changes

D.1 Circuit packs TN1285B and TN1286B provide for Conférence d'Europe de Poste et Télécommunication (CEPT) (European Conference of Postal and Telecommunications) administration capability.

D.2 Made documentation changes to App. and option index to reflect options M, N, and Q.

D.3 Made documentation change to composite diagram 1 to reflect options N, T, Y, and Z.

D.4 FS 1 and 2, symbols 5 and 8 have been revised to reflect option Q, TN1275B.

D.5 FS 1 and 2, symbol 9 has been revised to reflect options M and N, TN1285B and TN1286B.

D.6 FS 1, symbol 9 has been revised to remove lead designation O DO SO CR 0/1.

D.7 FS 2, symbol 9 has been revised to remove lead destination 1 DO SO CR 0/1.

D.8 Apparatus figures have been revised to reflect options M, N, and Q.

D.9 Notes 203, 302, 303, and 304 have been revised to reflect circuit packs TN1275B, TN1285B, and TN1286B, note 307 has been added to reflect circuit pack TN1274.

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5ESS® SWITCHING EQUIPMENT REMOTE CLOCK UNIT CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The 5ESS Network CLocK - Model 2 (NCLK2) provides the timing signal to the 5ESS switching network that allows it to be synchronized to a connected digital network. The NCLK2 provides high-stability operation, multiple reference facilities, analog references, and mutual synchronization.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The NCLK2, in a synchronized mode, derives a timing signal from designated external reference facilities, thus locking the 5ESS switching network to these reference facilities. In the case of a 5ESS system operating as a master clock source for a digital network, the NCLK2 generates this timing signal from its own internal source.

SECTION II - DETAILED DESCRIPTION

1.01 Each NCLK2 side functionally consists of a time-base oscillator, a Controller, a Digital Phased-Lock Loop (DPLL), and a Sync unit. The Sync unit interfaces to the external reference facilities, up to a maximum of eight. The Sync unit extracts the timing information from the external references and passes this information to the DPLL. The DPLL generates the 8 kHz timing signal that is sent to the Line Interface (LI) and locks this timing signal to the external reference facilities based on the information extracted by the Sync unit. In the event that a problem is detected on the external reference facilities or the external reference signals are lost, the DPLL will continue to provide a signal to the LI. In this "holdover" mode, the phase of

this output signal will be based on the last known good state of the external references. The stability of the timing signal sent to the LI during holdover will depend on the stability of the local NCLK2 oscillators. The DPLL also outputs a cross-couple signal to the opposite-side NCLK2. The NCLK2 sides are normally operated such that one side is providing an active timing signal (active-major mode) to its associated LI. The other side NCLK2 is forced to lock to the cross-couple signal that it receives (active-minor mode) to prevent any slips or hits in the 5ESS switching network when the sides are switched.

1.02 The Controller handles the communications with the HSM, performs the DPLL calculations, does maintenance on the NCLK2 circuits and on the external references, and performs some diagnostics on the NCLK2 under commands from the HSM.

1.03 The NCLK2 architecture uses a fixed-frequency time base to perform its function of locking to the external references. This time-base signal is provided by duplicated NCLK2 OSCillator units (NC-OSC), one NC-OSC residing in each half of the shelf. Each NCLK2 DPLL has access to both NC-OSC units and each NC-OSC unit is a unique failure group (separate powering, etc.), separate from the other components of the Office Network Timing Complex (ONTC).

1.04 The NCLK2 DPLL will be instructed from the Maintenance Software as to which NC-OSC it should use as its time-base. The NCLK2 architecture will allow the DPLLs on the two sides of the duplicated ONTC to operate either off the same NC-OSC or with each DPLL using the NC-OSC physically located in the same half of the shelf. For maintenance reasons, the normal mode of operation will be with both DPLLs using the same NC-OSC unit. Note that a failure of one NC-OSC does not force a switch of the ONTC sides, only a switch of NC-OSC units. (This switch will be required by both NCLK2 sides.)

1.05 For stand-alone applications, the NCLK2 will not be synchronized to any external reference facilities. Instead, the NCLK2 will serve as the master timing reference for the switch. In this case, another local oscillator will be used in place of the Sync unit on each NCLK2 side. This oscillator will then serve the same function as the external references -- it will provide a signal to which the NCLK2 DPLL will lock.

1.06 The DPLL used by the NCLK2 will be a second order type. The loop filter will consist of both a proportional term and an integral term, thus enabling the NCLK2 to zero out any errors caused by either phase steps or frequency steps on the external references. The time constants of the loop filter determine the response of the loop to changes on the external references.

1.07 The DPLL can be operated in four different modes. In the normal mode, the DPLL attempts to track the external references using the normal time constants for that application. In the fast mode, the time constants are reduced to allow the DPLL to achieve lock faster or, in the case of the minor clock side, to more accurately track the cross-couple signal from the major side. The third mode of operation is the holdover mode and is entered whenever problems are detected on the external references. In this mode, the DPLL is no longer locked to the external references. Instead, the DPLL puts out a signal based on the last known "good" frequency of the external references. The final mode of DPLL operation is the free-run mode. Here, the DPLL is instructed to put out a signal in the

approximate center of its range. This mode would only be used if the NCLK2 had to be initialized without any external references available to lock to.

Depending on the particular synchronization plan being used, the NCLK2 DPLL will lock to the external references in one of two ways. For a master/slave network, the DPLL will lock to one of the external references. If that reference fails, the DPLL will then be told to use the backup reference. In a mutually-synchronized network, the DPLL will lock to the weighted average of the phases of all the active references. Depending on the weighting values used, a particular reference can be given greater control over the DPLL output. If a reference is suspected of being bad, it can be removed from the averaging algorithm by assigning it a weight of zero.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Working limits for the individual circuits are in their respective schematic drawing circuit descriptions.

2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for the individual circuits are in their respective schematic drawing circuit descriptions.

3. FUNCTIONS

3.01 Function information for individual circuits are in their respective schematic drawing circuit descriptions.

4. CONNECTING CIRCUITS

4.01 Connecting circuit information is provided in SD-5D075-01

SECTION IV - REASONS FOR REISSUE

1. CHANGED AND ADDED FUNCTIONS

1.01 Options U and X which provided a high stability oscillator were rerated to discontinued availability.

2. CHANGES IN APPARATUS

2.01 Removed
Circuit pack - TN1274

2.02 Added
Circuit pack - TN1274B

2.03 Wiring Added
-48V and GRD for 'OOS' and 'RINH'.

3. DESCRIPTION OF CHANGES

3.01 In FS2 and FS4 lead designations were changed from side A/B to side 0/1 respectively.

3.02 In FS4 clock lead terminations between RCU and FIU were changed. Four surface wires were replaced by two twisted pairs. Added options Z (domestic) and Y (export) reference source wiring. Added note 305.

3.03 In FS2 and FS4 added option T (TN1274B) in place of option Z (TN1274).

3.04 In FS1 and FS3 added -48V and ground for 'OOS' and 'RINH' operation. Added note 306.

3.05 In option index rerated options U and X (high stability oscillator).

3.06 In FS2 and FS4 added -48V and ground for 'OOS' operation and current limiting resistor for 'OOS' led.

3.07 In FS1 and FS2 wiring was corrected for 'ROS' operation.

3.08 In FS1 and FS2 new formed cable design was added between RCU and FIU.

3.09 In the Unit Symbol Table of Contents, corrections were made to 'AL' and 'AK' to have the respective element with the corresponding FIU input.

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