CIRCUIT DESCRIPTION

CD-5D077-01
ISSUE 1
APPENDIX 3B
DWG ISSUE 4B
DISTN CODE AT13

5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH CONTROL UNIT
MODEL 2
CIRCUIT

CHANGES

B.   Changes in Apparatus

Replaced TN70B, TN856B and SN516 circuit packs with TN70C, TN856C and SN516B circuit packs.

D.   Description of Changes

The TN70C and TN856C circuit packs provide additional functionality for feature switching module 2000 (SM2000). The SN516B circuit pack provides additional functionality for the auto power recovery feature. Figure 1 has been changed to reflect changes to apparatus.

Added option T in the feature option table and the information notes for a second direct memory access controller (DMAC) between the communication module 2 (CM2) and the 3B20 for SMs with 400K and greater busy hour calls.

SN516B	495FB	TN856C	TN886	TN856C	UN173	SN516B	495FB	UN25B	UN25B	UN25B	UN25B	UN178	UN199	TN70C	TN69B
MSPU C&D	MSPU CONV	MSPU	PPC	MSPU	FPC	MSCU C&D	MSCU CONV	IOMI A	IOMI B	IOMI C	IOMI D	PIC2	PMCS	BIC	DDSBS
008	024	032	040	048	056	066	082	090	106	120	134	146	156	170	178

Figure 1- Message Switch Control Unit, Model 2,
Layout of Circuit Packs

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DEPT NA5360100-CEH-JBCM

CIRCUIT DESCRIPTION

CD-5D077-01
ISSUE 1
APPENDIX 2M
DWG ISSUE 3M
DISTN CODE AT13

5ESS™ SWITCHING SYSTEMS
MESSAGE SWITCH CONTROL UNIT,
MODEL 2
CIRCUIT

CHANGES

A. Changed And Added Functions

A.1 Add wiring option information for new MLB backplane
     ED5D635-30 allowing it to make dual serial channel assignments
with 963E-2 Connectors (Options V, W, and X) rather than the D-3
wiring (Options Y and Z) used on the wire wrap backplane
ED5D571-30.

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AT&T DEPT 55614-CWR-CEJ

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CIRCUIT DESCRIPTION

CD-5D077-01
ISSUE 1
APPENDIX 1A
DWG ISSUE 2A
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH CONTROL UNIT,
MODEL 2
CIRCUIT

CHANGES

A. Changed and Added Functions

A.1 Add wiring option information to allow the communication module to communicate with the administrative module on channel 11 or 12.

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DEPT 55614-SJL-CWR

5ESS^{TM} ELECTRONIC SWITCHING EQUIPMENT

MESSAGE SWITCH CONTROL UNIT 2
MODEL 2
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The message switch control unit, model 2 (MSCU2) controls the message transfers between the administrative module (AM), and as many as 16 communities, each consisting of one to four peripheral controllers. A peripheral controller (PC) can be a module message processor (MMP), a foundation peripheral controller (FPC) or a pump peripheral controller (PPC). The community with the FPC and PPC is limited to two PCs and is contained within the MSCU2. Message transfers are accomplished via a bit-slice processor called the peripheral interface controller, model 2 (PIC2). The functions of the MSCU2 are as follows:

(a) Perform the serial-to-parallel conversion of data received from the AM, and the parallel-to-serial conversion of data transmitted to the AM via the duplex dual serial bus selector (DDSBS).

(b) Provide a bus interface controller (BIC) to interface the 16-bit PIC2 to the 32-bit DDSBS.

(c) Provide one to four input/output microprocessor interfaces (IOMIs) to interface the PIC2 to the MMPs, FPC, and PPC.

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(d) Provide control over the BIC and IOMIs to transfer data between MMPs or between the AM and MMPs.

(e) Provide control over the BIC and IOMIs to transfer data between the AM and the FPC or PPC.

(f) Perform self diagnostics resident in the pumpable microcontrol store (PMCS).

(g) Provide control and diagnostic access for the dual message interface (DMI), the network clock (NCLK), and the time multiplexed switch, model 2 (TMS2) via the FPC.

(h) Provide a PPC for loading the switch module (SM) with data at a high rate (192k bytes/sec).

(i) Provide both manual and AM control of the MSCU2 from an in-service/out-of-service point of view.

SECTION II - DETAILED DESCRIPTION

A description of each circuit pack in the MSCU2 (as seen in Fig. 1) can be found in this section.

1. DUPLEX DUAL SERIAL BUS SELECTOR

1.01 The DDSBS serves to interface the MSCU2 with the AM dual serial channel (DSCH). Up to 16 DDSBSs can be connected to a single DSCH. All signaling is compatible with EIA standard RS422. Each DDSBS interfaces with the DSCH via connectorized cables, each of which consists of two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The data rate between the DDSBS and DSCH is at 10 MHz.

1.02 To specify the operation type, 4-bit start codes are transmitted to the DDSBS over the two bidirectional data leads. The DSCH issues one of the following seven different start codes to the DDSBS:

(a) Write data in the word mode.

(b) Send device command.

(c) Write data in the block mode.

(d) Read data in the word mode.

(e) Sense DDSBS status.

(f) Read data in the block mode.

(g) End of transfer (EOT).

1.03 Similarly, the DDSBS issues one of the following four completion codes to the DSCH to specify the success or failure of the operation:

(a) All seems well.

(b) Device reported an error.

(c) Invalid DDSBS command.

(d) Illegal start code received.

1.04 The DDSBS receives and decodes the incoming serial message, executes the specified operation with the BIC, and transmits the serial reply message back to the DSCH.

1.05 The DDSBS interfaces with the BIC over information, control, and response leads as follows:

Information — There are 36 bidirectional information leads of which four are parity leads. Information leads are used either to send data or commands to the BIC, or to receive data or status from the BIC.

Control — Five control signals to the BIC are:

Command present (CP),

Data present (DP),

Data request (DR),

Sense status (SST), and

End of transfer (EOT).

Response — Five response signals from the BIC are:

Sync,

Error (ER),

Interrupt (INT),

Transfer (XFER), and

Setup.

2. BUS INTERFACE CONTROLLER

2.01 The BIC acts as a buffer between the 32-bit DDSBS and the 16-bit PIC2. Included in the BIC are a 16-word by 32-bit data FIFO, a 32-bit command register, a 32-bit status register, and a 16-bit sanity timer. The PIC2 can access each of these registers, 16 bits at a time. The BIC buffers data and commands to the PIC2, buffers data and status from the PIC2, and performs the necessary hand shaking to communicate with the DDSBS.

2.02 The FIFO can be accessed by both the PIC2 and DDSBS but not at the same time. Parity checks over transfers between the BIC and DDSBS are always performed by the BIC. Parity checks over transfers between the PIC2 and BIC may or may not be performed by the BIC, depending on the state of an internal flag controlled by the PIC2.

2.03 The command register records commands from the AM destined for the PIC2. The PIC2 may read and, for maintenance purposes, may write this register.

2.04 The timer provided on the BIC is used to maintain the sanity of the MSCU2. The PIC2 has read/write access to the timer, which is incremented once every 5 microseconds. A timer interrupt is issued to the PIC2 at an interval specified in the initialization block from the maintenance software. The PIC2 has 30 ms to reset the timer; otherwise, a sanity error bit will be set to report the detection of an error to the AM.

2.05 The BIC flags are segmented into 16 bits of status and 16 bits of error. The flags are used to request interrupt and Direct Memory Access (DMA) service from the AM, to alert the PIC2 of the presence of an AM command or data requests, and to record the detection of error conditions.

3. PERIPHERAL INTERFACE CONTROLLER, MODEL 2

3.01 The processor used on the PIC2 consists of four 4-bit sliced microprocessors. These bit-slices work together to form a very fast 16-bit microprocessor.

3.02 The microprogram register provides a data latch for the microword from the PMCS. This register contains all control information required to execute a single microinstruction.

3.03 The source and destination register decoders are used to decode 10 bits of the microprogram register into the appropriate register input and output enable signals.

3.04 The arithmetic logic unit (ALU) consists of four 4-bit sliced

Page 3

microprocessors that form a 16-bit microprocessor. The ALU can perform addition, two forms of subtraction, and five logical operations.

3.05 A 16k by 16÷2 parity bit random access memory (RAM) is equipped on the PIC2 to be used as temporary data storage. Associated with the RAM is a 14-bit address sequencer that also provides auto increment function of memory addresses.

3.06 Fifteen vectored interrupt levels are incorporated by priority on the PIC2. A 16-bit mask register is included to individually inhibit or enable selected levels. The MSCU2 interrupt assignments are shown below:

LEVEL	0	Unused - highest priority; unmaskable
LEVEL	1	Microword parity error
LEVEL	2	PIC2 instruction timer
LEVEL	3	BIC command flag, used to alert the PIC2 of the presence of a command from the AM awaiting execution.
LEVEL	4	IOMI-A PC interrupt request (PCIR) summary
LEVEL	5	IOMI-B PC interrupt request (PCIR) summary
LEVEL	6	IOMI-C PC interrupt request (PCIR) summary
LEVEL	7	IOMI-D PC interrupt request (PCIR) summary
LEVEL	8	Unused
LEVEL	9	Unused
LEVEL	10	Unused
LEVEL	11	Unused
LEVEL	12	BIC sanity timer.
LEVEL	13	IOMI parity error
LEVEL	14	Stop the world (STW)

3.07 The microprogram address sequencer provides full control capability to perform normal sequential execution of up to 64k words of microcontrol store. The sequencer also performs conditional and unconditional jumps for the following eight conditions:

(a) Carry.

(b) Overflow.

(c) Negative.

(d) Zero.

(e) BIC data flag.

(f) BIC error summary.

(g) PIC2 data ready.

(h) Intelligent microcontrol store (IMCS) data ready. This condition will only be used in conjunction with the IMCS test board. ·

4. PUMPABLE MICROCONTROL STORE

4.01 The PMCS contains 15k by 48 bits of high speed execution RAM (E-RAM) used by the PIC2 as microcontrol store, and 1k by 48 bits of boot programmable read-only memory (PROM) microcontrol store which contains PIC2 firmware used to pump the E-RAM from the AM disk and to diagnose the PMCS hardware.

The function of each bit, or series of bits within each 48-bit word, follows:

Bits 0-35 form the instruction to be executed by the PIC2. Bits 36-43 are used by the PMCS to determine the instruction execution speed of the microinstruction (instruction speeds can vary from 100 ns to 300 ns in increments of 25 ns). Bits 44-47 are used by the PIC2 to check parity over the 48-bit word.

5. INPUT/OUTPUT MICROPROCESSOR INTERFACE

5.01 The IOMI serves to interface the 16-bit PIC2 with up to four communities of four 8-bit peripheral processors. The MSCU2 can be equipped with up to four IOMIs for a maximum of 16 communities. Selection of the IOMI by the PIC2 is accomplished by data bus bits 0, 1, 2, and 3.

5.02 All signals between the IOMI and the message switch peripheral processors (MSPUs) are at TTL levels. Each community consists of a 16-bit DMA address bus, and 8+1 parity bit bidirectional data bus, eight control signals, and one out-of-level signal. Each of the four peripheral processors in each community has an individual service request (SR), interrupt request (IR), error request (ER), and control signal acknowledge (CSA) signals.

5.03 The interface between the PIC2 and IOMI consists of a 16+2 parity bit data bus, five source signals, and five destination signals for control of the IOMI.

6. MESSAGE SWITCH PERIPHERAL PROCESSOR

6.01 The message switch peripheral processor (MSPP) is the controlling circuit pack of all message switch peripheral controller applications. The MSPP is a single-board processor with an interface through an IOMI bus to the PIC2 and with an interface to application boards needed for each particular function. Contained on the MSPP is a 16-bit microprocessor, 128k bytes of dynamic random-access memory (DRAM), 8k bytes of static RAM, 16k bytes of erasable programmable read only memory (EPROM), and clock circuits to ensure its own sanity as well as to provide needed timing to application boards.

6.02 The interface to the application boards supports either 8- or 16-bit peripherals. Through this interface, the MSPP performs parity generation and checking functions for both the data bus and address bus. Also, DMA operations are supported, allowing efficient data transfers without direct processor involvement.

7. FOUNDATION PERIPHERAL CONTROLLER

7.01 The FPC contains circuitry that performs the following functions:

(a) Provides serial interface to the three subdevices over the control and diagnostic access link (CDAL). This interface is accomplished through a fixed hardware protocol provided by the control and diagnostic access circuit (CDAC). A PROM sequencer is used to provide the necessary control signals associated with the protocol.

(b) Generates maskable interrupt control vectors to the MSPP upon reception of error or service requests from one of the three subdevices.

(c) Selects the active CDAL (0 or 1).

(d) Checks parity of address and data received from the MSPP, and generates parity over the data bus during data transfers to the MSPP.

7.02 On the MSPP microprocessor bus interface, the FPC receives address, address parity, data, data parity, and various control signals. The FPC sends data, data parity, and control signals to the MSPP on this bus.

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7.03 On the CDAL interface, the FPC sends and receives serial data and control signals.

8. PUMP PERIPHERAL CONTROLLER

8.01 The PPC provides the interface for rapidly pumping an SM. Data is pumped from the disk in the AM, through the PIC2, via the IOMI bus, to the PPC. The PPC then sends the data to the communication module control unit (CMCU) via a message interface bus (MIB). The CMCU sends it to the TMS2, where it is distributed to the destination SM via a network control and timing (NCT) link.

8.02 The PPC contains circuitry which performs the following functions:

(a) A pair of 4k byte RAM buffers temporarily store blocks of data written by the MSPP.

(b) An 11-bit word counter generates the RAM buffer address during reads (transmissions to the switch module). An address multiplexer switches the source of the RAM buffer's address from the address counter to the processor's address bus.

(c) A data formatting circuit converts the 16-bit words read from the RAM buffer to 8-bit time slots. Each time slot contains six data bits, a framing bit, and a parity bit.

(d) An 8-bit time slot counter has two functions: it counts the eight bits per time slot and the 32 time slots per frame.

(e) The output data circuit contains a multiplexer that switches idle code or data to the output. A shift register converts the parallel data to serial data, which is outputted on the MIB at a 2 MHz rate.

(f) A 32-by-1 bit RAM performs time-slot selection. Each bit corresponds to one of the 32 time slots and is used to determine which of the time slots will be used for data transmission during SM pump.

(g) Diagnostic circuits check data parity, address parity, data formatting, and the time-slot select RAM.

8.03 Data blocks are transferred in parallel format from the MSPP to the PPC. This interface contains a 16-bit address bus, 16-bit data bus, and various control signals.

8.04 Data blocks are transferred in serial format from the PPC to the DMI on the MIB. This interface contains transmitted data, received data, and 4 MHz clock and sync signals. The maximum data transfer rate is 192k bytes/second.

9. CONTROL AND DISPLAY

9.01 In service/out of service control, and alarming of the power converters is performed by control and display (C&D) circuit packs. The MSCU2 incorporates two C&D packs (Fig. 1). One provides manual and AM control of the FPC, PPC, and their associated MSPPs; the other provides manual and AM control of the PIC2, PMCS, BIC, DDSBS, and the IOMIs. The AM monitors the C&D packs for fuse alarms, power status (alarms, manual off, and power on), and request for out-of-service (OOS).

10. 495FB POWER CONVERTER

10.01 The purpose of the converter is to change a nominal -48 volt input to a well regulated +5 volt output for applications in the MSCU2 circuits. The power unit is pulse-width controlled for regulation, is self-oscillating, and operates at a fixed frequency. The 495FB provides +5 volts at 250 watts. The MSCU2 incorporates two converters (Fig. 1). One provides power for the FPC, PPC, and their associated MSPPs; the other provides power for the PIC2, PMCS, BIC, DDSBS, and the IOMIs.

SECTION III - REFERENCE DATA

1. CIRCUIT PACKS

1.01 Circuit pack CDs reside within the following circuit pack schematics (CPSs).

(a) Duplex Dual Serial Bus Selector (DDSBS) - CPS TN69B.

(b) Bus Interface Controller (BIC) - CPS TN70B.

(c) Pumpable MicroControl Store (PMCS) - CPS UN199.

(d) Peripheral Interface Controller, Model 2 (PIC2) - CPS UN178.

(e) Input Output Microprocessor Interface (IOMI) - CPS UN25B.

(f) Power Converter - CPS 495FB.

(g) Control and Display (C&D) - CPS SN516.

(h) Foundation Peripheral Controller (FPC) - CPS UN173.

(i) Pump Periphral Controller (PPC) - CPS TN886.

(j) Message Switch Peripheral Processor (MSPP) - CPS TN856B.

2. WORKING LIMITS

(a) Voltages

1. -42.75 to -52.5 volts (Nominal -48 volts).

(b) Ambient Temperature

1. 2 to 70 degrees Celsius (maximum air temperature at frame outlet).

2. 2 to 50 degrees Celsius (aisle ambient, fan inlet).

3. CONNECTING CIRCUITS

(a) Message Switch Peripheral Unit, Model 3 (MSPU3) - SD-5D078-01.

(b) Communication Module Control Unit (CMCU) - SD-5D060-01.

(c) Fuse/Filter Panel - SD-5D084-01.

(d) Input Output Processor (IOP) - SD-4C101-01.

(e) Dual Serial Channel (DSCH) - SD-4C099-01.

SN516	495FB	TN856B	TN886	TN856B	UN173	SN516	495FB	UN25B	UN25B	UN25B	UN25B	UN178	UN199	TN70B	TN69B
MSPU C&D	MSPU CONV	MSPP	PPC	MSPP	FPC	MSCU C&D	MSCU CONV	IOMI A	IOMI B	IOMI C	IOMI D	PIC2	PMCS	BIC	DDSBS
008	024	032	040	048	056	066	082	090	106	120	134	146	156	170	178

Fig. 1 - Message Switch Control Unit, Model 2,
Layout of Circuit Packs

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DEPT 55612-MFD-DPS