5ESS® SWITCHING EQUIPMENT MESSAGE SWITCH PERIPHERAL UNIT, MODEL 3 CIRCUIT

CHANGES

B. Changes in Apparatus

Replaced the TN856C and SN516B circuit packs.

D. Description of Changes

The TN856C circuit pack provides additional functionality for the feature switching module 2000 (SM2000). The SN516B circuit pack provides additional functionality for the auto power recovery feature.

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5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
MODEL 3
CIRCUIT

CHANGES

D. Description of Changes

D.1 Modify Figure 1 for Dual Module Message Processor (DMMP) equipage in the B Community. Remove Figure 2 (MSPU1) from this CD.

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MESSAGE SWITCH PERIPHERAL UNIT, MODEL 3
CIRCUIT

CHANGES

D. Description of Changes

D.1 Document lug location differences on the two backplanes used on the unit.

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5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT, MODEL 3
CIRCUIT

CHANGES

D. Description of Changes

D.1 Clarification of feature and option table.

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5ESS™ SWITCHING SYSTEM
MESSAGE SWITCH PERIPHERAL UNIT
MODEL 3
CIRCUIT

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Message Switch Peripheral Unit, Model 3 (MSPU3) is a part of the Communications Module 2 (CM2) for the 5ESS™ Switching System multi-module office. The minimum configuration for a simplex CM2 includes one Message Switch Control Unit, Model 2 (MSCU2), one Communication Module Control Unit (CMCU), one Time Multiplexed Switch, Model 2 and one MSPU3 to support up to 32 Switching Modules (SMs). The CM2 can accommodate additional MSPU3s to support up to 192 SMs.

2. GENERAL DESCRIPTION OF OPERATION:

2.01 MSPU3 provides two communities, with each community being able to house up to four 2-board Module Message Processors (MMPs). The MMPs are the communication processors that provide for the interchange of messages with SMs using the BX.25 protocol. Each MMP is equipped to handle communications with up to eight SMs. Figure 1 illustrates this configuration along with the circuit packs used in the MSPU3.

2.02 The characteristics of the MSPU3 are:

A. The MSPU3 can accommodate two communities of four 2-board MMPs.

B. Each MMP supports up to eight fixed time slot channels. When equipped with four 2-board MMPs, there are 32 time slot channels per community. Each time slot in a community is allocated to a different SM.

C. The MSPU3 interfaces to the CMCU by the Message Interface Bus (MIB).

D. The MSPU3 interfaces to the MSCU2 by the Input/Output Microprocessor Interface (IOMI) bus.

E. Each MMP community of the MSPU3, may consist of one

Control and Display (C&D) pack, a power converter and up to four 2-board MMPs.

SECTION II - DETAILED DESCRIPTION:

There are two communities (side A and side B) in a MSPU3 unit. Community side A contains Functional Schematic 1 and 2 (FS1 and FS2) and community side B contains Functional Schematic 3 and 4 (FS3 and FS4). FS1 and FS2 contain the Module Message Processors (MMPs) and the Control and Display of side A respectively. FS3 and FS4 also contain the MMPs and Control and Display of side B respectively.

Each community can handle up to four 2-board MMPs (32 time slots). The 2-board MMP is an Input/Output processor capable of supporting eight message links from the MSCU2, through the TMS, and to the SMs.

1. FUNCTIONAL SCHEMATIC 1

1.01 Module Message Processor - Side A: FS1 can provide up to four MMPs which are MMP0 (Symbol 1 & 2), MMP1 (Symbol 3 & 4), MMP2 (Symbol 5 & 6) and MMP3 (Symbol 7 & 8). Each MMP consists of two circuit packs: the TN856B Message Switch Peripheral Processor (MSPP) and the TN870 Message Interface Bus Controller (MIBC).

1.02 Symbol 1 (Message Switch Peripheral Processor 0) - TN856B: The TN856B of MMP0 is the controlling circuit pack of all message switch peripheral controller applications. The MSPP is a single-board processor with an interface through an IOMI bus to the MSCU2 and an interface to application boards needed for each particular function. Contained on MSPP is a 16-bit microprocessor (Intel 8086), 128 Kbytes of dynamic random-access memory (DRAM), 8 Kbytes of static RAM, 16 Kbytes of erasable and programmable read-only memory (EPROM), and clock circuits to ensure its own sanity as well as to provide needed timing to application boards.

The interface to the application boards supports eight 8- or 16- bit peripherals. Through this interface, the MSPP performs parity generation and checking functions for both the data bus and address bus. Also, Direct Memory Access (DMA) operations are supported allowing efficient data transfers without direct processor involvement.

1.03 Symbol 2 (Message Interface Bus Controller 0) - TN870: The TN870 of MMP0 contains the custom protocol chips (XPC8s) and the CMOS Message Interface Bus Controller (CMC) chip for selecting eight transmit and eight receive time slots on the MIB. This board provides multiplexing between the 2 Mb/s MIB serial rate and the 48 Kb/s XPC serial rate, with parity insertion and checking on the MIB. It is controlled through the MSPP's microprocessor address, data and control busses.

Through multiplexers here, and in the SM, dedicated links are supported by this board between the MMP and the SMs. The XPC chips process messages according to strict interpretation of level 2 BX.25 protocol. The XPC chip's interfaces to the system are through a duplex 48 Kb/s serial port to the MIB multiplexing circuitry and an internal dual channel DMA controller which accesses memory on the MSPP board. The Dual Access Memory (DAM) of the TN856B acts as the interface buffer between the Peripheral Interface Controller (PIC) in the MSCU2 and the MSPP. It is implemented with 8K static RAM.

The MSPP receives messages destined for the SM in DAM, transfers it to dynamic RAM and writes an XPC lookup table (also in dynamic RAM). The XPC chip

makes use of pointer and message length information in the lookup table to program its internal DMA controller. The XPC chip then transfers the message to the serial MI bus via DMA cycles into dynamic RAM. Messages traveling in the reverse direction are handled similarly.

The CMC chip provides the interface from the MIBs to the XPCs. This interfacing function consists of multiplexing and demultiplexing between the 2.048 Mb/s MIB serial data rate and the 48 Kb/s XPC serial data rate, with parity checking and generation over both the transmit and receive portions of the interface. It provides access to eight transmit and eight receive time slots to and from the MIB.

1.04 Symbol 3 (Message Switch Peripheral Processor 1) - TN856B: The TN856B of MMP1 provides the same functions as symbol 1 (see II-1.02).

1.05 Symbol 4 (Module Message Processor 1) - TN870: The TN870 of MMP1 provides the same functions as symbol 2 (see II-1.03).

1.06 Symbol 5 (Message Switch Peripheral Processor 2) - TN856B: The TN856B of MMP2 provides the same functions as symbol 1 (see II-1.02).

1.07 Symbol 6 (Module Message Processor 2) - TN870B: The TN870 of MMP2 provides the same functions as Symbol 2 (see II-1.03).

1.08 Symbol 7 (Message Switch Peripheral Processor 3) - TN856B: The TN856B of MMP3 provides the same functions as symbol 1 (see II-1.02).

1.09 Symbol 8 (Module Message Processor 3) - TN870: The TN870 of MMP3 provides the same functions as symbol 2 (see II-1.03).

1.10 Symbol 9 (Bus Terminating Resistors) - BTR1: The BTR1 is a 2x12 paddle board with terminating resistors and it is located on the wiring side of the unit. The BTR1 is used to terminate both MIB 0 and MIB 1 from the MSCU2. Each of the MIB signals is tied to ground through a 110 ohm resistor.

2. FUNCTIONAL SCHEMATIC 2

2.01 Control and Display - Side A: FS2 contains one SN516 Control and Display (C&D) circuit pack and a 495FB Power Converter.

2.02 Symbol 1 (Control and Display) - SN516: The SN516 circuit pack is used for controlling and monitoring power for community side A. The following functions are provided by the SN516:

A. Allow to power converter on/off and request a unit either in service or out-of-service.

B. Display the status of the power circuits such as power alarms, fuse alarms and unit status such as out-of-service, request out-of-service, request restore and request in-progress.

C. Software interface is in the form of scan points to report alarms and signal distributor points to light status LEDs.

2.03 Symbol 2 (495FB Power Converter) - 495FB: The purpose of the converter is to provide a means of converting nominal -48 volt input to a well regulated +5 volt output for applications in the MSPU3 circuits. The power unit is pulse width controlled for regulation, self-oscillating and operated at a fixed frequency. The 495FB provides +5 volts at 250 watts.

3. FUNCTIONAL SCHEMATIC 3

3.01 Module Message Processor - Side B: FS3 can also provide up to four MMPs which are MMP0 (Symbol 1 & 2), MMP1 (Symbol 3 & 4), MMP2 (Symbol 5 & 6) and MMP3 (Symbol 7 & 8). Each MMP consists of two circuit packs: the TN856B Message Switch Peripheral Processor (MSPP) and the TN870 Message Interface Bus Controller (MIBC).

3.02 Symbol 1(Message Switch Peripheral Processor 0) - TN856B: The TN856B of MMP0 provides the same functions as symbol 1 of FS1 (see II-1.02).

3.03 Symbol 2 (Module Message Processor 0) - TN870: The TN870 of MMP0 provides the same functions as symbol 2 of FS1 (see II-1.03).

3.04 Symbol 3(Message Switch Peripheral Processor 1) - TN856B: The T856B of MMP1 provides the same functions as symbol 1 of FS1 (see II-1.02).

3.05 Symbol 4 (Module Message Processor 1) - TN870: The TN870 of MMP1 provides the same functions as symbol 2 of FS1 (see II-1.03).

3.06 Symbol 5 (Message Switch Peripheral Processor 2) - TN856B: The TN856B of MMP2 provides the same functions as symbol 1 of FS1 (see II-1.02).

3.07 Symbol 6 (Module Message Processor 2) - TN870: The TN870 of MMP2 provides the same functions as symbol 2 of FS1 (see II-1.03).

3.08 Symbol 7 (Message Switch Peripheral Processor 3) - TN856B: The TN856B of MMP3 provides the same functions as symbol 1 of FS1 (see II-1.02).

3.09 Symbol 8 (Module Message Processor 3) TN870: The TN870 of MMP3 provides the same functions as symbol 2 of FS1 (see II-1.03).

3.10 Symbol 9 (Bus Terminating Resistors) - BTR1: The BTR1 of community side B provides the same functions as symbol 9 of FS1 (see II-1.10).

4. FUNCTIONAL SCHEMATIC 4

4.01 Control and Display - Side B: FS4 also contains one SN516 Control and Display (C&D) circuit pack and a 495FB Power Converter.

4.02 Symbol 1 (Control and Display) - SN516: The SN516 circuit pack of community side B provides the same functions as symbol 1 of FS2 (see II-2.02).

4.03 Symbol 2 (495FB Power Converter) - 495FB: The 495FB pack of community side B provides the same functions as symbol 2 of FS2 (see II-2.03).

5. EXTERNAL INTERFACES (CADS)

5.01 Cads 01. All input and output points to the unit are listed in CAD 01. They are grouped by function and alphabetized by net name.

5.02 Cads 02 to 03. Cad 02 (side 0) and cad 03 (side 1) comprise the MIB cabling used to interface MMPs side A of the MSPU3 with the Dual Message Interface (DMI) of the CMCU. Each MIB cable consists of eight leads. Because a differential interface is used, positive and negative leads of a particular signal are twisted, thus forming four pairs of twisted unidirectional signal. Three of these signals are terminated at the MSPU3, they are - received data (2MHz rate), 4MHz clock and a 124 usec sync pulse. The remaining signal is for the

transmitted data (2MHz rate) from the MSPU3 to the CMCU.

5.03 Cad 04. Cad 04 comprises the Input/Output Microprocessor Interface (IOMI) bus which is the hardware interface between the MSCU2 and community side A of the MSPU3. The signals are unidirectional (with the exception of the data bus and data parity bit) and paired with ground.

5.04 Cad 05. Cad 05 comprises the scan and distribute cable used in conjunction with FS2 and FS4. Both communities of the MSPU3 report to Input/Output Processors (IOP) side 0 by 6 scan points. Two will be used to request out-of-service and the others will monitor the unit powers (blown fuse, converter shutdown). The four distribute points are used to control the LEDs on the C&D packs. Two are used to drive the "out-of-service" LED and the others are used to drive the "request in progress" LED.

5.05 Cad 06. Same function as "Cad 05" (see II-5.04) but this cable connects to IOP side 1 instead of side 0.

5.06 Cad 07. Cad 07 is the input manual override and diagnostic cable and it is used to connect community side A to the MSCU2 or to another MSPU3 unit.

5.07 Cad 08. Cad 08 is the output manual override and diagnostic cable and it is used to connect community side B to the next MSPU3 unit.

5.08 Cad 09. Cad 09 comprises the Fuse alarm cable used to connect community side A to the Fuse panel.

5.09 Cad 010. The power converter of community side A of the MSPU3 is connected to the fuse block by a hot lead -48 volts and a ground potential lead, 49R (return).

5.10 Cad 011. Cad 011 referred to as staging points, was also created for documentation reasons. Because the MSPU3 was designed with the intentions of it being able to support future designs, a common bus was wired to all peripheral slots. The 2-board MMPs only use a portion of the bus. The remaining leads which are not used are documented here.

5.11 Cad 012. Cad 012 documents a 2x12 paddle board which is located on community side A of the MSPU3 backplane. The paddle board is used to terminate both MIB 0 and 1. Each of the signals in the MIB are tied to ground through a 110 ohm resistor.

5.12 Cad 013 to cad 014. Same function as "Cad 02 to cad 03" (see II-5.02) but they are used for community side B instead of side A.

5.13 Cad 015. Same function as "Cad 04" (see II-5.03) but it is used for community side B instead of side A.

5.14 Cad 016. Cad 016 comprises the Fuse alarm cable used to connect community side B to the Fuse panel.

5.15 Cad 017. The power converter of side B of the MSPU3 are connected to the fuse block by a hot lead -48 volts and a ground potential lead, 48R (return).

5.16 Cad 018. Same function as "Cad 011" (See II-5.10) but these are the staging points for side B instead of side A.

5.17 Cad 019. Cad 019 documents a 2x12 paddle board which is located on community side B of the MSPU3 backplane. The paddle board is used to terminate both MIB 0 and 1.

Each of the signals in the MIB are tied to ground through a 110 ohm resistor.

5.18 Cad 020. Cad 020 documents the ground straps in the MSPU3. These ground straps provide better grounding between units in a Message Switch cabinet.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltages:

A. -42.75 to -52.5 volts. (Nominal -48 volts)

1.02 Ambient Temperature:

A. 0 to 70 degrees Centigrade (at circuit pack).

B. 0 to 50 degrees Centigrade (office aisle ambient).

2. CONNECTING CIRCUITS

2.01 Message Switch Control Unit Model 2: SD5D077-01

2.02 Communication Module Control Unit: SD5D060-01

2.03 Fuse/Filter Panel: SD5D146-01

2.04 Input Output Processor: SD5D053-01

3. REFERENCES

1. K. E. Sallese, Module Message Processor Circuit Description - November 16, 1983, 55612-831116.01IM.

2. J. L. Gray, Two Board Module Message Processors - September 22, 1982, 40288-600.01IM.

3. Bell System Practices - November 1983.

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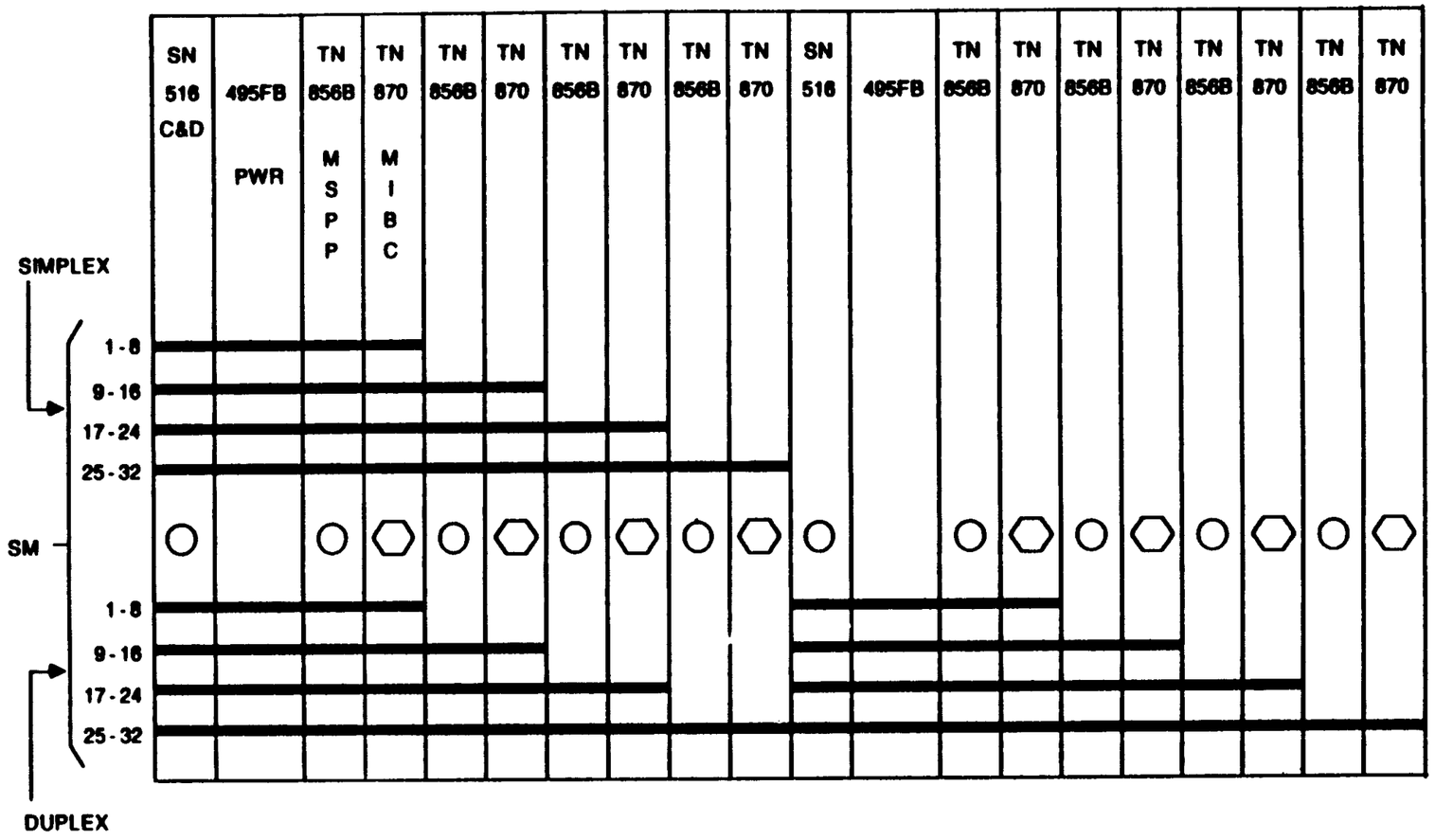
DEPT. 55612-TDN-DD

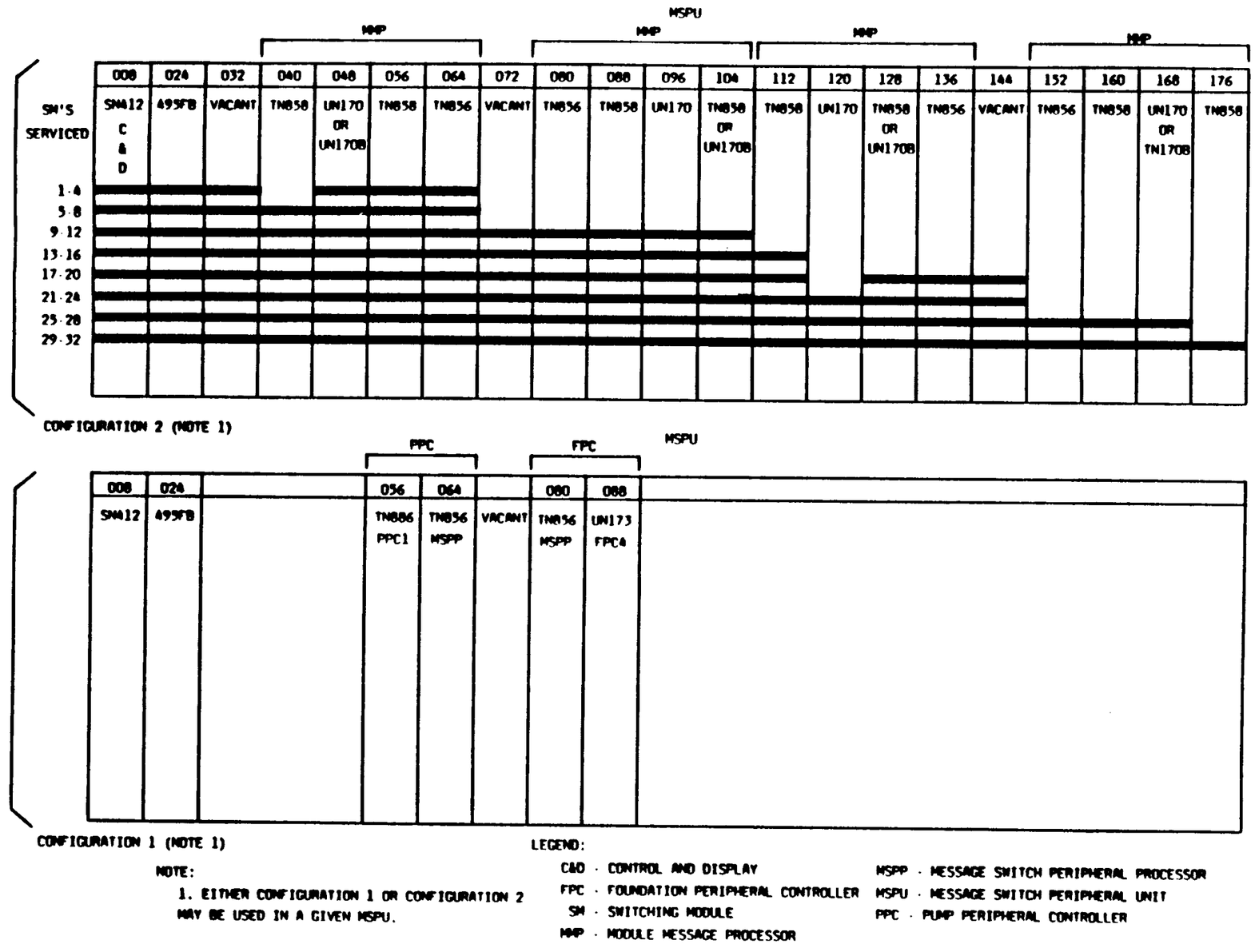


SD-5D078-01 J5D020AC-1 ED-5D523-30

Message Switch Peripheral Unit, Model 3 (MSPU3)
MMP Equipped

IHL41668A01

Figure 1



NOTE:

1. EITHER CONFIGURATION 1 OR CONFIGURATION 2 MAY BE USED IN A GIVEN MSPU.

LEGEND:

C&D · CONTROL AND DISPLAY
FPC · FOUNDATION PERIPHERAL CONTROLLER
SM · SWITCHING MODULE
MMP · MODULE MESSAGE PROCESSOR
MSPP · MESSAGE SWITCH PERIPHERAL PROCESSOR
MSPU · MESSAGE SWITCH PERIPHERAL UNIT
PPC · PUMP PERIPHERAL CONTROLLER

IML41668A02

Message Switch Peripheral Unit (MSPU) Circuit Packs

Figure 2