CIRCUIT DESCRIPTION

CD-5D082-01
ISSUE 2
APPENDIX 4B
DWG ISSUE 7B
DISTN CODE BT13

**5ESS® SWITCHING EQUIPMENT
MESSAGE INTERFACE/CLOCK UNIT,
MODEL 2
CIRCUIT**

CHANGES

D.   Description of Changes

FS4, symbol no. 1 had reference to option "S" and option "R" information added.

FS4, symbol no. 2 had references to options "P" and "B" and options "N" and "A" information added.

FS4, symbol no. 3 had reference to option "M" and option "L" information added.

FS4, symbol no. 4 had references to options "K", "H", "F", and "D" and options "J", "G", "E" and "C" information added.

Apparatus figures 9, 11, 15, 16, 17, 18, 19 and 22 have been expanded to show new, additional options.

"Information Note" 302 has been modified to show new options.

"Information Note" 303 has been updated.

"Information Note" 304 has been expanded to include two new microcode controlled circuit packs and information about additional circuit packs required to bring this SD into agreement with the J drawing.

"Information Note" 308 has been added for clarification.

AT&T BELL LABORATORIES

DEPT NA5301700-RKVS-SDS

CIRCUIT DESCRIPTION

CD-5D082-01
ISSUE 2
APPENDIX 3M
DWG ISSUE 6M
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT
MESSAGE INTERFACE/CLOCK UNIT,
MODEL 2
CIRCUIT

CHANGES

D. Description of Changes

D.1 Apparatus Figure 22 is added to include the High Stability, Stradum 2 Network
Clock Controller, MC5D222 (TN1276).

D.2 Note 302 is corrected to bring the SD into agreement with the J drawing.

D.3 MC5D222 (TN1276) is added to note 304.

D.4 Apparatus Figure 13 is corrected to break it into Apparatus Figure 13 and
Apparatus Figure 14.

AT&T BELL LABORATORIES

DEPT NFNW260570-ALT-MG

CIRCUIT DESCRIPTION

CD-5D082-01
CD ISSUE 2
APPENDIX 2AC
DWG ISSUE 5AC
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT
MESSAGE INTERFACE/CLOCK UNIT
MODEL 2
CIRCUIT

CHANGES

B. Changes in Apparatus

1 1. Superseded   Superseded By

TN1274 Circuit Pack   TN1274B Circuit Pack IN App Fig. 14   IN App
Fig. 14 "U" Option   "T" Option

D. Description of Changes

D.1 A Network Clock 2 Synchronizer Circuit Pack, TN1274B Option
     "T", which is compatible with the lower input levels generated
by the analog reference frequency (BSRF), replaces TN1274 Circuit
Pack Option "U" on a Class A basis for those domestic toll or
tandem applications using Stratum 2-Network Clock 2 and the analog
(BSRF) reference frequency.

D.2 The TN1274B Circuit Pack will be introduced on an after date
     "B" basis for all new products.

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DEPT 55614-CJW-ALT

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5ESS^{TM} SWITCHING EQUIPMENT
MESSAGE INTERFACE/CLOCK UNIT,
MODEL 2
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added the following Information Note 307:
"When   network   clock 2   is   provided,   software
Generic 5E2(2) or later is required for domestic uses,
and 5EE1(2) or later is required for export uses."

D.2 In Information Note 302, added reference to Information
Note 307 for features specifying network clock 2.

AT&T BELL LABORATORIES

DEPT 55614-ALT-TWF

5ESS™ SWITCHING EQUIPMENT
MESSAGE INTERFACE/CLOCK UNIT
MODEL 2
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF UNIT

1.01 The message interface/clock unit model 2 (MICU2) houses three sub-devices which are the message interface (MI) link interface (LI) and the network clock (NCLK). The message inter-face consists of four circuit packs which provide the message time slot distribution function between the LI and up to eight communities of module message processors (MMPs) and the distribution of the control and diagnostic access link (CDAL) for the foundation peripheral controller (FPC) with the time multiplexed switch (TMS), NCLK, LI and MI.

1.02 The link interface consists of two circuit packs which interface between the MI and the network control and timing (NCT) links which are the fiber optic communications paths to the TMS. The LI contains a link interface circuit, a clock circuit, and a control circuit.

1.03 The network clock synchronizes the 5ESS offices with an external reference and provides the office with this uniform clock. The NCLK in MICU2 has two major versions; Network Clock Model 1 (NCLK1), and Network Clock Model 2 (NCLK2). NCLK2 provides additional capabilities over NCLK1 and will eventually replace the NCLK1 as the only 5ESS network clock.

SECTION II - DETAILED DESCRIPTION

1. MI HARDWARE CIRCUIT DESCRIPTION

1.01 The message interface (MI) is the interchange for the transmission of the message (control) time slots between the link interface (LI) and up to eight communities of module message processors (MMPs). Its main function is the management of the control data contained in each time slot during transmission between the LI and the MMPs.

1.02 The MI was designed to operate in conjunction with the LI to provide the message switch (MSGS) with the interface for the duplex transmission of the 256 message time slots with the time multiplex switch (TMS). The LI provides the network control and timing (NCT) interface with the TMS to allow for the serial transmission of the message time slots over the fiber optic link. The MI provides the synchronous interface with eight communities of MMPs to allow for the duplex transmission of the BX.25 protocol data with the HDLC subdevices on each MMP. Several key features of the MI are its capability of time slot switching, transmission of central processor intervention (CPI) and its interfacing of the control and diagnostic access link (CDAL).

1.03 The MI consists of four circuit packs which are MI 1 (TN859), MI 2 (TN860), MI 3 (TN861) and MI 4 (TN862). MI 1 provides two separate functions: the control and diagnostic

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access link (CDAL) and the distribution of the BX.25 protocol data from the LI to eight communities of MMPs. CDAL is a serial communications channel that provides the foundation peripheral controller (FPC) with access to the TMS, network clock (NCLK), LI and MI. This link is used to provide the central processor (CP) with a mechanism to control those subdevices not serviced by a control time slot. This board also provides the interfaces and sequence generators needed in extracting the control information from the message time slots received from the LI and converting them into serial format for transmission to the eight communities of MMPs. MI 2 (TN860) provides the interfaces and the timing sequencers necessary for the transmission of the BX.25 protocol control data from eight communities of MMPs to the LI. MI 3 (TN861) is the processor control interface for the MI complex. It provides the serial interface to the CDAL which supplies a communication channel with either side FPC. This board acts as an I/O port for initializing and controlling the special features provided by the MI. MI 4 (TN862) contains the hardware structure for the distribution of the message interface bus (MIB) network. The MIB is the communications link between the MI and a community of MMPs.

2. MI 1 (TN859) HARDWARE DESCRIPTION

2.01 MI 1 (TN859) receives all 256 message time slots from the LI via a 4-bit wide unidirectional synchronous data bus with a transmission rate of 8.192 MHZ. The 16 bits of each time slot are sent four bits (a nibble) at a time. This translates into an MI time slot rate of 2.048 MHZ.

2.02 Each of the four nibbles is stored in a register to facilitate (odd) parity which checks across each time slot. After parity is checked, only the control byte (bits 0 to 7) is used for transmission to the MMPs. Bits A through P are discarded, since the control information in BX.25 protocol format is contained in bits 0 to 5. At present, bit 6 contains no useful data and is maintained to simplify synchronous operations. Bit 7 is overwritten and used to create odd parity across the eight bits; then each of these control bytes is loaded into one of the eight parallel-to-serial converters.

2.03 Time slot distribution from the MI to eight communities of MMPs is handled by a load pulse generator and eight parallel-to-serial converters. The converters are the source of the transmit data for each MIB with one converter dedicated to each of the eight MIBs. The converters reformat the parallel byte into a serial data stream for transmission to a community of MMPs. Each converter handles every eighth time slot and with the message time slots evenly distributed over the eight MIBs; each bus handles 32 time slots.

2.04 Associated with the synchronous transmission functions are three control registers and two error sources registers. The control registers provide the capability of forcing errors in certain miscellaneous points in the board's operation. The maintenance philosophy is to exercise the error detection schemes by forcing errors in order to verify proper operation. The error source registers monitor several points along the synchronous transmission path to provide error detection capability.

2.05 Two energy detectors are provided to monitor clocks used by the MI in transmission with the MMPs. One is the MIB clock because it controls the data flow between the MI and MMP. The other detector is on the 8 KHZ sync pulse, because it is used to provide a

frame rate reference for each of the eight MIBs.

3. MI 2 (TN860) HARDWARE DESCRIPTION

3.01 MI 2 (TN860) provides the interface and the timing sequencers necessary for the transmission of the BX.25 protocol control data from eight communities of MMPs to the LI. Architecturally, this board has eight serial input buses, one associated with each MIB. At the front of each bus is an input multiplexer circuit. It terminates the two receive data buses associated with the cross-coupling of the MMPs. This gives the MI the capability to select a time slot from the same side MMP or its mate MMP. The selection of the serial data stream from the active side is accomplished by initializing the input multiplexer circuit. It consists of a data selector and a time slot switching register.

3.02 The information necessary to sequence the hardware for relation of the active control byte is received from time slot switching memory on the processor control interface board (MI 3). This binary data is sent from memory to the time slot switching register where it is stored. This register feeds the selector inputs to the multiplexer. The inputs are decoded to provide for propagation of the active control bytes from the selected input and onto the serial bus. Each serial input bus is terminated by a serial-to-parallel converter to change the control information from serial into parallel format for transmission to the LI. The outputs of the converters are tied to a common parallel bus. The converters are sequenced to allow one of the eight access to the bus.

3.03 The central processor intervention (CPI) bit for each time slot is inserted into the bit seven position of the control byte,

when it is loaded into the LI buffer register. The CPI bit is transmitted from the sequence generator located on the processor control interface board (MI 3).

3.04 The function of the LI buffer register is to hold the control information for each time slot prior to transmission to the LI. The transmission of each nibble to the LI is via the time slot interchange 0 transmit bus. This unidirectional, synchronous bus has a data rate of 8.192 MHZ. With four nibbles comprising the 16-bit time slot, the time slot rate is 2.048 MHZ.

4. MI 3 (TN861) HARDWARE DESCRIPTION

4.01 MI 3 (TN861) is the processor control interface for the MI complex. It provides the serial interface to the CDAL which supplies a communication channel with either side foundation peripheral controller (FPC). The serial interface to the CDAL circuit acts as an I/O port for initializing and controlling the special features provided by the MI. The hardware structure of this board incorporates the serial interface for FPC communication, several error source and control registers as well as the time slot switching and central processor intervention functions.

4.02 The control and diagnostic access link (CDAL) is a serial communications channel that provides the FPC with access to the TMS and each of the three subdevices within the MICU2. The CDAL circuit at the MI provides two functions: first, it provides voltage level conversions for the balanced differential interface; secondary, it provides one mechanism by which the FPC is able to select a communication path to the control interfaces on either the NCLK, LI, MI, or TMS.

4.03 CDAL is cross-coupled in the multimodule office. The FPC

provides the mechanism for controlling which side has access to each CDAL circuit. This is accomplished by an active lead from each FPC to the CDAL circuit on each MI. Feedback of this lead to each FPC allows it to monitor which FPC is active on each side. One FPC makes itself active which forces the other side inactive. Thus, either side FPC can communicate with one or both MICU2s.

4.04 The error source and control registers are used to monitor and test the operation of the MI. The error source registers provide basic checking capability by monitoring parity on the time slot data at various stages in the synchronous transmissions paths. It also provides checks on asynchronous CDAL messages communication and on the operation of the special function circuits. The control registers provide a means for testing key sections of the hardware operations. The bits in each control register provide access to points in both synchronous operation and special function circuits that cause failures to occur. These failures are flagged by the error source registers to verify that an error condition exists. The philosophy behind these test features is to provide a confidence level in the integrity of the operation of the MI. The status register is used in conjunction with several test features to provide a means of monitoring the operation of several functions.

4.05 One of the special features of the MI is time slot switching. This function allows either side of the MSGS to be active on a per time slot basis. This means that the synchronous transmission path between the MI and the MSPUs is cross-coupled. At the transmitting ends of each bus, the MI and MMPs send the time slots to both sides. Therefore, the selection of a time slot from a particular side is performed at the receiving end. In the

MI, this is accomplished by synchronous operation of circuit elements on both MI 2 and the MI 3 boards. On MI 2, this function involves the use of an input multiplexer circuit and a time slot sequencer which are coupled to MI 3 through the time slot switching counter and time slot switching memory.

4.06 Each time slot has a corresponding location in memory that is used to store the bit pattern that sequences the hardware to setup the path for the reception of the control data from the active side. This data is accessed from memory by the time slot counter. The counter is used as a reference for tracking time slot transmission from the MMPs to the MI. Since the memory's address spectrum is on a one-to-one correspondence with the time slot number, the counter's outputs act as an address generator to sequence through memory in synchronization with time slot transmission. The data accessed from memory is then transmitted to the input multiplexer circuits on MI 2.

4.07 Central processor intervention (CPI) is a function through which the central processor (CP) is able to force an interface module (IM) into a known state. CPI effectively provides, through a set of 16 commands initiated by software, a hardware mechanism that forces the controllers in the IM into a configuration that can be determined.

4.08 CPI is accomplished in the MI by a transmitter circuit which generates a 63-12 cyclic code. This sequence is inserted into the bit 7 position of one of the active message time slots for the IM. In the IM, a receiver circuit samples its message time slots for a correct sequence, and decodes the message and takes appropriate action. This feature is a one-way transmission. It is issued to an IM; there is no provision for a response to the CP in a similar manner.

5. MI 4 (TN862) HARDWARE DESCRIPTION

MI 4 (TN862) contains the hardware structure for the distribution of the message interface bus (MIB) network. The MIB is the communications link between the MI and a community of MMPs. Each MIB contains two undirectional data leads, a clock lead and a synchronization lead. This structure provides for the duplex transmission of the message (control) information between the MICU2 and the MSPUs.

5.01 The transmission over the MIBs is synchronous. The clock and sync, which provide the necessary timing signal to allow for communication, are controlled by the MI.

5.02 The data leads are structured to allow the transmitting end to send the control information to both sides. Then the selection of the active side, performed on a per time slot basis, is achieved at the receiving end under software control.

5.03 The architecture of the MSGS provides for the growth of up to eight communities of MMPs from one MICU2. It also specifies that each community be cross-coupled to its mate side MICU2. This strategy allows each community to communicate with an MIB from the same side or from an MIB cross-coupled side. This means that each MICU2 is capable of handling 16 MIBs to communicate with the eight MSPUs on the same side or the eight mate MSPUs on the cross-coupled side.

6. NETWORK CLOCK HARDWARE CIRCUIT DESCRIPTION

6.01 There are two versions of the Network Clock in the MICU2; Network Clock - Model 1 (NCLK1), and Network Clock - Model 2 (NCLK2). Refer to 7.0 through 10.08 for the NCLK1 detailed circuit description and 11.0 through 15.02 for the NCLK2 detailed circuit description.

7. NETWORK CLOCK MODEL 1 (NCLK1) HARDWARE CIRCUIT DESCRIPTION

7.01 Network clock model 1 (NCLK1) is broken down into three circuit packs: synchronizer (TN245 or TN249), digital phase lock loop (TN1130), and controller (TN1131).

8. CONTROLLER UNIT (TN1131) HARDWARE DESCRIPTION

8.01 The controller unit consists of two sections. The first is composed of an 8086 microcomputer system. In the second section are two LSI devices which comprise the serial control link interface to the FPC. The FPC transmits a message to the NCLK1 by writing into its half of a two port RAM within one of these LSI devices. A flag is set in RAM by the FPC to indicate that a message is waiting for the NCLK1. The 8086 answers by writing into the two part RAM and possibly setting the corresponding flag. Information which does not demand the immediate attention of the FPC is provided without any flag. High priority messages to the FPC are sent using the scan points located on one of the LSI devices making up the serial control link. Going the other way, high priority messages to the NCLK1 use distribute points located on the same chip. In either direction of transmission, these points manage to bypass the uP and dual port RAM. An interrupt from NCLK1 to FPC exists for the more urgent messages.

8.02 The NCLK control link interface interconnects the FPC and network clock. The four signaling paths between the FPC and NCLK1 are:

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1. A 1 MHZ clock from the FPC to the NCLK1.

2. A 1 MHZ order message from the FPC to the NCLK1.

3. A 1 MHZ reply message from the NCLK1 to the FPC.

4. An active low interrupt load from the NCLK1 to the FPC.

All 4 signal paths are TTL compatible. The 1 MHZ clock signal works in a burst fashion. It is present only during transmissions. When idle, both the order and reply lines rise to a high level. The clock idles low.

8.03 (Missing pulse detector). The sequential circuitry inside the control link receiver/transmitter (CLRT) must be cleared during idle periods. We can easily accomplish this feat with a missing pulse detector on the 1 MHZ clock line. The 1 MHZ clock bursts for transmissions only. The absence of this clock asserts the absence of any transmissions. The missing pulse detector times out after 1 MHZ clock burst from the FPC, issuing the CLRT clear. The CLRT is the message handler for the NCLK1 control link. Its sole communication comes in the form of a reply to an FPC generated order. The control communications buffer FPC can either read or write any CLRT-CLB location. It extends no further into the NCLK1.

8.04 The CLRT performs a significant task apart from passing messages back and forth between the CCB and FPC. The CLRT allows the FPC direct access and control of various NCLK1 signals. These are the eight scan points and fourteen distribute points of the CLRT, not all of which are used. The eight scan points are ones catchers which hold information on NCLK1 configuration and assorted NCLK1 alarms. The CLRT

status latch which contains the scan point indicators can be employed in combination with the PSR mask latch to cause an interrupt back to the FPC. If a PSR mask latch and the corresponding scan point are both set, an interrupt occurs. In this way, the FPC can receive instant notification of NCLK1 alarms, or it can selectively ignore them. The distribute points (eight of which are active high and six of which are active low) provide FPC control of such activities as CCB clear and µP reset.

8.05 The control-communication buffer (CCB) is the mailbox used for storing and retrieving messages passed between the FPC and NCLK1. The buffer memory contains 124X8 bit RAM locations, half of which are available for writing by each direction of transmission. The buffer memory also contains a set of RAM flags that signal the FPC or NCLK1 controller that a message has been loaded or unloaded, or that something concerning that message is particularly outstanding. Each set of data registers is arranged in eight banks of eight registers apiece. One block of the 62 data registers is available exclusively to the NCLK1 for depositing messages. The other block is reserved for FPC messages.

8.06 In the FPC to µP direction of transmission, the data registers can be written and read by the FPC, but only read by the µP. The register flags are set by the FPC and reset by the µP. The NCLK1 side activity block indicates to the µP that at least one message has been placed in the RAM memory by the FPC.

Messages from the µP to the CCB are written/read using the lower eight bits of the µP data bus along with various µP control leads. Two µP memory writes are required to load a message into the CCB. The same write procedure allows the µP to both set and clear CCB flags.

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The data does not effect the flags and is discarded.

8.07 The uPs most imperative task is in performing the filtering operation for the DPLL. Every 500 μsec it pulls in the phase comparator data and applies a filtering algorithm. The resulting calculation drives the D/A converter and through it, the VCXO, thus closing the feedback loop. The processor also periodically gathers in the data of all error source registers. The CP is continually updated on the condition of the NCLK1. The NCLK1 controller also executes orders from the CP.

8.08 The uP nucleus consists of an 8086 microprocessor chip, clock generator, reset logic, wait state generator, interrupt controller, bus drivers, and transceivers. In this design, the 8086 is connected in the minimum mode. In this mode, the 8086 generates bus control signals itself, so we can do without a bus controller. The 16-bit data handling of the 8086 is vital for rapid calculation of the digital filter function. The system clock for the 8086 is generated by a crystal (14.747 MHZ) controlled Intel 8284 clock generator. The 8284 also synchronizes the reset pulse to the 8086. The wait state generator allows wait states to be inserted into the 8086's bus cycle to compensate for slow I/O or memory. The 8284 clock chip provides synchronization of the wait state circuit to the ready lead of the 8086. Also the 2.41 MHZ output from the 8284 is tapped for CCB system clocking. Finally, the 8086 is reset, when power is applied or upon FPC command.

8.09 When an interrupt occurs, a programmable interrupt controller (AMD9519) flags the 8086 which returns an interrupt acknowledge, and the interrupt controller releases a pointer to a service routine. There are a total of three interrupt inputs to the interrupt controller, each with its own priority level. The highest level is the loss of the 2 KHZ reference coming from the sync board. In the middle is the 500 μsec interrupt, triggered by this same 2 KHZ reference. This interrupt leads the uP into the DPLL filter parameter calculation algorithm. The lowest priority interrupt is a 2 msec timer which provides a base cycle for the uP, acts as a stop watch when timing certain events, and insures fairly regular communication with the FPC. The interrupt controller is the only device in the NCLK1 to be accessed by the uP as an I/O port.

8.10 The address decoder provides the address control signals for registers on each of the other NCLK1 units as well as for the EPROMs, RAMs, and the interrupt controller on the controller board. All addresses are memory mapped with the exception of the interrupt controller which uses two I/O ports. The program memory of the controller is stored in Intel 2732A 4Kx8 EPROMs. Two EPROMs hold the program, with another dedicated to parity bit storage. The variable and stack storage is furnished by 5 1Kx4 bit Intel 2148 RAM chips. In all cases, the data bus is 18 bits wide. (2 msec TIMER) the 2.41 MHZ output of the 8284 clock generator is divided by 5120 to produce a 2 msec clock. The 2 msec clock is applied as a low priority interrupt for the uP. It provides a base level loop for message exchange with the CP. These interrupts are also counted up in software to provide time keeping for maintenance and facility (DS 1) programs. (PARITY CHECKS) Both the EPROM and RAM memory use parity bits generated over both data bytes. The EPROM parity bit is checked during a read. The RAM parity bit is generated during a write and checked during a read. (SANITY TIMER) The sanity timer is a retriggerable one shot which the uP is obligated to reset on a

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periodic (every 48 msec) basis to pro-tect against the possibility of the uP losing its place in the program. When-ever the sanity timer times out, an interrupt to the FPC occurs. (2 KHZ REFERENCES ENERGY DETECTOR) An energy detector hangs off the 2 KHZ reference signal coming from the sync board. The detector is retriggered every 500 u sec by the incoming reference. If the reference is missing, the energy detec-tor alarm interrupts the uP, disabling further DPLL filter calculations and thereby placing the NCLK1 in the hold-over mode. Holdover means that the PLL loop is broken and the DPLL DAC relies on the last value given to it to hold the VCXO at a stable frequency. (CLRT Scan Point Override) The FPC can mani-pulate the scan points by writing to the CLRT distribute points. The over-ride feature itself is regulated by an active low distribute point. (MAINTE-NANCE REGISTER) Maintenance activity on the controller board centers around three registers: the error source register (ESR), the error force regis-ter (EFR) and the error clear register (ECR). The controller ESR takes in information from the parity checker circuit. The controller EFR can force either. type of parity error as well as trip; to 2 KHZ reference energy detec-tion alarm. Old data in the controller ESR is flushed out with the controller ECR. The controller ECR is also used to reassert uP sanity by pulsing the sanity timer every 48 msecs.

9. DS 1 SYNCHRONIZATION UNIT (TN245)

9.01 The function of the DS 1 synchronization unit is to select a reference from one of three possible synchronization sources for each NCLK1. These include a primary and secondary DS 1 line and a cross couple source supplied by the mate network clock. Each DS 1 line terminates on a 2662B transformer followed by a 555N clock extractor circuit. The clock extractor recovers a 1.544 MHZ unipolar clock

from the bipolar PCM bit stream by means of an integrated digital PLL. The center frequency and gain of the internal VCO (astable) is set by exter-nal components. Without a DS 1 line, the clock frequency drifts. Unipolar PCM data is realigned with the recovered clock. Both the 1.544 MHZ clock and data are then introduced into a 140T framer chip, where the PCM sig-nal is inspected for the proper framing pattern. Any error in the framing pat-tern or complete loss of frame gen-erates an error indication to the uP. The uP screens these error indicator every 48 msec.

9.02 The 1.544 MHZ DS 1 clock then goes on to a line switch (SEL DS 1). This switch controls which DS 1 line has been chosen as the possible synchronization reference. The switch is controlled by the 8086 processor, but the result of the switching action is directly readable by the FPC through a CLRT scan point. Generally, one DS 1 line (primary) is preferred over the other. The DS 1 line that is not selected is divided down to 2 KHZ before being sent to a phase detector where any changes in its frequency relative to the selected reference can be monitored. The phase detector is periodically surveyed by the processor. The selected DS 1 reference is also divided by 772 and the resultant 2 KHZ signal is sent to a second switch (active/standby line switch) which decides whether the NCLK1 is active or standby. This switch is also con-trolled by the 8086 and the outcome of the switch is directly readable by the FPC. The 2 KHZ clock that is not selected is then sent to a phase detec-tor where any departure in frequency from the reference can be observed.

9.03 The other input to the active/standby line switch is the 2 KHZ cross couple line coming from the companion NCLK1. It is this signal to which the NCLK1 locks when it assumes

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the standby position in the office. The cross couple signal is balanced, so it must first convert to a single-ended TTL. The presence of the cross couple signal is established with an energy detector. Should the line frequency clip to around 1 KHZ, the energy detector fires. The event is recorded in two ways. It appears directly to the FPC on a CLRT scan point. The pulse is also latched up in a ones catcher flip-flop. From there, the bit is loaded into the sync ESR.

9.04 The 8 KHZ TMS/LI signal returned to the synchronizer serves a sort of handshaking function. The TMS/LI locks to the 8 KHZ NCLK1 output and acknowledges it by returning its own 8 KHZ locked output. In a multimode office the TMS returns the NCLK1 signal. Next, the TMS/LI signal is fed into an energy detector designed to trip whenever the frequency drops below about 5 KHZ. The energy detector reports are returned by either the CLRT scan point or the sync ESR. The TMS/LI signal is divided down to 2 KHZ and put away in a phase register where any frequency disagreement with the selected reference can be measured. If the difference exceeds the threshold set by the µP, the CP is alerted.

9.05 There are three phase registers: alternate phase register, defaulted active/standby phase register, and TMS phase register. A 12-bit binary counter is perpetually clocked by a 2.048 MHZ clock, derived from the DPLL VCXO. The phase registers latch counter data on each leading edge of a 2 KHZ version of either a DS 1 cross couple or the TMS, depending on the particular phase register and sync board switch positions.

9.06 The following is a tabulation of the different registers on the sync board which can be addressed by the µP as memory:

REGISTER NAME	DESCRIPTION
Command Reg.	Controls reference switches and loop-back selection.
Status reg.	Displays reference switch positions, loopback selection, and identifies type of sync board (DS 1 or stand alone).
Error Force Register (EFR)	Exercises energy detectors framer chips, and phase detectors.
Error Source Register (ESR)	Records energy detector alarms, framing and out-of-frame indications.
Phase Exerciser Register	Loads phase counter with 12-bit data from µP.
Alternate Phase Register (ALT)	Contains phase information of DS 1 not selected as the NCLK1 reference.
Defaulted Active/Standby Phase Register (DAS)	Contains information of either the selected DS 1, or the cross couple, depending on the NCLK1s roll in the office.
TMS Phase Register (TMS/LI)	Contains phase information of TMS/LI loopback signal.

timing plan. The fast mode allows one to attain lock much more quickly but makes the clock susceptible to line hits. The normal mode allows bridging of most line hits. Phase builtout and correction to bridge line hits or reference switches are done in software.

10.05 The digital to analog converts has 12 bits of linear accuracy with a 0 to 10 volt full scale output. Trimpots are provided by which the DAC offset and full scale range can be adjusted. A 16-bit DAC register keeps the µP value transferred to the DAC. The lower nibble of this register can be written and read, but it does not affect the DAC. Any change in the other 12 bits of this register is immediately echoed in the DAC, since its load pin is always held low.

10.06 The phase comparators provide a ready supply of low frequency derivatives of the 2.048 MHZ VCXO. From here, we pick off the 8 KHZ signal to be sent to the TMS/LI and the 2 KHZ cross couple going to the other NCLK1 in the office. Although there are two phase comparators, phase comparator A is the boss. So, we take its counter outputs to the periphery. Both the TMS and cross couple outputs are converted into differential signals, while the LI output goes out as TTL. The TMS and LI outputs are both present on the backplane regardless of office size.

10.07 Hanging off the 8 KHZ TMS/LI signal is another energy detector. Its RC components and electrical hooking is a twin to the sync board TMS/LI energy detector. To distinguish it from the other in name, we call this block the VCXO energy detector, since the VCXO is the originator of the signal.

10.08 Five registers on the DPLL board can be accessed by the controller board µP as memory. Enable signals for

each register are furnished by another load address decoder. The latches and their descriptions are charted below:

REGISTER NAME	DESCRIPTION
Error Force Register (EFR)	Exercises the energy detector on the 8 KHZ output.
Error Source Register ESR)	Records the one and only alarm coming from the 8 KHZ output energy detector.
Phase Comparator A	Picks up 12 bits of phase information on the reference signal.
Phase Comparator B	Picks up 12 bits of phase information on the references signal. Serves as a check on phase comparator A.
DAC register	Supplies 12 bits of data to drive the DPLL DAC.

11. NETWORK CLOCK MODEL 2 (NCLK2) HARDWARE CIRCUIT DESCRIPTION

11.01 The Network Clock - Model 2 (NCLK2) provides the timing signal to the 5ESS switching network. The NCLK2 provides additional capabilities over those available with NCLK1. Specifically, the NCLK2 introduces a new architecture that provides the following new capabilities: high-stability operation, multiple reference facilities, and analog references. The NCLK2 consists of three fundamental circuit packs. They are the controller (TN1276), the oscillator (TNs 1283-1286), and the synchronizer (TN1274/TN1275). An additional TN1275

synchronizer pack can be installed if more than four T1 references are required.

11.02 The current NCLK1 design allows the 5ESS system to be used only in medium-stability applications. The NCLK2 will enable the 5ESS system to be used in both domestic and high-stability export applications.

12. NCLK2 CONTROLLER (TN1276) HARDWARE DESCRIPTION

12.01 The TN1276 circuit pack performs many integral functions. First, being the controller for the NCLK2, it handles the communications with the FPC. Secondly, it performs the Digital Phased-lock loop (DPLL) calculations. This pack also handles maintenance on the NCLK2 circuits, its external references, and performs some diagnostics on the NCLK2 under commands from the FPC.

12.02 The DPLL can be operated in four different modes. In the normal mode, the DPLL attempts to track the external references using the normal time constants for that application. In the fast mode, the time constants are reduced to allow the DPLL to achieve lock faster or, in the case of the minor clock side, to track more accurately the cross-couple signal from the major side. The third mode of operation is the holdover mode and is entered whenever problems are detected on the external references. In this mode, the DPLL is no longer locked to the external references. Instead, the DPLL puts out a signal based on the last know "good" frequency of the external references. The final mode of DPLL operation is the free-run mode. Here, the DPLL is instructed to put out a signal in the approximate center of its range. This mode would only be used if the NCLK2 had to be initialized without any external references available to lock to.

12.03 The DPLL also outputs a cross-couple signal to the opposite side NCLK2. The NCLK2 is normally operated such that one side (active-major mode) is providing a timing signal to its associated TMS/LI. The other side NCLK2 (active-minor mode) is forced to lock to this cross-couple signal in order to prevent any slips or errors in the 5ESS switching network when the ONTC sides are switched.

13. NCLK2 SYNCHRONIZER (TN1274/75) HARDWARE DESCRIPTION

13.01 The synchronization pack (TN1274/75) interfaces to the external reference facilities. The TN1274 is the Sync pack for 24 channel synchronization and can interface up to a maximum of two digital and one analog external references. The TN1275 is used for 30 channel synchronization and can interface up to a maximum of eight digital and two analog external references. The NCLK2 locks to the external references in the following way. For a master/slave network, the DPLL will lock to one of the external references. If that reference fails, the DPLL will be told to use the backup reference. After the timing information is extracted, it passes it on to the DPLL. The DPLL then generates the 8 kHz timing signal that is sent to the TMS/LI and locks this signal to the external reference facilities. In the event of a problem detected on the external references or a loss of the external reference signals, the DPLL will continue to provide a signal to the TMS/LI. In this "holdover" mode, the phase of the output signal is based on the last known "good" state of the external references. The stability of the timing signal sent to the TMS/LI during holdover will depend on the stability of the local NCLK2 oscillators.

14. NCLK2 OSCILLATOR (TN1283-1286) HARDWARE DESCRIPTION

14.01 The NCLK2 architecture uses a fixed-frequency time base to perform its function of locking to the external references. This time-base signal is provided by duplicated NCLK2 Oscillator units (NC-OSC), one residing in each MICU2 shelf. Each NCLK2 DPLL has access to both NC-OSC units. Each NC-OSC unit is a unique failure group (separate powering, and alarming) that is separate from the other components of the Office Network Timing Complex (ONTC).

14.02 The NCLK DPLL is instructed, from the Maintenance Software, as to which NC-OSC it should use as its time base. The NCLK2 architecture allows the DPLLs on the two sides of the ONTC to operate either off the same NC-OSC, or with each DPLL using the NC-OSC that is physically located in the same MICU2 shelf. For maintenance reasons, the normal mode of operation will be with both DPLLs using the same NC-OSC unit.

14.03 For stand-alone applications, the NCLK2 will not be synchronized to any external reference facilities. Instead, the NCLK2 will serve as the master timing reference for the switch. In this case, another local oscillator will be used in place of the sync unit on each NCLK2 side. This oscillator will then serve the same function as the external references by providing a signal to which the NCLK2 DPLL will lock.

15. EXTERNAL REFERENCE CONFIGURATIONS (NCLK2)

15.01 The following list summarizes the various combinations of external references that are allowed by the NCLK2 architecture.

- 1 to 2 24-channel digital facilities

- 1 to 8 30-channel digital facilities

- 1 analog reference and 0 to 2 24-channel digital facilities

- 1 analog reference and 0 to 7 30-channel digital facilities

- 2 analog references and 0 to 6 30-channel digital facilities

15.02 There are also restrictions on what type of analog references can be supported by the NCLK2 design. Any analog reference used must be an exact multiple of 250 Hz and must have a maximum frequency of 7 MHz. For the domestic case, the analog reference is assumed to be the Basic Synchronization Reference Frequency (BSRF), operating at a frequency of 2.048 MHz. The minimum signal level allowed at the input to the sync unit is -13 dBm at 75 ohms. For export applications, the analog reference must be constrained to a multiple of 8 KHz, a maximum of 7 MHz and have a signal level in the range of -13 dBm to +10 dBm at 75 ohms.

16. LI HARDWARE CIRCUIT DESCRIPTION

16.01 The link interface (LI) provides an interface to one optical fiber link (NCT) pair which provides the connection from the time multiplexed switch (TMS) to the MICU2. Each NCT link carries data at a 32.768 megabit/second rate. This data is organized into 256, 16-bit time slots per 125 μsec frame. One time slot of each NCT link (designated the message time slot) is used to carry control information to and from the interface module (IM). One bit of each time-slot contains a frame sequence pattern. The NCT link interface obtains frame synchronization to the network via the frame sequence pattern. For interoffice use, the maximum length limit of the NCT link is 1000 feet.

16.02 The LI is the interface to the NCT links. It recovers timing information for these links in order to provide timing for the MICU2. The LI contains the transmit and receive circuitry needed to interface to the optic links. The LI functions are implemented in a two board complex. The complex consists of a TN834 and a TN835 circuit pack. The LI provides the following functions for the MICU2. The LI provides the interface to the network control and timing (NCT) links for the MICU2. The LI recovers clock and data from the incoming NCT links and distributes the resultant clocks and data to the MI. In the opposite direction, the LI receives outgoing data from the MI which is then multiplexed and sourced to outgoing NCT links.

16.03 The LI consists of a link interface circuit, a clock circuit, and a control circuit. The LI interfaces with one pair of NCT links (outgoing and incoming) which provide 256 time slots to and from the MI. Of these 256 time slots, 255 time slots are for message data and data paths to and from the MI with the remaining time slot unused. The incoming 32.768 megabit/second data stream from the NCT link enters the receive (RCV) circuitry in the LI, where it passes through a clock recovery circuit which derives a 32.768 MHZ clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the phase lock loop (PLL) in the clock circuit. The RCV circuit "frames up" on the incoming data stream at the source end of the NCT link (the TMS in a multimodule office and the interface module (IM) in a single module office). The incoming data stream is converted to time slots and written into the buffer circuit (a RAM capable of containing one frame of data).

16.04 The message interface operates from clocks derived at the output of the PLL. When time slots are read from the buffer, parity is checked and regenerated. Normal voice and data time slots are sent to the MI via a nibble bus operating at 8.192 megabits/second. In the return direction, data is selected from the MI and is transmitted to the TMS via the outgoing NCT link. In the transmit circuit, parity is checked and regenerated. The pseudo-random sequence, which is generated in the control circuit, is inserted (one framing bit per time slot). Finally, the time slots are converted to a 32.768 MHZ data stream and transmitted over the outgoing NCT link.

16.05 The clock circuit selects a clock reference from the LI (master mode) or from the mate LI (slave mode). This selected clock is used as a reference for the PLL, which in turn, provides a reference voltage to the voltage controlled crystal oscillator (CVXO). The output of the VCXO is a 32.768 MHZ clock which is divided by the clock circuit and distributed to the remainder of the LI, the mate LI, and the MI.

16.06 The control circuit provides control for the various functions performed by the LIs and clock circuit. Errors from these circuits are latched into error source registers (ESRs) which reside in the control circuit. These control registers and ESRs are accessible for writing and reading by either side of the FPC via the control and diagnostic access link (CDAL). This interface is a 1.875 MHZ serial data link. The data bits that make up the commands are clocked in by a clock which is provided by the FPC, and the command is executed upon the reception of a "go" signal received over a separate lead from the FPC. Parity over address and parity over data is checked in the control circuit. The control circuit provides a serial data link back to the FPC for read

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operations, and an interrupt lead back
to the FPC to indicate that an error
condition exists. Each bit of the ESRs
can be inhibited from causing an inter-
rupt via ESR mask registers.

17. TN834 HARDWARE DESCRIPTION (LI)

17.01 TN834 provides the LI with an
interface to the NCT link and one
message link to the MI. TN834 is com-
posed of the following five functions:

(a) MI interface - transmits and
receives 255 network data time
slots on the NCT link. One time
slot is always looped back to
the MI without transmission over
the NCT link and is dip switch
dependent to determine its time
slot.

(b) Buffer circuit - allows for tim-
ing skews on the received data
from the NCT link.

(c) Transmit circuit - multiplexes
the nibble bus format of data to
a serial NCT link format;
inserts a frame sequence and
buffer check bit in the G and F
bits of each time slot.

(d) Receive circuit - recovery
clock, data, and framing infor-
mation from the incoming NCT
link. Data is then reformated
from serial to 16-bit wide buses
to be sent into the buffer cir-
cuit.

(e) Clock circuit - generates syn-
chronous 16 MHZ, 8 MHZ, 4 MHZ,
and 2 MHZ clocks from a 32 MHZ
clock and 2 MHZ sync pulse from
TN835. These clocks drive all
the circuits on the TN834,
except the receiver.

18. TN835 HARDWARE DESCRIPTION (LI)

18.01 The TN835 provides the LI with a
control interface to the FPC and
a phase locked loop for synchronizing
LI clocks to the network clock. TN835
can be broken down to four basic func-
tions:

(a) Control interface - provides the
FPC access to the control and
error reporting registers in the
DLI.

(b) Control registers - allow the
FPC to control the various func-
tions performed by the LI and
monitor their state.

(c) Error register - accumulates and
latches any errors that occur in
the LI. The FPC can read the
status of these registers to
monitor the health of the LI.
Masking of each individual error
is also provided.

(d) Clock circuit - provides the LI
with a phase locked loop to syn-
chronize all locally generated
clocks to the incoming timing
reference from the NCT link or
NCLK. A cross-couple interface
also provides the ability to
synchronize to the mate LI.

18.02 A link message time slot select
switch (located on the MICU2
backplane) provides the capability of
selecting one out of 256 time slots as
the message time slot for NCT link B.

18.03 (LI cross-couple interface) The
8.192 MHZ clock from side 0 LI
and side 1 LI are required to have less
than a 20 nanoseconds skew between

them. The MI is required to switch its timing source from one LI to the other without causing errors (glitchless switch). The cross-couple interface between the two LIs in an MICU2 is the means by which this glitchless switch is accomplished. This interface consists of four signal leads from side 0 to side 1 MICU2 and four signal leads from side 1 to side 0 MICU2. One of the four leads, (OMATEEN and 1MATEEN) automatically switches the inactive or mate LI to the slave mode, when the active side is programmed to the master mode. In the case of one LI being powered down, this lead is pulled high by the receiving end which allows the mate LI to be put into the master mode when its control register is written. Two of the signal leads are clock lines (8.192 MHZ and 4.096 MHZ) used to drive the PLL of the slave LI. The last signal lead (6MSYN) synchronizes all of the clocks of the slave LI between the frequencies of 2 MHZ and 166 HZ to the clock in the master side. This sync pulse has an active low duty cycle equal to one 8.192 MHZ clock cycle.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Input Voltage

(a) Static -41.75 to -52.5 volts.

(b) Transient - 41.75 to 60 volts

(c) Temperature

0°c to 50°c (office aisle ambient)
0°c to 50°c (at circuit pack)

(d) Cable Lengths

1. Cross-couple cables - The maximum length for the NCLK1/NCLK2 cross-couple cables is 35 feet.

2. The maximum cable length between the NCLK1/NCLK2 and the TMS is 50 feet.

3. For domestic 24-channel references, the maximum distance from the DSX-1 to the NCLK1/NCLK2 is 655 feet.

2. FUNCTIONAL DESIGNATION

2.01 None. (There is a mnemonic listing for the MICU2 backplane). Also designations are described in Section II of this CD.

3. FUNCTIONS

3.01 The functions of this unit are defined in Section II of this CD.

4. CONNECTING CIRCUITS

4.01 This unit has connecting cables to the following units:

(MULTI MOD):   Module Message
                   Processor (MMP)
                   Foundation Peripheral
                   Controller (FPC)
                   Time Multiplexed
                   Switch (TMS)
                   3B IOP unit

(SINGLE MOD ONLY): Interface module (IM)
                   3B IOP unit

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Refer to X Specification X-79935.

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SECTION IV - REASONS FOR REISSUE

1.01 This is the first detailed circuit description and includes all changes up to drawing issue number 3D.

ISSUE 2B:

LDI 1A — was written in order to issue a new artmaster for the MICU2 backplane and correct any documentation that had changed since issue 1.

ISSUE 3D:

LDI 1B — was written to update any documentation that has changed since issue 1A.

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