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5ESS™ SWITCHING EQUIPMENT
TRANSMISSION RATE CONVERTER UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Changed option Y connections from terminal strips in locations 04-021, 061, 109, 149 pins 002 and 003 to locations 04-018, 058, 106, 146 pins 109 and 110.

D.2 This change now agrees with the manufactured product.

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5ESS™ SWITCHING EQUIPMENT

TRANSMISSION RATE CONVERTER UNIT

CIRCUIT

CHANGES

D. Description of Changes

D.1 Added +5 volt sense leads for the 494GB power circuit pack. Also removed backplane surface wires connecting the duplicated terminal designations 8KREF, MSTR, SELREF, and DOOF.

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5ESS™ SWITCHING EQUIPMENT

TRANSMISSION RATE CONVERTER UNIT CIRCUIT

CHANGES

D. Description of Changes

D.1 Add Option Z for use when backplane is used at a remote site.

D.2 Add Option Y for use when backplane is used in the host office.

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5ESS™ SWITCHING EQUIPMENT

TRANSMISSION RATE CONVERTER UNIT CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The transmission rate converter unit (TRCU) provides the time multiplexed switch (TMS) and the switching module (SM) with an interface to standard transmission equipment via the DS3 cross-connect. At the host end of the links, the TRCU is mounted in a miscellaneous frame, while at the remote end, it is mounted in the SM frame.

1.02 The TRCU contains network control and timing (NCT) links to the DS3 rate converter (NDRC) circuit packs, the DS3 interface circuit packs, and power for the NDRC circuit. The NDRC circuit pack provides the NCT to DS3 translation for the transmit half of the link and the DS3 to NCT translation for the receive half of the link. A total of four NDRC circuit packs are required to remote one SM since each circuit pack supports one link.

1.03 The DS3 interface circuit pack supplies equalization and padding of the DS3 bit stream between the NDRC circuit pack and the DS3 cross-connect. Each DS3 interface circuit pack handles two links; thus two of these packs are required to remote one SM. A fully equipped TRCU contains enough packs to remote two SMs.

2. GENERAL DESCRIPTION OF OPERATION

A. TMS to TRCU Interface

2.01 Four NCT links furnish the connection between the TMS and the TRCU. These NCT links are implemented with optical transmitters, optical receivers, and fiber optic cable just as in the standard TMS to SM NCT links. The NDRC circuit pack contains circuitry to detect the presence of two data patterns. One of these patterns is idle code on all time slots, which is used to light an LED to indicate that the link is idle. The other is a string of 32 ones followed by 32 zeros on the G bit. This pattern puts the NDRC circuit pack into the loop mode. The TMS, under diagnostic control, sends this special G-bit pattern to put the NDRC into the loop mode so that it can be diagnosed.

2.02 No power control and display function is provided for the power converters in the TRCU at the host end. The links are monitored for errors by the TMS; a loss of power produces errors which starts the recovery process.

B. DLI to TRCU Interface

2.03 The four NCT links between the TRCU and the data link interfaces (DLIs) are connected by shielded twisted pair because the distance is very short (less than 2 feet). The NDRC circuit pack produces an 8 kHz reference signal by dividing down the incoming DS3 clock. This signal is sent to the DLI as a reference for its phase locked loop. Each of the four NDRC circuit packs provides an 8 kHz reference signal, with only one being selected by the two DLIs. In the NDRC circuit pack, the unselected references are synchronized to the selected reference.

2.04 Two leads from its associated DLI supply an indication to an NDRC circuit pack whether its reference has been selected as the phase locked loop input. One of these leads indicates whether a particular DLI is master or slave, and the other indicates whether the A or B link is being used as a reference.

2.05 The NDRC circuit pack also produces an out-of-frame output. This output indicates whether the NDRC circuit pack can frame up on the incoming DS3 signal. The out-of-frame output signal is sent to the DLI where it forces the phase locked loop to free run if the 8 kHz signal to which it is locking is produced by a clock derived from a bit stream that the NDRC circuit pack cannot frame up on.

2.06 The power control and display function for the power converters in the NDRC is provided by the power control and display circuitry in the DLIs.

C. TRCU to DS3 Cross-Connect Interface

2.07 The interface from the TRCU to the transmission equipment is done at the DS3 rate via the DS3 cross-connect (DSX3). The DSX3 connections are implemented with coaxial cable, with one cable required for receive and one cable required for transmit for each DS3 channel. Each DS3 channel carries the information of one NCT link. Since four NCT links are required to support an SM, four DS3 channels are used to support one optically remoted module (ORM). The four NCT links require eight coaxial cables to connect the TRCU to the DS3 cross-connect.

3. BLOCK DIAGRAM

3.01 See Block Diagram BD 1 on sheet H1 of SD-5D086-01 for a general depiction of the TRCU in a 5ESS™ host/remote application.

SECTION II - DETAILED DESCRIPTION

1. POWER

1.01 A power converter (494GB) is furnished for each pair of NDRC circuit packs. This converter supplies two voltages, +5V and -5V. At the host end, the power converters have no associated control and display function. To turn a converter off, you must release its latch. At the remote end, the control and display function of the associated DLI also services the power converter in the TRCU. Both the NDRC circuit pack and the DS3 interface circuit pack can be removed with the power on.

2. DS3 INTERFACE CIRCUIT PACK

2.01 The distance between the TRCU and the DS3 cross-connect can vary from 0 to 450 feet. To accommodate this varying length, equalization and padding are provided in the TRCU by DS3 interface circuit pack SN563. Equalization is supplied on the receive side, and a manually switchable pad is inserted on the transmit side for distances less than 225 feet.

3. NCT LINK TO DS3 RATE CONVERTER (NDRC) CIRCUIT PACK

A. NCT Receive

3.01 The DLI chip developed for time slot interface unit Model 3 (TSIU3) is used to frame up on the incoming NCT bit stream. The incoming bits are converted to nibbles with a shift register and then sent to the DLI chip. The sync input to the DLI chip is produced from the write 8 kHz output, using a shift register. This sync forces the internal buffer in the DLI chip to be one time-slot in length. The nibble and 8 kHz sync outputs of the DLI chip are loaded into the FIFO.

B. FIFO

3.02 Because the nibbles received from the data link interface chip are asynchronous to the nibbles presented to the multiplexer demultiplexer (muldem) chip, a 64x5 FIFO is used to provide a variable length buffer with reads independent of writes. This FIFO is written at an 8 MHz rate using the same clock that drives the DLI chip. The FIFO is read using an 11 MHz clock from the muldem chip. The read FIFO generator eliminates enough clock cycles from the 11 MHz clock to produce an effective clock of 8 MHz. In every 125-microsecond frame a pattern of six clock pulses and two missing clock pulses is repeated 170 times followed by four clock pulses. Thus, in a full frame, 1024 writes to the FIFO are performed, and 1024 reads from the FIFO are performed.

C. C-Bit Generator

3.03 The C bits in the DS3 format pass the M-frame number over the link. A 10-bit counter that counts from zero to 698 supplies the M-frame number. The MSYNC output from the muldem chip increments the counter once per M-frame. The contents of the counter are loaded into a shift register using MSYNC, and muldem output MCBCLK shifts the value into muldem input MCBD. Once per superframe, the 8 kHz sync from the FIFO synchronizes the C-bit counter and the internal muldem circuitry to the FIFO output.

D. 45 MHz Clock Generator

3.04 A phase locked loop produces the 44.736 MHz transmit DS3 clock from the 32.768 MHz receive NCT clock. The 32.768 MHz clock is divided by 512 to produce a 64 kHz signal, and the 44.736 MHz output of the phase locked

loop is divided by 699 to produce a 64 kHz signal. These two 64 kHz signals are the inputs to the phase locked loop phase detector.

E. Starting Byte Table and Write Clock Generator

3.05 A 699 location look-up table is used to convert from the 106.402 microsecond M-frame to the 125 microsecond NCT frame. Each location contains the starting NCT frame byte number for its associated M-frame. Once per M-frame, under control of the dsync output of the muldem chip, the write counter and clock generator are written with the table entry addressed at that time. The table address is produced from the C bits received from the muldem chip over output AUXD.

F. Elastic Store

3.06 An elastic store is furnished to allow for differences of phase in the four different links. The elastic store is two frames in length to allow independent reading and writing regardless of phase. The frame slip buffer length adjustment moves the read address by one frame any time the write and read addresses get too close to the same address. This allows a slip without forcing the DLI out of frame. The read counter gets its clock and phase from the incoming NCT bit stream, while the write counter gets its clock and phase from the incoming DS3 bit stream via the muldem chip. A nibble from the muldem chip is converted to a byte and written to the elastic store. A byte is read from the elastic store and written in an 8-bit shift register, from which it is shifted out over the NCT link.

G. 8 KHz Reference Generator

3.07 The incoming DS3 recovered clock of 44.736 MHz is divided by 5592 to produce an 8 kHz reference square wave. This signal is sent to the associated link in the associated DLI where it is used as a reference to the DLI phase locked loop when that link is selected. The out-of-frame indication is also sent to the DLI. If the DS3 input goes out-of-frame, the DLI phase locked loop is forced to free run if it is locking to this link.

3.08 In the group of four links associated with a remote module, only one link is being used as a reference for the DLI phase locked loop. The 8 kHz generator associated with the reference link is allowed to free run while the generators associated with the other three links are synchronized to the 8 kHz sync derived from the incoming NCT bit stream. This forces all 8 kHz reference signals to be in phase so that a reference switch by the DLI does not introduce a large phase change. The MSTR, SELREF, and SELSENSE inputs defeat the synchronizing of the 8 kHz generator when a particular link is being used as the reference.

H. Loop-around Control

3.09 The loop-around control monitors the G bits of the incoming NCT bit stream, looking for the set loop-around and reset loop-around data patterns. The set loop-around data pattern is a string of 32 ones followed by a string of 32 zeros. The reset loop-around data pattern is a string of at least 64 ones. A timeout reset occurs 2 seconds after loop-around is set.

I. Idle Code Detector

3.10 The idle code detector looks for idle code on all time slots on an incoming NCT link and turns on the proper LED if this condition exists. When a link is taken out of service, the TMS sends idle code to all time slots on that link. The NDRC detects this condition and alerts the craft that it is all right to physically remove the pack.

J. DS3 Transmit and Receive

3.11 The DS3 bit stream coming from the DS3 interface circuit pack is a bipolar signal. A clock is recovered from this signal and then converted to two unipolar signals before sending it to the muldem chip. The DS3 muldem chip output consists of two unipolar data signals (M45N and M45P) and a clock (M45COUT). These signals produce a bipolar data signal that is sent to the DS3 interface pack.

3.12 In the transmit direction, the muldem chip takes the nibbles from the FIFO, the C bits and MSYNCIN from the C-bit generator, and the clock from the clock generator and adds the appropriate bits to produce the DS3 format output. In the receive direction, the muldem chip takes the two unipolar data signals and the clock and produces the nibble output along with clock, the C-bit output along with clock, the dsync output, and the out-of-frame indicator.

K. LED Indicators

3.13 Three LED indicators are provided on the faceplate of the NDRC circuit pack. These LEDs are used to indicate the following:

(a) The muldem chip cannot frame up on the incoming DS3 bit stream.

(b) The link chip cannot frame up on the incoming NCT bit stream.

(c) All time slots on the incoming NCT bit stream contain idle code.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Working limits for the individual circuit packs are in the respective circuit pack schematics (CPSs).

2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for the individual circuit packs are in the respective circuit pack schematics.

3. FUNCTIONS

3.01 Function information for the individual circuit packs are in the respective circuit pack schematics.

4. CONNECTING CIRCUITS

(a) DS3 Cross-Connect Circuit (DSX3) - SD-96621-01

(b) Time Multiplexed Switch Unit, Model 2 (TMSU2) - SD-5D061-01

(c) Module Controller and Time Slot Interchange Unit (MCTU) - SD-5D094-01

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