# *5ESS® SWITCHING EQUIPMENT TRANSMISSION RATE CONVERTER UNIT MODEL 2 CIRCUIT*

*Description of Changes*

The TRCU2 is being expanded to provide the capability to deliver SM2000 (5E9.2 release) functionality at an Optical Remote (ORM) location. This feature is known as EXM2000.

A minimum of one TRCU2 can be equipped for 1 EXM2000 in a remote office with 4 active NCT Links and 4 standby NCT links. A maximum of 6 TRCU2's can be equipped for 1 EXM2000 in a remote office with 24 active NCT Links and 24 standby NCT Links. With the additional NCT Links that are available in an EXM2000 configuration, the TRCU2 can now be fully equipped in a remote office.

Options "Y" and "Q" are required when a TRCU2 is to be equipped for an EXM2000 Application.

AT&T BELL LABORATORIES

DEPT NA5350300-WAM-FNG

# 5ESS® SWITCHING EQUIPMENT TRANSMISSION RATE CONVERTER UNIT MODEL 2 CIRCUIT

## CHANGES

### *B. Changes In Apparatus*

The 16E, 16F, 16G and 16K optical transmission packs manufactured at AT&T-MV Works are being manufactured discontinued (1/93). The 16E2 and 16F2 packs are being added to the J-Drawing (J5D003ED-2) stocklist and the SD-Drawing (SD5D086-02) as replacements (equivalents) for new orders. There will not be a direct replacement for the 16K pack that has the transmission span of 44.9 miles.

### *D. Description of Changes*

The 16E2 optical transmission pack will be used for 90Mbit/Sec optical transmission 0 to 25.1 miles (0-23.8 dB) applications. The 16E2 can be used as a direct replacement for the 16E pack (0 to 18 miles). In some applications the 16E2 pack can be used as a replacement for the 16F pack (0 to 28 miles) if the span does not exceed 25.1 miles (0-23.8 dB).

The 16F2 optical transmission pack will be used for 90 Mbit/Sec optical transmission 0 to 37.8 miles (0-28.9 dB) applications. The 16F2 can be used as a direct replacement for the 16F (0 to 28 miles) and 16G pack (10 to 36 miles). In some applications the 16F2 pack can be used as a replacement for the 16K pack (17 to 44.9 miles) if the span does not exceed 37.8 miles (0-28.9 dB).

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TABLE OF CONTENTS

## SECTION I - GENERAL DESCRIPTION

### 1. PURPOSE OF CIRCUIT

1.01 The Transmission Rate Converter Unit (TRCU) is a unit that was developed for the 5E3 generic. It provides the TMS and the SM with an interface to standard transmission equipment via the DS3 cross-connect. For this capability, a new version of the TRCU, called TRCU2, is being developed to allow direct connection to fiber optic cable, as well as to the DS3 cross-connect. At the host end of the links, the TRCU2 is mounted in a miscellaneous frame; at the remote end, it is mounted in the SM frame.

1.02 The TRCU2 contains NCT-to-DS3 Rate Converter (NDRC) circuit packs (TN1345), the network circuit packs (AKM3), and power for the NDRC circuit packs. The NDRC circuit pack provides the NCT-to-DS3 translation for the transmit half of the link, and the DS3-to-NCT translation for the receive half of the link. A total of four of these NDRC circuit packs is required to remote one SM, because each circuit pack supports one link. The network circuit pack provides equalization and attenuation of the DS3 bit stream between the NDRC circuit pack and the DS3 cross-connect. Each network circuit pack handles two links; so two packs are required to remote one SM.

1.03 For this capability, a new pack is being added to replace the network circuit pack when it is desirable to interface directly with a fiber optic link. This new pack (16E, 16F, 16G, or 16K), the Optical Line Interface (OLI), multiplexes two NDRC output bit streams together to produce a 90-Mb/s optical output. In the other direction, the OLI receives a 90-Mb/s optical input and demultiplexes it into two NDRC input bit streams. A fully equipped TRCU2 contains enough packs for remoting two SMs. The ORM is compatible with both CM1 and CM2. The SM that is used in the ORM must be provided with a TSIU3 that is equipped with circuit pack TN1077B.

### 2. GENERAL DESCRIPTION OF OPERATION

TMS-TO-TRCU2 INTERFACE

2.01 Four NCT links provide the connection between the TMS and the TRCU2. These NCT links are implemented with optical transmitters and receivers, and fiber optic cable just as the standard TMS-to-SM NCT links. The NDRC circuit pack has circuitry to detect the presence of three data patterns. One of these is idle code on all but one of the timeslots. This pattern is used to light an LED that indicates the link is idle.

2.02 The second pattern is a string of at least 33 ones followed by a string of at least 65 zeros on the G bit. This pattern is used to put the NDRC circuit pack into the loop mode. The third pattern is a string of at least 65 ones on the G bit. This pattern is used to reset the loop mode. In addition, the loop mode is reset automatically 2 seconds after it is set. The TMS, under diagnostic control, will send this special G-bit pattern to put the NDRC into the loop mode so that it can be diagnosed.

2.03 No power control and display function is provided for the power converters in the TRCU2 at the host end. The links are being monitored for errors by the TMS, and a loss of power will produce errors that will start the recovery process.

DLI-TO-TRCU2 INTERFACE

2.04 The four NCT links between the TRCU2 and the DLIs are implemented with a shielded twisted pair because the distance is very short (less than 2 feet). The loop mode control, mentioned above, is the same at this interface.

2.05 The NDRC circuit pack produces an 8-kHz reference signal by dividing down the incoming 45-MHz clock. This signal is sent to the DLI to be used as a reference for its phase-locked loop. Each of the four NDRC circuit packs provides an 8-kHz reference signal, with only one being selected by the two DLIs. In the NDRC circuit pack, those references not selected are synchronized to the reference that is selected.

2.06 Two leads from its associated DLI indicate to an NDRC circuit pack whether its reference has been selected as the phase-locked loop input. One of these leads indicates whether a particular DLI is master or slave, and the other indicates whether the A or B link is being used as a reference.

2.07 The NDRC circuit pack also produces an out-of-frame output. This output indicates whether the NDRC circuit pack can frame up on the incoming 45-Mb/s signal. This signal is sent to the DLI where it is used to force the phase-locked loop to free run if the 8-kHz signal to which it is locking is produced by a clock derived from a bit stream that the NDRC circuit pack cannot frame up on.

2.08 The power control and display function for the power converters in the TRCU2 is provided by the power control and display circuitry in the DLIs.

TRCU2-TO-DS3 CROSS-CONNECT INTERFACE (DS3 CONNECT OPTION)

2.09 The interconnection between the TRCU2 and the transmission equipment is done at the DS3 rate via the DSX-3 cross-connect. The DSX-3 connections are implemented with coaxial cable with one cable required for receive and one cable required for transmit for each DS3 channel. Each DS3 channel carries one NCT link worth of information. Because four NCT links are required to support an SM, four DS3 channels are used to support one ORM. These four links require that eight coaxial cables connect from the TRCU2 to the DS3 cross-connect.

TRCU2-TO-LGX INTERFACE (FIBER CONNECT OPTION)

2.10 The interconnection between the TRCU2 and the light guide cross-connect (LGX) equipment facility fiber optic cables is done at the 90-Mb/s rate via the LGX equipment. The LGX equipment allows the 90-Mb/s bit streams from the TRCU2 to be distributed, as desired, over the facility fiber optic cables. Each 90-Mb/s bit stream carries two NCT links of information. Because four NCT links are required to support one SM, two 90-Mb/s bit streams are used to support each SM. Four individual fibers are required to support these two links.

## SECTION II - DETAILED DESCRIPTION

### 1. POWER

1.01 Two power converters (494RA) are provided for each half of the TRCU2. One of these converters supplies the +5 voltage, and the other supplies the -5 voltage. At the host end, the power converters have no

associated control and display function. To turn a converter off, its latch must be released. At the remote end, the control and display function of the associated DLI also services the power converters in the TRCU2. Both the NDRC circuit pack and the network's circuit pack can be removed with the power on.

## 2. NETWORKS (DS3 CONNECT OPTION) AKM3 CIRCUIT PACK

2.01 This pack is used when it is desired to connect to the DSX-3. The distance between the TRCU2 and the DS3 cross-connect can vary from 0 to 450 feet. To accommodate this varying length, equalization and attenuation are provided in the TRCU2 by the network's circuit pack. Equalization is provided on the receive side, and a manually switchable pad is inserted on the transmit side for distances less than 225 feet.

## 3. OPTICAL LINE INTERFACE (FIBER CONNECT OPTION) 16E, F OR G CIRCUIT PACK

3.01 The OLI pack is used to connect directly to the facility fiber optic cables. In the lightwave transmitting direction, an 89.472-MHz clock is received from each of the associated NDRC packs. One of these clocks is selected for use by the OLI pack as the clock source. This clock is divided by two, and the resulting 44.736-MHz clock is sent to the NDRC packs. The 44.736-MHz clock is used by the NDRC packs to return synchronous data to the OLI. The OLI receives unipolar scrambled NRZ data and the 44.736-MHz clock from each NDRC pack.

3.02 These synchronized DS3 signals are combined to form the 89.472-MHz NRZ data signal. The DS3 signal from NDRC B is marked to allow the separator at the far end of the system to identify NDRC B's signal. The laser transmitter converts this electrical signal into pulses of light, which are coupled into a single mode fiber pigtail for connection to the transmitting single-mode or multi-mode fiber.

3.03 In the lightwave receiving direction, the receiving single-mode or multi-mode fiber is connected to a multi-mode fiber pigtail. The PIN-based lightwave receiver converts the pulses of light into electrical pulses. Clock is recovered from this 89.472-MHz unipolar NRZ data stream using a surface acoustic (SAW) filter. The signal is separated into two unipolar scrambled NRZ data and 44.736-MHz clock streams that are then sent to the appropriate NDRC packs.

3.04 The OLI pack was designed for the DDM-1000 Multiplexer. This pack comes in three different versions (16E, 16F, 16G, 16K) that result in span lengths from 8 to 37 miles, depending on the OLI version and the type of cable. Table A lists the parameters associated with 16E, 16F, and 16G, 16K. An option switch is provided on the OLI pack to adjust the output power of laser. This switch is set, based on the lightwave signal loss from the transmit plug to the receive plug (lightwave facility loss). Table B lists the switch points for the various combinations of transmitters and receivers.

## 4. NCT-TO-DS3 RATE CONVERTER

FORMAT

4.01 The superframe of the SYNTRAN format is used to convert the 125-microsecond/frame NCT format to the 106.402-microsecond/frame DS3 format.

Within the SYNTRAN 125-microsecond frame, bytes B1 to B682 are used to carry the NCT 16-bit timeslots, with every fourth byte being stuffed with arbitrary data. Bits C1 - C21 are used to pass the frame number of the next M-frame in the superframe. Bytes 683 - 691 are stuffed with arbitrary data.

NCT RECEIVE

4.02 The DLI link chip developed for TSIU3 is used to frame up on the incoming NCT bit stream. The incoming bits are converted to nibbles with a shift register and then sent to the link chip and the FIFO. The sync input to the link chip is produced from the write 8-kHz output using a shift register. This sync forces the internal buffer in the link chip to be one timeslot long. The nibble and 8-kHz sync outputs of the link chip are sent to the looparound control and the idle code detector.

FIFO

4.03 Because the nibbles received from the input shift register are asynchronous to the nibbles presented to the muldem chip, a 64x5 FIFO is used to provide a variable length buffer with reads independent of writes. This FIFO is written at an 8-MHz rate using the same clock that drives the link chip. This FIFO is read using an 11-MHz clock from the muldem chip. The read FIFO generator eliminates enough clock cycles from the 11-MHz clock to produce an effective clock of 8-MHz. In every 125-microsecond frame, a pattern of six clock pulses and two missing clock pulses is repeated 170 times followed by four clock pulses. Thus in a full frame, 1024 writes to the FIFO and 1024 reads from the FIFO are performed.

C-BIT GENERATOR

4.04 The C-bits in the DS3 format are used to pass the M-frame number over the link. A 10-bit counter that counts from 0 to 698 is used to supply the M-frame number. The MSYNC output from the muldem chip is used to increment the counter once per M-frame. The contents of the counter are loaded into a shift register using MSYNC; muldem output MCBCLK shifts the value into muldem input MCBD. Once per superframe, the 8-kHz sync from the FIFO is used to synchronize the C-bit counter and the internal muldem circuitry to the FIFO output.

90-MHZ CLOCK GENERATOR

4.05 A phase-locked loop is used to produce an 89.472-MHz clock from the 32.768-MHz receive NCT clock. The 32.768-MHz clock is divided by 512 to produce a 64-kHz signal, and the 89.472-MHz output of the voltage controlled oscillator is divided by 1398 to produce a 64-kHz signal. These two 64-kHz signals are the inputs to the phase-locked loop phase detector. The 89.472-MHz clock is divided by two and sent to the DS3 transmitter if the DSX-3 connect option is selected. The 89.472-MHz clock is sent to the OLI pack if the fiber connect option is selected.

STARTING BYTE TABLE AND WRITE CLOCK GENERATOR

4.06 A 699-location, look-up table is used to convert from the 106.402-microsecond M-frame to the 125-microsecond NCT frame. Each location contains the starting NCT frame byte number for its associated M-frame. Once per M-frame, under control of the dsync output of the muldem chip, the write counter and clock generator are written with the

table entry addressed at that time. The table address is produced from the C-bits received from the muldem chip over output AUXD.

ELASTIC STORE

4.07 An elastic store is provided to allow for differences of phase in the four different links. The elastic store is two frames long to allow independent reading and writing, regardless of phase. The frame slip buffer length adjustment moves the write address by one frame any time the write and read addresses get too close to the same address. This allows a slip without forcing the DLI out of frame. To prevent slips from occurring when the TSI switches sides from which it gets data, the buffer length adjustment circuitry tries to make the buffer plus facility delay equal on both sides. The delay on the two sides must be within 20 usec (2.5 miles) to guarantee this. The following rules are implemented in the buffer adjust algorithm.

1. If no collisions occur on self or mate keep buffer short.

2. If a collision problem occurs make the buffer one frame longer and send a signal to the mate to tell it to make its buffer long.

3. At both ends, look to the mate for the signal to go long only when the associated DLI is in the slave mode. One of the C-bits in the DS3 frame is used to pass the master/slave state of a particular DLI at the remote to its associated rate converter circuit packs in the host.

For the DSX-3 Connect case, the 2.5 mile route differential can be ignored if the odd links are sent on one route and the even links are sent on the other route. This allows the two alternate routes to have any lengths but if one route is lost half of the call capacity is also lost. For the Fiber Connect case, it is not physically possible with the present design to send odd links on one route and even links on the other route. When alternate routing is used send side 0 links on one route and side 1 links on the other route. To prevent slips, the routes must not differ in length by more than 2.5 miles. The read counter gets its clock and phase from the incoming NCT bit stream, while the write counter gets its clock and phase from the incoming DS3 bit stream via the muldem chip. A nibble from the muldem chip is converted to a byte and written to the elastic store. A byte is read from the elastic store and written in an 8-bit shift register from which it is shifted out over the NCT link.

8-KHZ REFERENCE GENERATOR

4.08 The incoming DS3 recovered clock of 44.736-MHz is divided by 5592 to produce an 8-kHz reference square wave. This signal is sent to the associated link in the associated DLI where it is used as a reference to the DLI phase-locked loop when that link is selected. The out-of-frame indication is also sent to the DLI. If the DS3 input goes out of frame, the DLI phase-locked loop will be forced to free run if it is locking to this link.

4.09 In the group of four links associated with a remote, only one link is being used as a reference for the DLI phase-locked loop. The 8-kHz generator associated with the reference link is allowed to free run while the generators associated with the other three links are synchronized

to the 8-kHz sync derived from the incoming NCT bit stream. This forces all 8-kHz reference signals to be in phase so that a reference switch by the DLI does not introduce a large phase change. The MSTR, SELREF, and SELSENSE inputs are used to defeat the synchronizing of the 8-kHz generator when a particular link is being used as the reference.

LOOPAROUND CONTROL

4.10 The looparound control monitors the G-bit of the incoming NCT bit stream looking for the set looparound and reset looparound data patterns. The set looparound data pattern is a string of at least 33 ones followed by a string of at least 65 zeros. The reset looparound data pattern is a string of at least 65 ones. A timeout reset occurs two seconds after looparound is set.

IDLE-CODE DETECTOR

4.11 The idle-code detector looks for idle code on all but one of the timeslots on an incoming NCT link and turns on the proper LED if this condition exists. When a link is taken out of service, the TMS or TSI sources idle code to all timeslots except the message timeslot on that link. The NDRC detects this condition, and alerts operating personnel that it is alright to physically remove the pack.

## 5. DS3 TRANSMIT AND RECEIVE

DSX-3 CONNECT OPTION

5.01 The DS3 bit stream coming from the network's circuit pack is a bipolar signal. A clock is recovered from this signal, and it is converted to two unipolar signals before sending it to the muldem chip. The DS3 muldem chip output consists of two unipolar data signals (M45N and M45P) and a clock (M45COUT). These signals are used to produce a bipolar data signal that is sent to the network's pack.

5.02 In the transmit direction, the muldem chip takes the nibbles from the FIFO; the C-bits and MSYNCIN from the C-bit generator; and the clock from the clock generator. It then adds the appropriate bits to produce the DS3 format output. In the receive direction, the muldem chip takes the two unipolar data signals and the clock and produces the nibble output along with clock, the C-bit output along with clock, the dsync output, and the out-of-frame indicator.

FIBER CONNECT OPTION

5.03 The DS3 bit stream coming from the OLI circuit pack is sent to muldem inputs D45P and D45N. The DS3 muldem chip output consists of two NRZ data signals (M45N and M45P) and a clock (M45COUT). One of these data signals, along with the clock, is passed on to the OLI pack. This selection is made with the scramble or unscramble lead.

5.04 In the transmit direction, the muldem chip takes the nibbles from the FIFO; the C-bits and MSYNCIN from the C-bit generator; and the 44.736-MHz transmit clock from the OLI pack. It then adds the appropriate bits to produce the DS3 format output. This output appears on M45P as a scrambled NRZ signal and on M45N as an unscrambled NRZ signal. In the receive direction, the muldem chip takes the scrambled NRZ data signal on D45P or the unscrambled NRZ data signal on D45N and the 44.736-MHz receive clock from the OLI pack and produces the nibble output along with clock, the C-bit output along with clock, the dsync output, and the out-of-frame indicator.

LED INDICATORS

5.05 Three LED indicators are provided in the faceplate of the circuit pack. These LEDs indicate the following:

(a) The muldem chip cannot frame up on the incoming DS3 bit stream.

(b) The link chip cannot frame up on the incoming NCT bit stream.

(c) All but one of the timeslots on the incoming NCT bit stream contain idle code.

## 6. ASSIGNMENT OF REQUIREMENTS

TRCU2 HARDWARE

6.01 TRCU2 hardware provides the following items:

(a) the bit rate and format conversion necessary to connect an NCT link to a DS3 link.

(b) the ability to transmit and receive electrical signals that conform to the DSX-3 cross-connect template.

(c) the ability to transmit and receive optical signals directly to and from single-mode or multi-mode fiber optic cable.

(d) looparound to give the diagnostic isolation capabilities.

(e) an LED that lights when all but one of the timeslots on the incoming NCT link have idle code.

# SECTION III - REFERENCE DATA

## 1. WORKING LIMITS

1.01 Working limits for the individual circuit packs are in the respective circuit pack schematics (CPSs).

## 2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for the individual circuit packs are in the respective circuit pack schematics.

## 3. FUNCTIONS

3.01 Function information for the individual circuit packs is in the respective circuit pack schematics.

## 4. CONNECTING CIRCUITS

(a) DS3 Cross-Connect Circuit (DSX3) SD-96621-01

(b) Time Multiplexed Switch Unit, Model 2 (TMSU2) SD-5D061-01

(c) Module Controller and Timeslot Interchange Unit (MCTU) SD-5D094-01

(d) Light Guide Cross-connect Equipment (LGX).

Table B

Switch Points for Various Combinations of Transmitters and Receivers

| OLI PACK TRANSMITTER SWITCH | | | |
|---|---|---|---|
| TRANSMITTER | RECEIVER | TRANSMITTER SWITCH | |
| | | LW | HI |
| | | FACILITY LOSS | |
| 16E OR 16F | 16E | 0 TO 9 dB | 9 TO 17.5 dB |
| 16E OR 16F | 16F OR 16G | 0 TO 11 dB | 11 TO 22 dB |
| 16G | 16E | 7 TO 15 dB | 15 TO 23.5 dB |
| 16G | 16F OR 16G | 7 TO 16 dB | 16 TO 28 dB |
| 16K | 16F,G,K | 13 TO 22 dB | 22 TO 34 dB |
| 16K | 16E | 13 to 21 dB | 21 to 29,5 dB |

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TABLE A

PARAMETERS ASSOCIATED WITH 16E, 16F AND 16G

| PARAMETER | | OLI | | | |
|---|---|---|---|---|---|
| | | 16E | 16F | 16G | 16K |
| WAVELENGTH | | 1305 ±30NM | 1305 ±20NM | 1305 ±20NM | 1305 (+-20NM |
| TYPE OF TRANSMITTER | | SINGLE MODE | SINGLE MODE | SINGLE MODE | SINGLE MODE |
| TRANSMITTER OUTPUT POWER-HI (1) | | -10 dBm | -10 dBm | -4 dBm | +2.0 dBm |
| TRANSMITTER OUTPUT POWER-LW (1) | | -16 dBm | -16 dBm | -10 dBm | -4.0 dBm |
| RECEIVER SENSITIVITY FOR BER-10E-9 | | -34 dBm | -38.5 dBm | -38.5 dBm | -38.5 dBm |
| AVAILABLE SYSTEM GAIN | | 24 dB | 28.5 dB | 34.5 dB | 40.5 dBm |
| EYE MARGIN | | 3.5 dB | 3.5 dB | 3.5 dB | 3.5 dB |
| EQUIPMENT MARGIN | | 3 dB | 3 dB | 3 dB | 3 dB |
| MAXIMUM FACILITY LOSS | | 17.5 dB | 22 dB | 28 dB | 34 dB |
| MINIMUM FACILITY LOSS | | 0 dB | 0 dB | 0 dB | 0 dB |
| CONNECTOR LOSS | | 1.5 dB | 1.5 dB | 1.5 dB | 1.5 dB |
| SINGLE MODE FIBER | OUTSIDE PLANT BUDGET (1305 +/-30NM) | 16 dB | 20.5 dB | 26.5 dB | 32.5 dB |
| | SPAN LENGTH (2) | 29 KM(18 MI) | 45.5 KM(29.3 MI) | 58.9 KM(36.6 MI) | 72.2 KM(44.8 MI) |
| MULTI-MODE FIBER | DISPERSION AND MODAL NOISE ALLOCATION (3) | 3 dB | 3 dB | 3 dB | 3 dB |
| | OUTSIDE PLANT BUDGET (1305 +/-30NM) | 13 dB | 17.5 dB | 23.5 dB | 29.5 dB |
| | SPAN LENGTH (4) | 13 KM(8 MI) (8 MI) | 17.5 KM(10.8 MI) (10.8 MI) | 23.5 KM(14.6 MI) (14.6 MI) | 29.5 KM(18.3 MI) (18.3 MI) |

(1) THE TRANSMITTER HAS A 6 DB SWITCH. POWER OUTPUT MAY BE SELECTED AS HI OR LW. SELECTION IS BASED ON THE INSTALLED CABLE LOSS.
(2) ASSUMES 0.55 DB/KM AVERAGE CABLE PLUS SPLICE LOSS (MEDIUM LOSS FIBER FOR THE 16E AND 0.45 DB/KM AVERAGE CABLE PLUS SPLICE LOSS (LOW LOSS FIBER) FOR THE 16F AND 16G.
(3) ASSUMES 90 MHz END-TO-END FIBER BANDWIDTH.
(4) ASSUMES 1.0 DB/KM AVERAGE CABLE PLUS SPLICE LOSS (MEDIUM LOSS FIBER).