CIRCUIT DESCRIPTION

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5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT CIRCUIT

B. Changes In Apparatus

Added UN395 and wiring options to the features and options table to provide the Packet Interface 2 (PI2) feature.

D. Description Of Change

Added information for the PI2 feature for the Module Controller and Time Slot Interchange Unit to provide a High Speed Packet Bus

Interface and allow the PI2 to interface with up to two Packet Switch Units (PSU/PSU2).

F. Changes In CS Sections

Paragraph 1.06:

All references to PI should read PI/PI2 and all references to PSU should read PSU/PSU2.

After paragraph 2.67, add the following paragraph:

2.68 Packet Interface Model 2 - UN395

The PI2 is essentially an enhanced version of the PI with improved performance and the ability to support multiple PSU/PSU2 complexes. The PSU2 is being developed for improved packets throughput for existing PSU features (ISDN), and for a feature for wireless referred to as Code Division Multiplexed Access (CDMA). The PI2 is architecturally the same as the PI and provides the basic PI function which is to buffer signaling and control packets between the PSU/PSU2 and the MCTU.

The Current PI supports one 10Mbps PSU complex. The PI2 can support up to two PSU complexes at a 10Mbps packet bus rate (PSU) or at a 100Mbps packet bus rate (PSU2).

The PI2 provides the buffering of signaling packets between the PSU complexes (PSU, PSU2) via the packet bus (PB) and from the MCTU via the SUIB. The PI2 is a 68040 based design. This design administers the communications of signaling packets to and from the PSUs via PBMAC devices and performs the sending and receiving of these packets to the MCTU via a 1Mbyte FIFO Dual port static RAM. Data is passed between the PI2 and the SMP via the Sub Unit Interface Bus (SUIB).

Add the following paragraph after paragraph 3.19:

Packet Switch Unit (PSU/PSU2) Interface

For the 10 Mbps packet bus interface, six differentially balanced signals are used:

a. Clear to send

b. Transmit/receive data

c. Request to send

d. Receive clock

e. Transmit clock

f. Carrier sense

The Packet Bus (PB) is a duplex bus connecting the PI/PI2 to the PSU or PSU2 complex. A PI only supports a 10Mbps PB opposed to the PI2 which supports both 10Mbps and 100 Mbps PBs. The following paragraphs describe the 10 Mbps and 100 Mbps packet bus interface.

For the 100 Mbps communication, the PSU provides the receive clock which is looped on the PI/PI2 back to the PSU (transmit clock). If the PI/PI2 is transmitting a signaling packet to the PSU, the PI/PI2 will issue a request to send. The PSU responds by sending carrier sense and clear to send and then the PI/PI2 transmits the signaling packet. If the PSU is transmitting signaling packets to the PI/PI2, the PSU sends carrier sense and the data are sent to the PI/PI2.

For the 100 Mbps interface, eight differentially balanced signals are used:

a. Clear to send

b. Two - Transmit data

c. Two - Receive data

d. Request to send

e. Receive clock

f. Transmit clock

For 100Mbps (PSU2 only) communication, the PSU2 provides the receive clock which is the PSU2 transmit clock. If the PI2 is transmitting a signaling packet to the PSU2, the PI2 will issue a request to send. The PSU2 responds by sending clear to send and the PI2 transmits the signaling packet. If the PSU2 is transmitting signaling packets to the PI2, the PSU sends receive data to the PI2.

Change the first sentence in paragraph 3.23 to read as follows:

The SMP subunit interface bus is used as the control interface to the TSI, SP, CI, and the PI/PI2 from the SMP.

Replace paragraph 3.53 with the following paragraph:

For units equipped with a TN1042 (PI) those element identifiers are:

IT, IS for side 1; and IV, IU for side 0.

For units equipped with a UN395 (PI2) those element identifiers are:

JM, JN, JO, JP for side 1 when configured as 100Mbps packet busses.

JI, JJ, JK, JL for side 0 when configured as 100Mbps packet busses.

JS, JT, JU, JV for side 1 when configured as 10Mbps packet busses.

JQ, JR, JW, JX for side 0 when configured as 10Mbps packet busses.

Add the following items to the table in paragraph 3.56:

TN1042	2	PI
TN1042B	2	PI
UN395	2	PI2

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B. Changes In Apparatus

Added the TN1407, TN1408, and wiring options to the features and options table to provide the SMP23 feature.

D. Description of Change

Added information for the SMP23 feature for the Module Controller and Time Slot Interchange Unit, and to increase the memory of the SMP unit from 16Mbytes to 32Mbytes, using the Memory Expansion Unit. (MEU).

F. Changes In CD Sections

After paragraph 2.17, add the following paragraph:

TN1407 - PROCESSOR CORE BOARD

Processor Core Board (TN1407) is used for the SMP23 option, uses the MC68020 microprocessor, and runs at 10MHz (system clock). It provides 128Kbytes of text cache, directly mapped, and 512Kbytes of static RAM, overlaying user stack memory.

After paragraph 2.23, add the following paragraph:

TN1408 - MEMORY CONTROLLER BOARD

The Memory Controller Board (TN1408) provides all the functions of the TN1527, but provides the memory interface between the TN56 and TN2012 memory packs and the TN1407 core board in the SMP23 option. This pack also provides a feature in International for Split Memory with additional wiring changes. The Split Memory feature allows the use of a TN1409 (8Mbyte board) to increase the SMP unit to 32 Mbytes without the memory expansion unit.

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B. Changes in Apparatus

B.1 Added option "YB" to provide microcode MC5X281A1B (TN874B) for the "5EE3(2) generic.

D. Description of Change

D.1 Microcode MC5X281A1B has been assigned to the (TN874B) for the 5EE3(2) Generic.

F. Changes in CD Sections

F.1 None.

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TABLE OF CONTENTS PAGE

TABLE OF CONTENTS PAGE

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This document describes the module controller and time slot interchange unit (MCTU). The MCTU has been developed to reduce costs, and this is the sole reason for its introduction. Cost reduction is achieved by increasing the level of hardware integration using very large scale integration (VLSI) technology.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 5ESS Switch is a digital time division switch with a time-space-time architecture. The time multiplexed switch (TMS) provides the central space division switching function and connects to various switching modules (SMs) that perform the time division switching function and interface to the transmission facilities.

2.02 An SM contains the following:

1. A switching module processor (SMP) to provide the intelligence for the SM.
2. A time slot interchanger (TSI) to perform the time division switch and related functions.
3. A dual link interface (DLI) to provide the interface between the TMS and SMs via optical fibers called network control and timing (NCT) links.
4. Various peripheral units[1].

2.03 The TSI, SMP and DLI are common to all SMs, and the peripheral units are equipped, as needed.

The MCTU is a two-shelf unit containing the SMP, TSI, and DLI circuitry. The MCTU provides the following:

1. An SMP to provide the operating environment for the software and interfaces to the TSI subunits.
2. A fast pump capability used for initialization of the SMP memory.
3. A time division switch under control of the SMP.
4. Preprocessing on the signaling and control bits of the time slot data and by the SMP.
5. An interface to the NCT links.
6. An interface to the peripheral units for control information from the SMP.
7. An interface to the peripheral units for processor control module (PCM) data.

2.04 The MCTU is a duplicated unit. The mate (nonactive) side is updated by the active SMP to provide the ability to switch from side to side. Under no-fault conditions, this switch to the mate side is accomplished without introducing errors. Error-checking circuitry and diagnostic aids are used extensively to facilitate maintenance of the MCTU.

SECTION II - DETAILED DESCRIPTION

1. PHYSICAL LAYOUT

1.01 The MCTU has seven subfunctions: the time slot interchanger (TSI), the signal processor (SP), the dual link interface (DLI), the data interface (DI), the control interface (CI), the switching module processor (SMP), and the bootstrapper (BTSR).

1.02 The TSI is the time division switch; it contains two 512 x 512 time slot interchangers, one for data from the TMS to the peripheral units

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1. Digital service unit, metallic service unit, digital line and trunk unit, line unit, trunk unit, etc.

and one for data from the peripheral units to the TMS. The two 512 x 512 switches are connected such that time slots may be looped, thereby providing the capability to connect peripheral time slots (for intramodule calls). The TSI also provides a data port to the local digital service unit (DSU).

1.03 The SP does the hit timing and processing on the signaling and control bits (A-G) from peripheral time slots. It provides the SMP access to these bits and provides a first-in/first-out (FIFO) type queue to report state changes of these bits. It also allows the SMP to source these bits to the peripheral units.

1.04 The DLI, which is the interface to the NCT links, contains the transmit and receive circuitry needed to interface to the optic links. It recovers timing information from these links to provide timing for the MCTU. It also provides the SMP an interface to the message time slot (MTS) on each NCT link. Because the DLI is in the same failure group as the TMS, cross-coupling is necessary for all connections between the DLIs and the duplex MCTU. The DLI selects one of the two NCT links connected to it or to the mate DLI as a reference timing source; the TSI selects one of the two DLIs as a clock source. The TSI then distributes this clock to the rest of the MCTU.

1.05 The DI provides the data interface to peripheral units. It reformats time slot information and does a 2:1 concentration on peripheral time slots. Two DIs are connected to the TSI, each providing the TSI with 256 time slots per frame. Each DI provides 16 peripheral interface data buses (PIDBs) for connection to peripheral units.

1.06 The PI is a subunit of the SMP and a design unit of the packet switch unit (PSU). The PSU implements integrated services digital network (ISDN) capabilities on the 5ESS Switch. The main function of the PI is to buffer signaling packets between the protocol handlers (PHs) via the packet bus (PB) and the SMP via the subunit interface bus. Resident on the PI is circuitry that interfaces to the SUIB and a port processor (PP), which transmits and receives packets between the SMP and PHs. The PP design is common to the PI and PH. The signaling packets are first first-in/first-out (FIFO) buffered in a 1 Mbyte dual port memory of the PP circuitry. The PP controls Port A of the dual port memory and transfers the signaling packets across the PB. Port B of the dual port memory transfers signaling packets to/from the SMP over the SUIB.

1.07 The CI provides the interface between the SMP and the various peripheral units for control information. Each CI provides 23 PICBs for these connections. The MCTU may be equipped with two CIs (per side) to provide a total of 46 peripheral interface control buses (PICBs).

1.08 The SMP may operate in the active, standby, or out of service (OOS) mode. In the active state the SMP performs call processing, executes code, and controls the DLIs and interface units. In the standby state the SMP does not execute code but allows the active processor access to its internal buses. In the OOS state the SMP is able to execute code but cannot access the DLIs. The normal operating mode of the SMP is with one processor active and the other processor standby. "Active" means having the "A" flip-flop set and executing code. Circuitry is provided to ensure that neither a standby nor OOS processor can access a DLI. Under normal (no faults) operating conditions, the active processor keeps all data areas in the standby controller up to date, such that the standby processor may at any time, be made active. Should a fault occur in the active processor, the standby processor will be made active, and the active processor OOS.

1.09 The BTSR provides the interface between the fast pump data link and the SMP. The BTSR receives serial data from a dedicated peripheral interface data bus and performs data transfers into the SMP memory for purposes of initialization.

2. FUNCTIONS

SWITCHING MODULE PROCESSOR - FS 1, 2, 3, 4

2.01 The SMP function in the MCTU is realized using six circuit packs codes (TN871/TN871B, TN872/TN1617, TN873, TN874/TN874B, TN875B/TN875C, TN56). The SMP dynamic memory system uses up to five TN56 memory planes, each of which is 2 Mbytes. This allows a maximum of 10 Mbytes of dynamic random access memory (RAM) to be equipped.

2.02 A generic 5E4(2) feature, officially known as the MCTU-EMA (module controller time slot interchange unit - extended memory access), introduces the MC68012 processor in place of the MC68000 SM processor to provide memory beyond the 16 Mbytes limit. This feature requires the switch module processor (SMP) to be equipped with three new circuit packs (the TN1397, TN1527 and TN1533) that replace the TN871B, TN875C and TN873, respectively. With generic 5E4(2) the SMP dynamic memory system can use up to seven TN56 memory planes, each of which is 2 Mbytes. This allows a maximum of 14 Mbytes of dynamic RAM to be equipped.

2.03 This feature also allows the SMP dynamic memory system to use up to three TN2012 memory planes, each of which is 4 Mbytes; this allows a maximum of 12 Mbytes of dynamic RAM to be equipped.

2.04 In generic 5E4(2), the MCTU and memory expansion unit (MEU) can expand the switch module processor's memory from its current size of 16 Mbytes with the use of TN56s, and from 20 Mbytes to 32 Mbytes with the use of TN2012s.

2.05 The normal operating mode of the SMP is active/standby. In this mode one of the processors, actively executing code, is said to be in the "running" state. In addition, the processor is called "active" if its "A" flip-flop is set. The other processor is in the standby "dormant" mode. While dormant, the internal buses of the SMP can be controlled by the mate[2] allowing it read and write access to the dormant processor. Whenever a processor becomes dormant, it releases control of its internal buses to its mate. This operating mode allows the running processor to keep an up-to-date copy of its memory in the dormant processor.

The SMP can operate in the following hardware states:

1. The processor is actively controlling its internal buses. While running, the mate is unable to gain access to the active processor's buses.
2. When dormant, the processor is in a direct memory access (DMA) hold condition, granting the mate access to all the internal buses.

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2. Mate refers to the other processor in the SMP.

3. The DMA transfer mode allows the DMA unit to transfer data bytes to/from the message time slot links. The DMA unit controls the internal buses. If the update mode is enabled, the data writes also occur in the mate.

2.06 Active and standby are software states, distinct from the hardware states. An active processor must be running and have access to the DLIs. A standby processor is dormant with its mate active and keeping its memory up to date.

2.07 Three types of memory are provided in the SMP: 128K erasable programmable read-only memory (EPROM), 8K of static RAM, and a maximum of 10,096K of dynamic RAM used for the operational programs and data. The EPROM provides program storage for power-up initialization and fault recovery. The static RAM provides data storage, independent of the dynamic RAM. This is an important feature when exercising the dynamic memory system. There is 8K of address space reserved for I/O access via memory reference instructions.

2.08 The dynamic memory system uses TN56 memory planes, each of which is 2048K bytes. Detection and correction of single-bit memory errors and detection of double-bit errors are provided by hamming parity across all of memory. Memory word size is 40 bits, which includes 4 bytes of data, parity over each byte, and 4 bits of hamming. The mapping to the processor's 16-bit word size is accomplished on the memory controller pack.

2.09 A write-protection capability is provided on the SMP memory. Each 1K byte of data memory is protectable. Each 4K block of text memory also is protectable. All text can be protected with a single bit. Any attempt by software to write into a write-protected area results in a reset (nonmaskable interrupt) being applied to the SMP, and the write being blocked. The selection of whether a particular 1K byte data block or a 4K byte text block of memory is write-protected is made under software control. Additionally, a mechanism for implementing stack protection is available. When activated, the memory region from 0x80000 to 0x100000 becomes write-protected, except for a 2K block assigned to the currently running process. Stacks are available in 2K-bytes only, allowing a total of 256 separate stacks.

2.10 To allow efficient control of and response to asynchronous events, 25 interrupts are provided per side in the SMP. Twenty-four of the interrupts are presented to the SMP as level-4 interrupts. Errors from the subunits, error reporting, and message completion from the data link controllers, time intervals, status changes, and errors are all presented to the processor as interrupts. Two types of level-4 interrupts are provided: A high-priority set for reporting errors from the subunits, and a low-priority set for all other interrupts (disabled during the I/O time interval). The twenty-fifth interrupt arrives at the SMP as a level-5 (higher priority) interrupt. This interrupt is generated by the central processor intervention (CPI) circuitry and is used to indicate a TMS switch.

2.11 Each processor possesses a sanity timer, reset under software control. Failure to reset the timer, or resetting the timer too often causes a reset (nonmaskable interrupt) to be applied to the SMP. The active processor resets the timer in the standby processor. A timeout of the sanity timer in the standby processor results in the standby processor leaving the standby state and, under software control, entering the out-of-service (OOS) or inactive state. The minimum interval requirement is disabled in the off-line side.

2.12 The SMP receives two message time slots from each DLI. The SMP can select any of two of these time slots for message communication with the message switch (MSGS). Messages over these message time slots adhere to the BX.25 communication protocol. All communication with the central processor (CP) is all under DMA control in the SMP.

2.13 A central processor intervention (CPI) path to each processor can be used as a hardwired path to force an SM into a known state from the CP. The SMP has a minimum of control over the path of the CPI message and no control over the designated action taking place. The seven possible CPI actions are:

1. Force side 0 of the SMP active; also forces side 1 inactive.

2. Force side 1 of the SMP active; also forces side 0 inactive.

3. Clear the force active set by one of the above CPI functions.

4. Force a reset to the processor(s).

5. Disable the sanity timers in both processors.

6. Enable the sanity timers in both processors.

7. Level-5 interrupt to SMP indicating a TMS switch.

2.14 A mate power fail (MPF) detection capability is provided to prevent the active processor from mutilating the mate's memory when the active processor sustains a power failure. The circuitry prevents a processor that has lost power from writing the mate and forces the mate active.

2.15 A 32-bit counter is used for a stable billing clock. Either DLI 0 or DLI 1 can drive the 32-bit counter, with an enable bit provided for each DLI clock. A software strobe point, used for diagnostics, can advance the counter at a software rate if the two clocks are disabled.

A. TN871 - Processor Core Board

2.16 The TN871/TN871B board provides the following functions for the module processor (MP):

1. A Motorola 68000 microprocessor with associated clock generator, local bus controller, status generator, ready logic, and interrupt interface. The microprocessor utilizes a 9 MHz clock. The TN871B can switch to a 10 MHz clock, and, when used in conjunction with the TN875C Memory Controller, will provide processor speed-up capabilities. Wait states are required for all bus cycles. Other boards in the SMP may request the additional wait states required for refreshing dynamic RAM, I/O operations, and for certain sequences of dynamic RAM cycles. During refreshing, which requires 5-6% of the available memory bandwidth, reads of dynamic memory by the microprocessor are delayed until after the refresh operation has completed.

2. Bus control for the three major bidirectional buses, i.e., system data bus, microprocessor data bus, and update address and data bus.

3. Parity generation and checking for the three major buses.

Parity checking is performed on read data.

4. Wait logic to generate appropriate wait states for EPROM, static RAM, I/O, update, and memory operations.

5. Direct memory access (DMA) and dormant request logic to time properly requests and grants for bus cycles. A timing circuit to detect invalid or prolonged DMA states.

6. Diagnostic latches that record address and data on system bus during a nonmaskable interrupt (NMI).

7. The special function register that allows the forcing of address and parity errors, the source for hamming write inhibit signal, the force text bit that will force a data access into the text memory space, and the control bits for accessing and modifying the write-protect map.

8. Ready timer circuitry. The ready timer will generate an NMI if the processor wait line is not released after 56 μsec.

9. Interface to the non-interfering match and trace set (NMAT).

B. TN1397 - Processor Core Board

2.17 TN1397 is another version of the TN871C circuit pack. The only difference between these boards is the use of micro-processor chip. The TN1397 is using the MC68012 and the TN871C is using the MC68000.

C. TN873 - Processor Support Board

2.18 The TN873 contains the following:

1. Address decoding to enable EPROM, static RAM, I/O, and dynamic RAM.

2. Address parity checking for system address bus, SA1-SA23.

3. Subunit interface, including subunit data, address, read and write and not ready leads. It also contains the subunit board select checker.

4. Bus control register, that enables DMA activity, update, and entering standby state.

5. Sanity timer, I/O timer and ready timer circuits. The sanity timer has a safe window from 233 to 699 msec where it may be reset. The I/O timer must be enabled to perform most I/O operations. There are 114 μsec allowed for I/O cycles before the timer generates an NMI.

6. Hardware and software error source registers and abort logic for bad address parity, and main reset source register and its masking.

7. Processor status registers 1 and 2, reflecting the status of the reset counter, and operations on the system bus before an NMI.

8. The I/O data bus interface and the parity generation and checking on the I/O data bus. The translation from 16 bits to 8 bits, necessary for the LSI 8-bit peripherals, is made here.

D. TN1533 - Processor Support Board

2.19 TN1533 is another version of the TN873 circuit pack to use in generic 5E4(2).

E. TN872/TN1617 - Communications Board

2.20 The TN872/TN1617 has the following functions:

1. The DMA unit and support logic. The DMA unit provides four independent channels, each with separate byte count and address registers. Each channel can transfer up to 64K bytes of data in one block starting anywhere within a 64K address space. DMA transfers may be accomplished only within the memory data space. No DMA transfer is allowed in text space.

2. Two synchronous data link controllers (SDLCs) for handling the message links, use the BX.25 protocol, between the DLI and SMP. Circuitry is provided to connect either SDLC device to either of the serial links. Parity is generated and checked on each of the SDLC data links. The SDLC devices have receive and transmit interrupts to simplify normal (or abnormal) message completion.

3. "A" flip-flop circuitry used to determine which processor has access to either DLI. When both processors are running, only one may have its A flip-flop set. A processor cannot set its A flip-flop if the A flip-flop of the mate is set and the mate is running. An NMI clears the A flip-flop. The active processor can set the A flip-flop on a dormant mate.

4. Circuitry to provide three clocks for software timing. Normally one is programmed for a 10 msec interrupt, one for miscellaneous functions, and the third counts the number of 10 msec interrupts (or whatever the first counter is programmed).

5. Circuitry for controlling the SMPs' 25 interrupts. The interrupt from the CPI gate array is given the highest priority. Error interrupts from the DLIs, the subunits, and those resulting from mate processor errors are given the next highest priority, allowing them to interrupt the processor during the I/O timer interval. All other interrupts must wait for the I/O timer interval to complete. Buffers are provided to allow the processor to read directly the interrupt request lines from the DLIs and subunits.

6. Billing counter and associated circuitry.

7. Interface circuitry to the DLI control, status, and error source registers (ESRs).

F. TN874/TN874B - RAM/ROM Board

2.21 The TN874B is required for speed-up and EMA. The TN874/TN874B board has the following:

1. 128K of EPROM. Parity is used over both address and data to ensure correct data addressing.

2. 8K of static RAM. Parity is generated and checked over address and data.

3. Write data parity checking for the 16-bit system data bus. Writes to memory are aborted if bad parity is detected on the

data bus, and an NMI applied to the processor.

4. The write-protect circuitry for all the address space provided, the data space, including EPROM, static RAM, and I/O, and text space. Writes to static or dynamic memory are aborted if the write-protect bit was set for that block. Writes to EPROM can be detected by setting the write-protect bit in the write-protect control register. The I/O space also has write-protect bits associated with it. Writes are not aborted to the I/O space if a write-protect bit is set, but a write-protect error is generated.

5. Control for the alarm control/display packs that sense and control various points within the IM. Scans for request out of service (OOS), and craft lights for request in progress, OOS, and diagnostic control are here.

6. The CPI gate array and associated circuitry.

7. Stack protect and associated circuitry. When activated, the memory region from 0x80000 to 0x100000 becomes write-protected, except for a 2K block assigned to the currently running process. Stacks are available in 2K bytes only, allowing a total of 256 separate stacks.

G. TN875B/TN875C - Memory Controller Board

2.22 The TN875B/TN875C acts as the interface between the processor and the dynamic memory. When used in conjunction with the TN871B, the TN875C will provide processor speed-up. The TN875B/TN875C provides the following:

1. Supports 8- and 16-bit read and write operations with a 32-bit word.

2. Automatically performs the read-modify-write cycle required to maintain the check bits for all write operations.

3. Performs an automatic rewrite of corrected data into memory when a correctable error is detected.

4. Provides pipelining of write operations so that the processor is not unduly delayed while the read-modify-write operation is in progress.

5. Provides address decoding to select individual memory circuit packs.

6. Checks that the memory circuit packs are properly selected and receive correct address information on each access.

7. Blocks write operations if incorrect data parity is received, if a memory address check fails, or if the write-protect circuit indicates that the write should not be allowed.

8. Refreshes circuitry. An entire row (address bits 2 - 10) on all memory boards is refreshed simultaneously. A refresh operation occurs approximately every 8 μsec. A 64-μsec timer is reset after each refresh operation; a timeout will cause an NMI to be applied to the processor.

9. Text/Data selection. When in the separate instruction/data mode, A24 serves as the text/data distinguisher. When A24 is a "0", data space is under interrogation. When A24 equals "1", text space is being accessed. When not in SID mode, A24 is ignored.

10. The hamming gate arrays used for error detection/correction. These gate arrays generate a modified hamming code over 32 bits (8 bits of parity generated) to give double-bit error detection and single-bit detection/correction.

H. TN1527 - Memory Controller Board

2.23 The TN1527 is another version of the TN875C that acts as the interface between the processor and the dynamic memory. When used in conjunction with the TN1396, the TN1527 will provide processor speed-up.

I. TN56 Memory Board

2.24 The TN56 is a 2 Mbyte dynamic RAM memory board. Data is organized into 4-byte words with an additional 8 bits of hamming and parity associated with each word.

J. TN2012 Memory Board

2.25 The TN2012 is a 4 Mbyte dynamic RAM memory board.

CONTROLLER POWER - FS 5, 6

2.26 The Controller Power Circuit is a three circuit pack function, consisting of one SN516 Control and Display pack, and two 410AA power converters.

A. 410AA Power Converters

2.27 The purpose of these converters is to provide a means of converting nominal -48 volt input to a well regulated and isolated +5 volt output for applications in the MCTU circuitry. The bottom and top shelves are each equipped with one 414AA which provides +5 volts at 300 watts.

B. SN516 Control and Display Pack

2.28 The SN516 control and display pack provides the following functions for the MCTU:

1. The human interface allows an operator to power on, power off, request a unit either in service or out of service, and manually override momentarily.

2. Alarm display, allows the operator to read the status of the power circuits by observing an LED display that indicates the following:

   a. OFF - A red LED, when lit, indicates that power is off.

   b. ALM - A red LED, when lit, indicates a power fault on the unit fuse or converter alarms. Note: in the alarm state, all power may not be off in the unit. After an operator powers down the unit for repairs, the OFF LED will light, and the ALM LED will extinguish.

   c. OOS - A yellow LED controlled by the system and is lit whenever the unit is out of service.

d. RQIP - A green LED, controlled by the system, lights whenever a request to restore or remove a unit has been received by the system. If this request is denied, the LED will flash for 5 to 10 seconds.

e. ROS - A green LED lights whenever the ROS/RST switch is in the request out of service position.

3. Converter control interface, allows the human interface and software interface to control the power converter or converters.

4. Software Interface, all 5ESS units will require some interface between their power and the system software. This interface is in the form of scan points to report alarms and signal distributor points to light status LEDs (out-of-service, request-in-progress).

BOOTSTRAPPER - FS 7

2.29 The BTSR function in the MCTU is realized by using a single circuit pack (TN878). The BTSR receives serial data from a dedicated peripheral interface data bus (PIDB) and performs data transfers into the SMP memory. Six bits per PIDB time slot are used for transferring pump data. With 32 PIDB time slots per frame, data is downloaded into the SMP memory at a rate of 192 Kbytes/second. Any subset of the 32 PIDB time slots may also be used for a pump, with the "E" bit of a time slot distinguishing used/unused time slots.

2.30 The BTSR receives pump data in the form of 2-Kbyte blocks. Each block of data is preceded immediately by a 16-byte header containing start code, block size, starting address and hashsum check (on the header) for that block.

2.31 The BTSR is a simplex entity that interfaces to the SMP update bus, thereby gaining access to either processor. During the transfer of a block of data, the BTSR places the processor(s) being pumped into total DMA hold and performs 16-bit word DMA transfers into the processor(s) memory. For the duration of the block the BTSR also assumes maintenance of the SMP sanity timer(s). Between blocks of data, the active processor is allowed to run.

2.32 The BTSR also provides a resident diagnostic to facilitate the early detection of hardware failures when in the non-pump state.

A. TN878 - Bootstrapper Board

2.33 The TN878 circuit pack contains the following:

1. Data assembler circuitry. Distinguishes between active/idle PIDB time slots, strips off the 6 valid data bits from active PIDB time slots and reassembles them into 16-bit words. This circuitry also checks parity for a PIDB time slot and returns the same parity for that time slot on the next frame.

2. An Intel 8748 Microcomputer. Used for BTSR initialization, data block header processing, SMP sanity timer maintenance, and execution of resident diagnostic.

3. An Advanced Micro Devices 9517 DMA Controller. Used for transfer of pump data.

4. Address latches for generating the 24 bits of address required.

5. Control register for software configuration of BTSR. This includes PIDB selection, processor selection, and diagnostic selections.

6. Parity checking/generation circuitry. Three bits of parity are generated over address, and 2 bits of parity over data.

7. Test RAM and associated circuitry. Used for diagnostic purposes. "Simulated" time slots can be sourced from the test RAM and switched in at the data assembler. Test blocks of data can be loaded into the Test RAM and pumped into the SMP memory.

8. Update bus interface circuitry.

DUAL LINK INTERFACE - FS 8, 9, 10, 11

2.34 The dual link interface has been redesigned for the MCTU. It is functionally the same as the DLI in the 5E2.1 version of the TSI, but it has been reduced to one circuit pack (TN1077) by incorporating an onboard power converter and the related circuitry to control that converter.

2.35 The DLI provides the interface to the NCT links for the MCTU. The DLI recovers clock and data from the incoming NCT links and distributes the resultant clocks and data to the MCTU. In the opposite direction, the DLI receives outgoing data from the MCTU. The outgoing data is then multiplexed and sourced to outgoing NCT links. In each SM, two DLIs operate in a master/slave (active/standby) configuration.

2.36 The DLI consists of two link interface (LI) circuits: a clock circuit, and a control circuit. Each LI interfaces with one pair of NCT links (outgoing and incoming) that provides 256 time slots to and from the SM. Of these 256 time slots, 255 are for voice and data paths to and from the MCTU, and the remaining time slot is reserved for communications between the administrative module and the SMP (this time slot is referred to as the message time slot). The incoming 32.768 megabit/second data stream from the NCT link enters the receive (RCV) circuitry in the LI where it passes through a clock recovery circuit that derives a 32.768-MHz clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the phase lock loop (PLL) in the clock circuit. The RCV circuit "frames up" on the incoming data stream via a pseudo-random sequence inserted into the data stream at the source end of the NCT link (the TMS in a multimodule office and the MICU in a single-module office). The incoming data stream is then converted to time slots and written into the BUFFER circuit (a RAM capable of containing one frame of data).

2.37 The TSI interface and message interface operate from clocks derived from the output of the PLL. When time slots are read from the BUFFER, parity is checked and regenerated. Normal voice and data time slots are sent to the duplex TSIs via nibble buses operating at 8.192 megabits/second. The message time slot is sent to both the active and standby sides of the SMP via serial data links to the synchronous data link controller (SDLC). These data links operate at 48 kilobits/sec. The message time slot select switches (955B) provide the capability to select one of 256 time slots as the message time slot for NCT links A or B. When the MCTU is in a remote switching module (RSM) environment, these switches are removed and the message time slot is selected by the SMP. However, in a minimally equipped RSM (two or three T1 lines), the switches are not removed, but the message time slots are forced to zero and one.

2.38 In the return direction, data is selected from one of the TSIs at the TSI interface and from one side of the SMP at the message interface for transmission to the TMS via the outgoing NCT link. These time slots are then multiplexed to provide a full frame of 256 time slots. In the transmit (XMIT) circuit, parity is checked and regenerated. The pseudo-random framing sequence that is generated in the control circuit is inserted (one framing bit per-time-slot). Finally, the time slots are converted to a 32.768-MHz data stream and transmitted over the outgoing NCT link.

2.39 The clock circuit selects a clock reference from one of the two LIs (master mode) or from the mate DLI (slave mode). This selected clock is used as a reference for the PLL which, in turn, provides a reference voltage to the voltage controlled crystal oscillator (VCXO). The output of the VCXO is a 32.768-MHz clock that is divided by the clock circuit and distributed to the remainder of the DLI, the mate DLI, the TSI, and the SMP.

2.40 The control circuit provides control for the various functions performed by the LIs and clock circuit. Errors from these circuits are latched into error source registers (ESRs) that reside in the control circuit. These control registers and ESRs are accessible for writing and reading by either side of the SMP via the SMP-DLI control interface. This interface is a 1.875-MHz serial data link. The data bits that make up the commands are clocked in by the SMP, and the command is executed on the reception of a "go" signal received over a separate lead from the SMP. Parity over address and parity over data are checked in the control circuit. The control circuit provides a serial data link back to both sides of the SMP for read operations and an interrupt lead back to both sides of the SMP to indicate that an error condition exists. Each bit of the ESR can be inhibited from causing an interrupt via ESR mask registers.

2.41 The control circuit is contained in a custom NMOS device (327P). The clock circuit is implemented in SSI/MSI devices, along with the PLL and VCXO daughter boards. The circuitry that composes the RCV circuit and the portions of the TSI interface and message interface that send data to the TSI and SMP, is implemented in an LS1500 functional logic array (FLA), coded 374F. The XMIT circuits for both LIs and their corresponding portions of the TSI interface and message interface are implemented in one LS1500 FLA (374B). The DLI is contained on a single TN circuit pack (TN1077). Each DLI is in a failure group separate from the rest of the SM and is powered by an onboard power converter (984A). The power converter will interface to the SN516 control and display functions that are integrated onto the TN1077. In an RSM environment, the DLI will also include the facilities interface unit (FIU) in its service group.

TIME SLOT INTERCHANGER/SIGNAL PROCESSOR - FS 12, 13

2.42 The time slot interchanger in the MCTU consists of one circuit pack (TN1086) per side that incorporates both the TSI and SP functions. An overview of the TSI/SP operation is presented here.

2.43 The primary data path delivers 512 peripheral time slots from the DIs to the receive TSI RAM to be stored in consecutive order. Time slots are then translated from the Receive RAM and can be delivered to both DLIs on any of the 512 network time slots. In the opposite direction 512 network time slots from the DLIs are written consecutively into the transmit TSI RAM. Time slots are then translated from the transmit RAM on chosen peripheral time slots as instructed under software control and delivered to the DIs. Any peripheral time slot written into the receive TSI RAM can be read out onto multiple (up to all) network time slots toward the DLIs. The same fanout capability is provided by the transmit TSI RAM. A maximum delay in each direction of one frame (125 μsec) can be introduced by the time slot interchange.

2.44 Two DIs are connected to the TSI: one is dedicated to even TSI time slots, and one is dedicated to odd TSI time slots. Each DI provides 256 time slots to the receive TSI RAM. Sixteen-bit time slots in nibble format are sent to the TSI by the DIs (PCM, A-G, and parity). The seven signaling and control bits, A-G, are transmitted with the PCM bits through the receive TSI RAM and are also sent to the SP.

2.45 The TSI transmits 16-bit time slots in nibble format to the DIs. Of the A-G bits sent to the DIs, the E-G bits are always sourced from the SP. The A, B, C, and D bits can either be sourced from the SP or passed through from the transmit TSI RAM. All PCM data sent to the DIs passes through the Attenuation ROM. The attenuation ROM allows one of 31 values of digital loss to be inserted in the PCM data path on a per-time-slot basis. The loss values are 0dB through 15dB of 0.5dB increments. The integrity of the data path (TSI to peripheral unit to TSI) is protected by a walking parity scheme administrated by the TSI that inverts the parity sense of every ninth TSI time slot.

2.46 The TSI receives 512 time slots from the DLI via two 256 time slot nibble buses. The TSI selects which DLI (e.g., DLI0 or DLI1) is the source of time slots to the TSI. This is accomplished by automatic time slot switching (AUTISS) that allows the TSI to switch its network data source on a per-time-slot basis between the active and standby sides of the system based on a validity marker (E-bit signaling stream) in each time slot. If AUTISSing occurs for 256 consecutive frames, the chip outputs a 125 μsec pulse that can be used to alert system software to the switching activity.

2.47 The TSI transmits 512 time slots toward both DLIs in the MCTU. The time slots consist of 16 bits in nibble format. The E bit of each time slot sent to the DLIs is set on a per-time-slot basis via a TSI control RAM written by the SMP. The A-D bits of each time slot sent toward the DLIs are either passed through from the receive TSI RAM or sourced from a TSI control RAM.

2.48 Two forms of connections are possible between the XMIT and RCV RAMs. The first connection allows intramodule paths to be set up by looping time slots on the DLI side of the TSI memories. A connection of this type will block an incoming time slot from the DLIs. The other connection allows intra-DLI connections to be made. A connection of this type will block an incoming peripheral time slot from reaching the RCV TSI RAM, but the blocked peripheral time slots will still have access to the SP and local DSU.

2.49 The alternate data RAM (ADR) provides the SMP and local DSU with access to the contents of all 512 time slots. By means of the ADR the SMP can write constants (e.g., idle code) to be sent to the DIs and DLIs, and sample time slots at various points within the TSI. The ADR also provides SMP access to the E bits received from the DLI. Parity errors on time slots received by the TSI from the DIs are reported to the SMP via the ADR. Data stored in the ADR (e.g., tones from the DSU) can be sent to the DIs, to the receive TSI RAM, or to the transmit TSI RAM. The TSI time slots written to the ADR can be sourced on a per-time-slot basis from four different locations in the TSI. This permits maintenance access and allows time slots from both DIs and DLIs to be sent to the local DSU.

2.50 The SP performs hit timing on all signaling and control bits received from the TSI. This hit timing is performed by scanning the data at a 3 ms rate. A time slot is considered to have changed to a new state only if the bit persists in that state for two consecutive scans.

2.51 Hit timing is accomplished by comparing data on the incoming selected TSI time slot with data contained in the Last Look RAM (LLR). The LLR contains the values of the signaling and control bits from the selected TSI time slot during the previous 3 msec scan. Every 3 msec all 512 time slots are hit-timed and if a bit has remained the same for two consecutive 3-ms scans it passes the hit timing algorithm.

2.52 The state of all signaling and control bits received by the SP from the TSI are stored after hit timing in the LRR through the LRR, the SMP has access to the most recent hit timed state of all signaling and control bits of all time slots received by the TSI from the peripheral units and all signaling and control bits whose state, after hit timing, has changed. The SP is also capable of storing (in an SMP-readable FIFO) the peripheral time slot number.

2.53 State change calculations are based on the result of the hit timing circuit, the ignore RAM, and the LRR. The ignore RAM, set by the SMP, indicates on which bits of which time slot state change reports should be made. The LRR contains the previously calculated states of all signaling and control bits after hit timing. If a new time slot bit has passed the hit timing algorithm, i.e., has not changed during the last 3 ms, it is compared to the state stored in the LRR. If a change has occurred, the LRR is updated. If the bit being processed is not set to ignore in the ignore RAM and if there is a change from the state contained in the LRR, the new bit value is written into the report FIFO. All changes for one time slot are collected before the FIFO is written. The FIFO is readable by the SMP.

2.54 The signaling and control bits (A, B, C, D, E, F, and G) are transmitted to the TSI for all 512 peripheral side time slots every 125 μsec. These signaling bits are read from a 512 time slot RAM designated as the M RAM. The M RAM is both writable and readable by the SMP.

DATA INTERFACE - FS 14, 15, 16, 17

2.55 The data interface (TN876) interfaces the TSI to the various peripheral units that may be attached to the SM. In an international application, the TN1129 will be used in place of the TN876. These circuit packs are identical in function. The only difference in the TN1129 involves the sourcing of idle code that has a different bit pattern from the TN876.

2.56 In the incoming direction, the data interface performs a multiplexing function by combining the time slot traffic of several peripheral units onto a single bus for the TSI; in the outgoing direction. it demultiplexes a single bus from the TSI to the various peripheral units.

2.57 The DI communicates with each peripheral unit over a peripheral interface data bus (PIDB). Each of these buses consists of four signals: serial data in, serial data out, a 4.096-MHz clock, and an 8-KHz sync. The data in and out operate at 4.096 megabits/second, carrying 32 time slots per frame, with 16 bits per-time-slot. Up to 16 PIDBs may be connected to the DI, with each PIDB carrying traffic to a service group in one of the peripheral units.

2.58 The DI passes data to and from the TSI over nibble buses. These buses operate at 8.192 megabits/second carrying 256 time slots per 125-µsec frame (two DIs, each connecting 256 time slots, are needed to carry traffic for the 512 time slot TSI). With 512 peripheral side time slots (16 PIDBs x 32 time slots) and 256 TSI side time slots, the DI can perform a 2:1 concentration function.

2.59 All PIDBs operate in synchronization. In the time of a single PIDB time slot, eight time slots are sent and received from the TSI. After a single time slot from all 16 PIDBs has been clocked into the DI, up to eight of those are chosen (via control information received from the TSI) to be inserted into the eight time slots to the TSI. The time slots not selected are blocked and lost. If less than eight are chosen, "1s" are sent on the nibble bus to the TSI in the time slots for which no PIDB time slot was connected.

2.60 In the outgoing direction, the TSI provides eight time slots to the DI during a single PIDB time slot period. These eight time slots are connected, again using control information received from the TSI, to eight of the 16 PIDBs. PIDBs not selected to receive TSI data transmit idle code to the peripheral units.

2.61 All eight TSI time slots need not be connected to a PIDB time slot. If less than eight are to be connected to PIDBs, the control information from the TSI associated with the "unused" TSI time slots informs the DI to ignore that incoming time slot. All unselected PIDBs transmit idle code. In this case, more than eight will do so.

2.62 In addition to the nibble bus in and out of the DI from the TSI, the DI also receives from the TSI an 8.192-MHz clock, an 8-KHz sync pulse, four address leads, a board select lead, and two leads used for diagnostics. The 8.192-MHz clock provides all the timing for processes internal to the DI; it is used also to generate the 4.096-MHz clock for the peripheral units. The 8-KHz sync pulse properly synchronizes the DI to the network and generates the sync pulse to the peripheral units. The address leads indicate, on a per-time-slot basis, to which PIDB a given TSI time slot is to connect. The address is used by the DI both for the TSI-to-PIDB demultiplex function, and for the PIDB-to-TSI multiplex operation. The board-select lead informs the DI, again on a per-time-slot basis, whether to connect the TSI time slot to the PIDB, as determined by the address, or to ignore that time slot and make no connection to it. The diagnostic leads are used to loop data received from the TSI through the DI circuit and back to the TSI. These leads also provide the capability of having the DI loop idle code back to the TSI rather than the received TSI data. Maintenance of the DI, as well as of the PIDB and parts of the peripheral units, is performed by the TSI by means of the walking parity scheme.

CONTROL INTERFACE - FS 18, 19, 20, 21

2.63 The control interface (UN71B) provides the control interface between the SMP and the various peripheral units. This interface is used for control information to and from the SMP. The peripheral interface is a peripheral interface control bus (PICB). Up to 23 PICBs are available with each CI. Either one or two CIs may be equipped in the MCTU, thereby providing a maximum of 46 PICBs. Each PICB contains five twisted-wire pairs that carry clock, output data, input data, SMP select information, and peripheral unit service requests.

The interface to the SMP is by way of the SMP subunit interface bus. This bus is a parallel, 16-bit bidirectional data bus with a 6-bit address bus. The CI contains several registers that are accessible by the SMP through this bus.

The CI performs four functions for the SMP:

1. Permits the SMP to write 16 bits of information to a peripheral unit register (maximum of 256 destination registers).

2. Permits the SMP to read 16 bits of information from a peripheral unit register (maximum of 256 source registers).

3. Receives, latches, and reports service requests from peripheral units.

4. Detects and reports CI operational errors.

2.64 The CI reads and writes peripheral registers through an exchange of serial messages over the PICB. A distribute operation writes 16 bits of data into a peripheral unit destination register. A scan operation reads 16 bits of data from a peripheral unit source register.

2.65 The SMP will initiate all scan and distribute operations. In all scan and distribute operations, the peripheral unit will send a reply message back to the CI. In the reply message there is a 3-bit all seems well (ASW) code. These bits are used to report errors detected by the peripheral unit. If errors are detected during a scan or distribute order by either the CI or a peripheral unit, the error will be reported by latching a bit in the error source register. The interrupt lead to the SMP will become active if an error occurs, the ability to inhibit this interrupt on a per-PICB basis is provided.

2.66 In addition to performing scan and distribute orders, the CI reports peripheral unit service requests by latching an active state on the PICB interrupt lead into the interrupt source registers. Inhibit registers (remote interrupt inhibit registers) are provided such that these service requests may be handled by interrupts or polling.

PACKET INTERFACE

2.67 The Integrated Services Digital Network (ISDN) Switching Module (SM) incorporates the PSU to provide a centralized high bandwidth interface to support packetized signaling messages, packet data switching, and OSPS operator data messages. By centralizing packet processing in the PSU, efficient signaling, maintenance, and administrative interfaces are maintained and the distributed architecture of the 5ESS Switch is enhanced. The PI will be packaged as a part of the Time Slot Interchanger Unit.

3. INTERFACES

EXTERNAL INTERFACES

A. RSM Intervention - CAD 1

3.01 The element identifiers BB and BC of this CAD show the interconnections between the SMP and the RSM status panel. These panels will be present in all RSMs and will allow an operator to monitor the status of each RSM. The RSM status panel will allow the following operations:

1. Force either side of the SMP active.

2. Monitor the status of communication between the RSM and the host by indicating the state of the links between them.

3. Monitor the status of the SMP by indicating the current state of sanity in each processor.

B. Memory Data, Address, and Control

3.02 This bus connects the SMP's dynamic memory controllers (TN875B), located on a separate shelf, to all additional memory circuit packs in the memory expansion unit (MEU). It consists of the following:

1. 40 bidirectional data leads. This is composed of 32 data bits (4 bytes) plus 8 bits of hamming and parity.

2. 20 bidirectional address lines plus two parity leads. There are 8 row address leads, 8 column address leads, a row parity and column parity lead, and four array selects to select a 64K array.

3. 14 memory control signals used for selecting memory boards, initiating memory cycles, controlling memory data bus direction, indicating refresh operations, strobing data into memory, and providing upward compatibility with future memory board designs.

C. SMP Ground Access - CAD 1

3.03 The backplane ground connections between the MCTU and MEU appear in element identifier IE of this CAD.

D. Controller Power

3.04 All controller power converters are connected to the fuse block by means of a hot lead -48V and a ground potential lead 48RTN.

E. Fan Unit Scan and SD Points - CAD 1

3.05 A fan failure is reported to the SMP by means of a scan point from the Fan Unit. A fan alarm can be retired by the SMP using a distribute point to the Fan Unit. The element identifiers AE and AL of this CAD show the scan and distribute point of side 1 and side 0, respectively.

F. MEU Power and Control

3.06 These cables connect the MCTU to the MEU to provide control and display functions if additional memory is needed by the SMP. If an MEU is not connected to the MCTU, 982JJ shorting bergs will replace these cables to provide a path from the MCTU converters back to the SN516.

G. NCT Link Interface - CAD 1

3.07 The serial data received and transmitted over the NCT links is at a 32.768-MHz rate. The DLI will track the received serial data up to ±1 KHz of the nominal frequency (±32 PPM). Each frame consists of 256 16-bit time slots. Bits 0 through 7 are PCM data bits in the 255 voice and data time slots. Bits A through E are signaling bits. The G bit is the bit position into which the pseudo-random framing sequence is inserted. The F bit is toggled at the beginning of each frame and is used for fault detection in the DLI/TMS interface (in a multi-module office) or the DLI/MICU interface (in a single-module office). The P bit is such that the 16 bits of the time slot have odd parity. In the message time slot, bits 0 through 5 are the data bits that contain data to/from the SMP; bit 7 is the central processor intervention bit. The element identifiers of this CAD are as follows:

1. Side 1: CW, CX or IW, IX

2. Side 0: DA, DB or IY, IZ

   The element identifiers IN, IM, IR, IQ of this CAD show the NCT Link for Optically Remoted Switching Module (ORM) side 0 and the element identifiers IL, IK, IO, IP is used to show NCT Link for ORM side 1. There are optional element identifiers of CAD 1 used to provide the "2-Mile ORM" NCT Link fiber optic connector. The "2-Mile ORM" is officially known as "Transmissionless Remote Module" (TRM).

H. LDSU Interface - CAD 1

3.08 The MCTU communicates to the local digital service unit (LDSU) over two dedicated serial ports connected to the TSI. The TSI transmits and receives 32 serial time slots to and from each of two service groups in the LDSU. Any of these 64 time slots can be selected as a source of PCM data for any time slot going to the DLIs or DIs. Similarly, the TSI can send the 16-bit word of any time slot received from the DLIs or DIs out on any of the 64 time slots to the LDSU. The data format and timing of the LDSU interface is of the PIDB type consisting of four balanced, differentially driven, RS-422 compatible, twisted-pair wires. Signals provided by this interface are a 4.096-MHz clock out, an 8-KHz sync pulse out, 32-time slot serial output data, and 32-time slot serial input data.

3.09 The twisted pairs carrying data from the LDSU to the TSI are terminated with a discrete resistor providing a differential mode termination of 220 ohms and a common mode termination of 55 ohms. The 8-KHz sync pulse is normally "high", and goes "low" for one clock period (244 nsec) every frame (125 μsec).

In a normally functioning SM, each service group in the LDSU will receive two of the PIDB-like interfaces described above, one from each side of the duplex TSI, with only one active at any given time. Identical data will be present on both buses to a given service group.

3.10 The element identifiers of dedicated PIDBs are GE and GF for side 1, and element identifiers GO and GP are for dedicated PIDBs side 0.

I. Peripheral Interface Data Bus - CAD 1

3.11 A PIDB provides the physical link for traffic between the DI of the SM and any peripheral unit connecting to the DI. It consists of four balanced, differentially driven, RS-422[3] compatible twisted wire pairs.

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3. EIA (Electronic Industries Association) RS-422 standards for balanced voltage digital interfaces.

3.12 The PIDB carries 4.096 megabit/second serial data from the DI to the peripheral units, a 4.096-MHz clock and 8-KHz sync to the peripheral units, and 4.096 megabit/second serial data to the DI from the peripheral units. The twisted pair carrying data from the periphery is terminated at the DI. The PIDB cable may vary in length, but it has a maximum limit of 20 feet.

3.13 The 4.096-MHz clock has a 244-ns period. The duty cycle of the clock, excluding this ±20 ns. is 50% ±5%. The 8-KHz sync is a normally high signal ("1" state) that pulses low for one 4.096-MHz clock period every 125 μs.

3.14 The peripheral units should clock PIDB data in from the DI on the falling edge of the 4.096-MHz clock, and clock data out onto the PIDB on the rising edge of that clock.

3.15 During the sync pulse, the peripheral should clock PIDB time slot No. 29, bit 7 in from the PIDB on the negative edge of the 4.096-MHz clock and clock out PIDB time slot No. 31, bit 15 onto the PIDB using the positive edge of the clock. Note the 2 1/2 ns time slot skew between incoming and outgoing information - this is caused by the skew required by the TSI and DI to perform their functions.

3.16 A peripheral unit service group will receive a PIDB from each side of the duplex MCTU. In a fully operational SM, data will flow over both PIDBs. Using control information received from the SMP via the CI, the peripheral unit will select only one PIDB from which to receive information. However, it will transmit the same data back over the PIDBs. The skew of the two PIDB clocks received from the duplex SM can be up to ±60 ns.

3.17 The elements identifiers of PIDB on side 1 are: CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CT, CU, CV, FP, FQ, FR, FS, FT, FU, FV, FW, FX, FY, FZ, GA, GB, GC, GD.

3.18 The elements identifiers of PIDB on side 0 are: DE, DF, DG, DH, DI, DJ, DK, DL, DM, DN, DO, DP, DQ, DR, DS, DT, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, HA, HB, HC, HD, HE.

J. <u>Peripheral Interface Control Bus (PICB) - CAD 1</u>

3.19 A PICB consists of 5-wire pairs that are used for balanced data transmission and signaling. The clock pair carries a 2.048-MHz gated clock signal to the peripheral units; the data out pair carries serial information to the peripheral units from the CI; the data in pair carries serial data from the peripheral units to the CI. The select lead carries signaling information which is used to select the active side CI, and the interrupt pair transmits service requests from the peripheral units.

Although the cable length of the PICB may vary, it has a maximum limit of 20 feet.

Data is to be gated in and out of the peripheral unit on the negative edge of the clock. The avoid a timeout error, the reply must be received by the CI within 21.5 μsecs from the first clock pulse.

The elements identifiers of PICB on side 1 are: BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU, BV, BW, BX, BY, BZ, CA, CB, CC, CD, CE, CF.

The elements identifiers of PICB on side 0 are: DU, DV, DW, DX, DY, DZ, EA, EB, EC, ED, EE, EF, EG, EH, EI, EJ, EK, EL, EM, EN, EO, EP.

K. Alarm Interface - CAD 1

3.20 The alarms are divided into four failure groups; DLI side 0, DLI side 1, controller side 0, and controller side 1. The DLI alarm consists of two signals to the fuse block for monitoring blown fuses. The alarm input lead monitors the 70-type indicator fuses used in the fuse block. When a fuse is blown, the fuse connects -48 volts to the alarm input lead. This lead lights the alarm LED on the control and display pack and connects the Y scan point to ground. The alarm test output lead is used by diagnostics to test continuity of the alarm connections to the fuse block and Y scan point operation.

3.21 The controller alarm interface has the same two alarm connections as the DLI alarm interface with the addition of a Z scan point monitor. The Z scan point monitors a group of fuses that protects power to the peripheral units. If a fuse is blown here, -48 volts is connected to the Z scan point alarm input and causes the scan point to be connected to ground. A test output is also provided for diagnostic testing.

3.22 The element identifiers to show the fuse alarms on side 1 are EQ and CY; the ones on side 0 are DC and ID.

INTERNAL INTERFACES

A. SMP Subunit Interface Bus

3.23 The SMP subunit interface bus is used as the control interface to the TSI, SP, and CI from the SMP. It utilizes a 16-bit bidirectional data bus and a 6-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two parity leads (bidirectional also), one each for the low byte and high byte of data. The parity is computed such that the sum of bits set to a logic one in each byte (including the parity bit) is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

3.24 Each subunit has five control leads. Two of these, the Read and Write signals, are shared by all subunits. These two signals distinguish between read and write operations to a subunit and are used by the selected subunit to gate the data to/from the data bus. The other three controls are Board Select, Ready, and Interrupt. Each individual subunit has separate Board Select, Ready, and Interrupt leads. the Board Select lead enables the desired subunit, the Ready lead allows the subunit to extend the SMP bus cycle for subunits with slower response time, and the Interrupt lead allows the subunit to interrupt the SMP.

In addition, the CIs receive a lead called NAE that is used to force the Select wire pair in the PICB on the non-active side to a nonconductive state.

B. SMP Message Interface

3.25 After the message time slot has been extracted from the normal data path through the LI, parity is checked and generated over the 6 bits that will be sent over the 48-KHz data links to the synchronous data link controllers (SDLCs) in both sides of the SMP. The generated parity is also sent to the SDLCs in both sides of the SMP over separate data leads. At the same time, the central processor intervention (CPI) bit is sent to the CPI gate arrays in both sides of the SMP. Two clocks are sent to both sides of the SMP from the clock circuit in the DLI. These clocks are used by the

SMP to clock the received message time slot data and parity into the SDLCs. In the return direction, the SMP uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each LI contains a message interface to and from both sides of the duplex SMP.

C. SMP-DLI Control Interface

3.26 The SMP-DLI control interface three signal leads and one clock lead from each side of the SMP to the DLI and two signal leads from the DLI to each side of the SMP. A control lead originates from each side of the SMP to indicate which side is sending commands to the DLI. Another control lead comes from each SMP side to control when a read or write command is executed by the DLI. A 1.875-MHz clock is sent by each SMP side along with the data that specifies the command to be executed. The entire write operation is specified in a serial 16-bit command in which the first 8 bits contain the data to be written, followed by a spare bit and a parity bit for the 8 bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four address bits that specify the register to be written. During a read operation, only 6 bits are sent by the SMP to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits that determine the register to be read. Following the execution of the read command as initiated by the module processor go (MPGO) signal, 8 bits of data plus one parity bit (parity over the data) are sent back to both sides of the SMP on separate signal leads with the results of the read operation. Interrupt leads indicating that error conditions exist in the ESRs of the DLI are also a part of the SMP-DLI control interface. These signals are asynchronous to the SMP and have no specified timing relationship.

D. TSI-DLI Interface

3.27 The TSI transmits the 512 DLI time slots to both DLIs in the MCTU. In the opposite direction, the TSI provides a switch, set under SMP control, to select the 512 DLI time slots from one of the two DLIs. This provision allows the TSI to be configured to receive its time slots from the active DLI, and under normal (no fault) conditions, to switch between the two DLIs, on a per-time-slot basis, without introducing data errors. The interface consists of two 256 time slot buses to and from each DLI. Each bus transmits 16-bit words made up of four consecutive 4-bit nibbles. The parity bit is set such the sum of bits (including parity) set to a logic one is odd. Each DLI supplies the TSI with an 8.192-MHz clock, an 8-KHz sync pulse, and a 6 msec sync pulse in addition to data. the TSI is required to perform an error free switch when selecting a DLI timing source. To accomplish this switch the maximum DLI clock skew between the duplicated DLIs cannot exceed 20 nsec.

E. TSI-SP Interface

3.28 The TSI sends the seven signaling bits (A-G) of all 512 time slots received from the DIs to the Signal Processor. The time slots consist of two consecutive 4-bit nibbles and are accompanied by an 8.192-MHz clock and a 6 msec sync pulse. In the opposite direction, the TSI receives the seven signaling bits (A-G) from the SP for all 512 outgoing peripheral time slots. Of these 7 bits received, the E, F, and G are always sent toward the DIs. The A through D bits are selectable as a group. They can either be passed through the TSI from the DLI or can be selected to be sourced by the SP. Even parity is used on the even time slot bytes and odd parity is used on the odd time slot bytes.

F. TSI-DI Interface

3.29 The interface between the TSI and the DI consists of a nibble bus in each direction carrying call traffic, control information from the TSI to the DI, clock, and sync.

Two DIs may be connected to the TSI (1 even, 1 odd), each supplying 256 time slots in nibble format.

3.30 The nibble buses carry a time slot on four consecutive nibbles, and operate at 8.192 mbits/sec; 256 time slots per frame are transmitted in each direction to each DI. These buses use a walking parity scheme for fault detection. In this scheme the parity is normally odd but in every ninth time slot, the parity is even.

3.31 The control information includes a 4-bit PIDB address that selects the source and destination for the 512, time slots associated with the DIs and a DI board select lead. This lead tells the DI to connect the TSI time slot with which it is associated to the specified PIDB, or to ignore the time slot and make no PIDB connection to it.

3.32 Two additional leads are used to diagnose the DI. One lead informs the DI to loop the TSI data received on that time slot through itself and back to the TSI on the same time slot of the next frame. The other lead directs the DI to replace the received TSI data with PIDB idle code.

3.33 The clock lead nominally is an 8.192-MHz clock (122 ns period). the 8-KHz sync is a normally "high" signal with an active "low" pulse of one 8.192-MHz period in duration occurring every 125 µs (once per frame).

G. ITS Test Access

3.34 The intergrated test system (ITS) interface pack (TN319) provides the means of accessing a host system (UNIX) from the MCTU. Use of ITS permits a user to interactively examine and modify the execution of an application program. ITS accommodates step-by-step execution of target programs, the setting of breakpoints, and the running of error detection programs.

H. NMAT Test Access

3.35 The noninterfering match and trace (NMAT) interface provides access to either processor via the update bus. The test set may also take active control of the update bus to control either processor. All memory operations are reported to the test set for its tracing and breakpoint features via the update bus.

3.36 The six test set status signals available in the update bus indicate whether the current operation on the update bus is a read, write, or opcode fetch. They also force a processor into the dormant state independent of all resets or force a processor to release the update bus to allow the test set to use it for controlling the processor.

I. Update Bus

3.37 The update bus runs between both processors and is used by the active processor for keeping all data areas in the standby processor up to date, by the BTSR when pumping a processor, and as a test access point for monitoring the activity of the processors.

3.38 The update bus consists of the following:

1. 25 bidirectional address lines with parity. The address space is treated as 1024K 16-bit words with separate byte selects. Even parity is used over the update bus.

2. 18 bidirectional data and parity lines (16 bits data and 2 bits parity).

3. Two bidirectional byte select signals. These selects indicate which data byte is affected by the data transfer. Both selects active indicate a 16 bit operation while one active indicates an 8-bit operation.

4. Six text set status signals.

5. Two cross coupled reset signals, one causing a maskable reset in this SMP (an input), the other a maskable reset in the mate processor (an output).

6. Two status signals indicating the running/dormant status of each processor. One signal, when active, indicates that this processor is in the dormant state. The other signal, when active, indicates that the mate processor is in the dormant state.

7. Four error status signals. Two indicate the occurrence of a subunit or processor error in this processor; two indicate the occurrence of a subunit or processor error in the other processor.

3.39 The positive edge of UADCLKB latches the update address in the mate processor. A high level on UWAITO indicates a ready state of the memory system in the dormant controller. Control signals URDO and UWRO are used for sending read/write data to/from the mate.

3.40 The refresh strategy allows each SMP autonomous control of refreshing. Writes to the mate are done on a delayed asynchronous basis. For each write operation, the address and data are latched at the mate processor to allow the write to proceed until the next mate memory operation from the running processor. In the update mode, only writes are done in both processors. Between each write there normally are several read operations for either opcode fetching or data reads. The low duty cycle of writes provides a large average time per write for the dormant memory system. Allowing the write to proceed on the mate after it has completed in the running controller requires that before starting any memory operations directed to the mate processor, it is necessary to check the ready status of the mate memory system. The ready logic delays the running processor until the mate memory is ready whenever the running processor attempts to initiate a mate memory operation.

3.41 A read from the mate memory waits until the read data is available before proceeding to the next instruction. Three wait cycles are added to the memory operation to insure sufficient time for a ready signal to be returned from the mate during the read. The read is further delayed one clock cycle before reaching the processor to insure proper de-skewing of the read data and ready.

3.42 The write data and memory address are latched at the mate controller because the update bus must still reflect the processor operations between successive mate writes.

J. DLI Time Slot Select Switch

3.43 Each DLI has two message time slot registers for the A and B NCT links. Each message time slot register has two modes of operation: software programmable and backplane programmable. The backplane programmable mode is selected by plugging the 955B message time slot select switches onto the CAD 21 and 22 locations. The backplane switches automatically ground the message address enable lead allowing the switches to indicate an 8-bit binary number corresponding to the NCT link time slot used for transmitting messages to and from the SMP and administrative module. After the switches are removed, the address enable lead is pulled high and the message time slot number can be programmed by the SMP writing to the message time slot address registers of the DLI.

K. Controller Power

3.44 All controller power converters (495FB, 494RA, 988A) are connected to the fuse alarm via a hot lead -48V and a ground potential lead 48RTN.

L. Link Monitor Test Access

3.45 The interface between the DLI and SMP can be monitored by the communication link monitor when installed in this CAD location.

M. MCTU Ground Access

3.46 The backplane ground connections between the two shelves appear in this CAD.

N. Control and Display to FIU - CAD 1

3.47 In an RSM environment, the facilities interface unit (FIU) will become part of the DLI service group via cables installed at the locations specified in these CADs. If the MCTU is not in an RSM environment, 982JJ shorting bergs will replace these cables to provide a path from the DLI converter back to its SN516 functions.

3.48 The element identifiers of C&D to FIU (in RSM) or to TRCU (in ORM) on side 1 is CZ and on side 0 is DD.

O. Wiring for Smart Signal Processor

3.49 There is an element identifier on the backplane to provide the wiring for a future application of a smart signal processor.

P. Wiring for ISDN Packet Interface

3.50 There is an element identifier on the backplane to provide the wiring for a future application of an ISDN packet interface function.

Q. Data Interface Subunit Bus Access

3.51 There is an element identifier on the backplane to provide the DI circuit packs with access to the SMP sub-unit interface bus if a future upgrading of a DI to a "smart" DI is needed.

R. ISDN Packet Interface Access - CAD 1

3.52 There are element identifiers to provide access to the Packet Interface function via twisted pair signals from the rest of the ISDN circuitry located in another cabinet.

3.53 Those element identifiers are: IT, IS for side 1; and IV, IU for side 0.

UNIT LAYOUT

3.54 A 150-watt, 2-inch, 495FB BELLPAC power converter is used to provide +5-volt power to all circuits on the bottom shelf of the MCTU with the exception of the BTSR which has its own on-board power supply. A 100-watt, 1 in., 494LA BELLPAC power converter is used to provide +5-volt power to all circuits on the top shelf related to the TSI functions. The DLIs will use a 5-volt 35-watt, 12-volt 5-watt onboard BELLPAC power converter. Two spare slots have been provided in the top shelf on each side to provide for future introductions of a "smart" signal processor and a processor interface for ISDN. A slot is also reserved for an SDLC link monitor. Three center locations in the shelf are used for test access, ITS, and the BTSR, respectively.

3.55 The MCTU consists of two shelves of circuit packs. The shelves are divided into duplicated halves, right and left side. The right half is an exact duplicate of the left, the only exception being physical location. The physical location of each circuit pack is a mirror image of the other half, rather than maintaining the same physical relationship between circuit packs. Each half is a single failure group.

3.56 In its fully equipped state the MCTU will contain the following:

MCTU

Pack Code	Quantity	Description
TN1086	2	Time Slot Interchange/Signal Processor
TN876/ TN1129	4	Data Interface -or-
TN1377/ TN1524	4	Fanout Data Interface
SN516	2	Control and Display
TN1077/ TN1077B	2	Dual Link Interface
UN71B	4	Control Interface
495FB	2	2" Power Converter
494LA	2	1" Power converter
TN871/ TN871B	2	Module Processor -or-
TN1397	2	Module Processor [5E4(2)]
TN872	2	Module Processor
TN873	2	Module Processor -or-
TN1533	2	Module Processor [5E4(2)]
TN874/ TN874B	2	Module Processor
TN875B/ TN875C	2	Module Processor -or-
TN1527	2	Module Processor [5E4(2)]
TN56	10	Module Processor

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltage Limits

a. +5±0.5-volts

b. +12±1.2-volts

1.02 Ambient Temperature

a. 0% to 70% Centigrade (at circuit pack).

b. 0% to 50% Centigrade (office aisle ambient).

1.03 Growth - Each side of the MCTU comes equipped with 32 PIDBs and 23 PICBs. The unit may be expanded by adding another control interface to each side, for a total of 46 PICBs per side.

2. FUNCTIONAL DESIGNATIONS

FDESIG	MEANING
0CI0	Side 0, Control Interface 0
0CI1	Side 0, Control Interface 1
1CI0	Side 1, Control Interface 0
1CI1	Side 1, Control Interface 1
0DI0	Side 0, Data Interface 0
0DI1	Side 0, Data Interface 1
1DI0	Side 1, Data Interface 0
1DI1	Side 1, Data Interface 1
DLI0	Side 0, Dual Link Interface
DLI1	Side 1, Dual Link Interface
OPTRCV	Receive Fiber Link to DLI
OPTXMIT	Transmit Fiber Link from DLI
TSI0	Side 0, Time Slot Interchanger/Signal Processor
TSI1	Side 1, Time Slot Interchanger/Signal Processor
0C/P	Side 0, Control and Power
1C/P	Side 1, Control and Power
0DLIC/P	Side 0, DLI Control and Power
1DLIC/P	Side 1, DLI Control and Power
0TSSDLIA	Side 0, Time Slot Switch for DLI Link A
0TSSDLIB	Side 0, Time Slot Switch for DLI Link B
1TSSDLIA	Side 1, Time Slot Switch for DLI Link A
1TSSDLIB	Side 1, Time Slot Switch for DLI Link B
0MEM1	Side 0, Memory Board 1
0MEM2	Side 0, Memory Board 2
0MEM3	Side 0, Memory Board 3
0MEM4	Side 0, Memory Board 4
0MEM5	Side 0, Memory Board 5
0MPC	Side 0, Module Processor Core Board
0MPCOM	Side 0, Module Processor Communication Board
0MPDMC	Side 0, Module Processor Dynamic Memory Controller
0MPROMRA	Side 0, Module Processor RAM/ROM Board
0MPS	Side 0, Module Processor Support Board
1MEM1	Side 1, Memory Board 1
1MEM2	Side 1, Memory Board 2
1MEM3	Side 1, Memory Board 3
1MEM4	Side 1, Memory Board 4
1MEM5	Side 1, Memory Board 5
1MPC	Side 1, Module Processor Core Board
1MPCOM	Side 1, Module Processor Communication Board
1MPDMC	Side 1, Module Processor Dynamic Memory Controller
1MPROMRA	Side 1, Module Processor RAM/ROM board
1MPS	Side 1, Module Processor Support Board
BTSR	Bootstrapper Board

3. FUNCTIONS

The function of this unit is described in Section 1 of this Circuit Description.

4. CONNECTING CIRCUITS

Time Multiplexed Switch Unit - SD5D061-01

Fan Unit - SD5D019-01

Fuse/Filter Panel - SD5D053-01

Peripheral Units

(a) Line Unit - SD5D051

(b) Trunk Unit - SD5D300

(c) Digital Line and Trunk Unit - SD5D201

(d) Metallic Service Unit - SD5D033

(e) Digital Service Unit - SD5D035

(f) Transmission Rate Converter Unit - SD5D086

(g) Packet Switch Unit - SD5D074

5. MANUFACTURING TESTING REQUIREMENTS

Refer to:

DS5U 1.04.01.00
COST-REDUCED TIME SLOT INTERCHANGE UNIT
UNIT TEST PLAN
DESIGN SPECIFICATION
CASE 40288-600
AUTHOR: L. K. TEMPLE

6. REFERENCES

Supplementary information is contained in the following documents:

1. SN516 Circuit Description in CPS-SN516
2. TN876 Circuit Description in CPS-TN876
3. TN1086 Circuit Description in CPS-TN1086
4. TN1077 Circuit Description in CPS-TN1077
5. TN1077B Circuit Description in CPS-TN1077B
6. UN71B Circuit Description in CPS-UN71B
7. TN871/TN871B Circuit Description in CPS-TN871
8. TN1397 Circuit Description in CPS-TN1397
9. TN872 Circuit Description in CPS-TN872
10. TN873 Circuit Description in CPS-TN873
11. TN1533 Circuit Description in CPS-TN1533
12. TN874 Circuit Description in CPS-TN874
13. TN874B Circuit Description in CPS-TN874B
14. TN875B/TN875C Circuit Description in CPS-TN875B
15. TN1527 Circuit Description in CPS-TN1527
16. TN878 Circuit Description in CPS-TN878
17. TN1617 Circuit Description in CPS-TN1617

7. ACRONYMS

ADR	alternate data RAM
AM	administrative module
ASW	all seems well
AUTISS	automatic time slot switching
BTSR	bootstrapper
CAD	cabling and distribution
CI	control interface
CP	control processor
CPI	control processor intervention
DI	data interface
DLI	data link interchanger
DLI	data link interface
DMA	direct memory access
DSU	digital service unit
EIA	Electronics Industry Ass'n.
EPROM	erasable, programmable, read-only memory
ESR	error source register
FIFO	first in, first out
FIU	facilities interface unit
FLA	functional logic array
I/O	input/output
ITS	integrated test system
ISDN	integrated service digital network

LDSU	local digital service unit
LLR	last look RAM
LI	line interface
LSI	loop supervision incoming
MCTU	module controlled time slot interchange unit
MP	module processor
MDF	mate power fail
MEU	memory expansion unit
MPGO	module processor go
MSGS	message switch
MTS	message time slot
NCT	network control and timing
NMAT	noninterfering match and trace
NMI	nonmaskable interrupt
OOS	out of service
PCM	processor control module
PICB	peripheral interface control bus
PLL	phase lock loop
RAM	random access memory
RCV	receive
RSM	remote switching module
SDLC	synchronous data lock controller
SM	switching module
SMP	switching module processor
SP	signal processor
TMS	time multiplexed switch
TSI	time slot interchange
VCXO	voltage controlled crystal oscillator
VLSI	very large scale integration
XMIT	transmit

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