5ESS™ SWITCHING EQUIPMENT

SWITCHING MODULE CONTROL CABINET CIRCUIT

CHANGES

D. Description of Changes

D.1 Added wiring option "C" for standard SM configuration and wiring option "T" for single bay SM configuration.

D.2 Changed the name Interface Module Control Cabinet to Switching Module Control Cabinet.

D.3 Assigned netnames to spare leads and wiring option added to MEU Cads to correct documentation errors.

AT&T BELL LABORATORIES

DEPT 55614-DEH-CEJ

5ESS™ SWITCHING EQUIPMENT

INTERFACE MODULE CONTROL CABINET

CIRCUIT

CHANGES

D. Description of Changes

D.1 This change is a documentation change to remove repetitious information from the cabinet SD that is shown in unit SDs and to reconfigure the feature and option table. The following CADs are removed: 1,2,3,4,5,6,7,8,10,11,12,13,14,23,27,28, and 29. The remaining CADs are renumbered as follows: 9A to 1, 9B to 2, 15 to 3, 16 to 4, 17 to 5, 18 to 6, 18A to 7, 18B to 8, 19 to 9, 20 to 10, 21 to 11, 22 to 12, 24 to 13, 25 to 14, 26 to 15, 30 to 16, and 31 to 17.

AT&T BELL LABORATORIES

DEPT 55614-DEH-DPS

5ESS™ SWITCHING EQUIPMENT
INTERFACE MODULE CONTROL CABINET
CIRCUIT

CHANGES

D. Description of Changes

D.1 This change is a documentation change to assign netnames to formerly "spare" leads in cables.

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DEPT 55614-DEH-DPS

5ESS™ SWITCHING EQUIPMENT
INTERFACE MODULE CONTROL CABINET
CIRCUIT

CHANGES

D. Description of Changes

D.1 This change corrects the wiring for the RSM craft intervention key, removes CAD 23, and makes changes required to use the SN516 control and display circuit pack.

AT&T BELL LABORATORIES

DEPT 55614-DEH-EPS

5ESS™ SWITCHING EQUIPMENT

INTERFACE MODULE CONTROL CABINET

CIRCUIT

CHANGES

D. Description of Changes

D.1 This change transmits design information to allow the use of the export local DSU to be used in the IMC6′ cabinet. This change creates the following new CADs: 9A, 9B, 18A, 18B and changes CADs 1, 3, 5, and 7. New App. Figs. are created for the domestic local DSU and export local DSU.

AT&T BELL LABORATORIES

DEPT 55614-DEH-DPS

5ESS™ SWITCHING EQUIPMENT

INTERFACE MODULE CONTROL CABINET

CIRCUIT

CHANGES

D. Description of Changes

D.1 This change corrects documentation errors in CAD 18 to pin numbers for DLI power.

AT&T BELL LABORATORIES

DEPT 55614-DEH-DPS

5ESS™ SWITCHING EQUIPMENT

INTERFACE MODULE CONTROL CABINET

CIRCUIT

CHANGES

D. Description of Changes

D.1 This change allows the FIU to be controlled by the DLI service group in the TSIU and adds the memory expansion unit (MEU) to the feature and option table. This change adds CADs 27, 29, and 30, and options V and W, to the feature and option table.

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DEPT 55614-DEH-DPS

5ESS* SWITCHING EQUIPMENT
INTERFACE MODULE CONTROL CABINET
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The interface module control cabinet (IMC) houses the units that provide the operating environment for the software, the time slot interface function, interface to the network, control, and timing (NCT) links, control and data interfaces to all peripheral units[1] within the same interface module (IM), as well as tone generation and decoding for that IM.

1. Digital service unit, metallic service unit, digital line and trunk unit, line unit, and trunk unit, etc.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The IMC houses the interface module processor unit model 2 (IMPU2), the time slot interchange unit model 2 (TSIU2), the local digital service (circuit) unit (LDSU), the fuse/filter unit (FPU), and the fan unit.

INTERFACE MODULE PROCESSOR UNIT (IMPU2)

2.02 The IMPU2 provides the intelligence for the IM. Two module processors (MPs) within the IMPU2 operate in a duplex configuration, such that either MP could singly perform the IMPU2 functions.

2.03 The IMPU2 also contains a fast pump "bootstrapper" (BTSR) capability for initialization of the MP memory.

TIME SLOT INTERCHANGE UNIT (TSIU2)

2.04 The TSIU2 provides the IM with an interface to the NCT links, performs time division switching, provides an interface to the peripheral units for PCM data by use of a peripheral interface data bus (PIDB), and provides the IMPU2 an interface to the message time slots of the NCT links.

2.05 The TSIU2 provides two control interfaces (CIs) for controlling all peripheral units within the same IM.

2.06 The TSIU2 houses the signal processor (SP) that provides the MP access to the signaling and control bits of time slots transmitted to/from peripheral units.

LOCAL DIGITAL SERVICE UNIT (LDSU)

2.07 The LDSU provides the high-usage functions of tone generation and tone decoding for its associated IM.

The LDSU connects to the IM via local digital service unit bus (LDSUB) and peripheral interface control bus (PICB).

FUSE/FILTER UNIT (FFU)

2.08 The FFU provides fusing for all equipment units located in the same IMC bay.

FAN UNIT (FU)

2.09 The fan unit provides air flow for maintaining correct operating temperatures.

SECTION II - DETAILED DESCRIPTION

1. FUNCTIONAL DESIGNATIONS

1.01 The IMC has five subfunctions, the interface module processor unit model 2, the time slot interchange unit model 2, the local digital service circuit unit, the fuse/filter unit, and the fan unit.

1.02 The IMPU2 provides the intelligence for the IM and the fast pump capability.

1.03 The TSIU2 performs time division switching, provides the interfaces to the NCT links, the peripheral units, the signaling and control bits of time slots transmitted to/from peripheral units, and the message time slots of the NCT links.

1.04 The LDSU provides the high-usage functions of tone generation and tone decoding for its associated IM.

1.05 The fuse/filter unit provides fusing for all equipment units located in the same IMC bay.

1.06 The fan unit provides air flow for maintaining correct operating temperatures.

2. FUNCTIONS

INTERFACE MODULE PROCESSOR UNIT (IMPU2)

2.01 The IMPU2 has two subfunctions: the module processor (MP) and the bootstrapper (BTSR).

2.02 The MP provides the intelligence for the IM. Two MPs within the IMPU2 operate in a duplex configuration, such that either MP could singly perform the IMPU2 functions.

2.03 The BTSR provides the interface between the fast pump data link and the MP. The BTSR receives serial data from a dedicated PIDB and performs data transfers into the MP memory.

A. Module Processor (MP)

2.04 The module processor function in the IMPU2 is realized using six circuit pack codes: TN871, TN872, TN873, TN874, TN875, TN28. The MP dynamic memory system uses up to eight TN28 memory planes, each of which is 1 Mbyte. This allows a maximum of 8048K[2] of dynamic random access memory (RAM) to be equipped.

2.05 The normal operating mode of the MPs is active/standby. In this mode, one of the processors is actively executing code, called the running state. In addition, the processor is called "active" if its "A" flip-flop is set. The other MP is in the standby mode and is dormant. While dormant, the internal buses of the MP can be controlled by the mate[3] allowing it read and write access to the dormant MP. Whenever an MP becomes dormant, it

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2. K = 1024 bytes

3. Mate refers to the other MP in the IMPU2.

releases control of its internal buses to its mate. This operating mode allows the running MP to keep an up-to-date copy of its memory in the dormant MP.

2.06 The MP can operate in the following hardware states:

1. Running, as previously described, is when the microprocessor is actively controlling its internal buses. While running, the mate is unable to gain access to this microprocessor's buses.

2. When dormant, the microprocessor is in a direct memory access (DMA) hold condition, which grants the mate access to all the internal buses.

3. The DMA transfer mode allows the DMA unit to transfer data bytes to/from the message time slot links. The DMA unit controls the internal buses. If the update mode is enabled, the data writes also occur in the mate.

2.07 Active and standby are software states, distinct from the hardware states. An active MP must be running and have access to the dual link interface (DLIs). A standby MP is dormant with its mate active and keeping its memory up-to-date.

2.08 Three types of memory are provided in the MP: 128K EPROM, 8K of static RAM, and a maximum of 8048K of dynamic RAM used for the operational programs and data. The EPROM provides program storage for power-up initialization and fault recovery. The static RAM provides data storage independent of the dynamic RAM. This is an important feature when exercising the dynamic memory system. The 8K of address space is reserved for I/O access via memory reference instructions.

2.09 The dynamic memory system uses TN28 memory planes, each of which is 1024K bytes. Detection and correction of single-bit memory errors and detection of double-bit errors is provided by hamming parity across all of memory. Memory word size is 40 bits, which includes four bytes of data, parity over each byte, and four bits of hamming. The mapping to the microprocessor's 16-bit word size is accomplished on the memory controller pack.

2.10 A write protection capability is provided on the MP memory. Each 1K byte of data memory is protectable. Each 4K block of text memory is also protectable. All of the text can be protected with a single bit. Any attempt by software to write into a write-protected area results in a reset (nonmaskable interrupt) being applied to the MP and the write being blocked. The selection of whether a particular 1K byte data block or a 4K byte text block of memory is write-protected is made under software control. Additionally, a mechanism for implementing stack protection is available. When activated, the memory region from 0x80000 to 0x100000 becomes write-protected, except for a 2K block assigned to the currently running process. Stacks are available in 2K bytes only, allowing a total of 256 separate stacks.

2.11 To allow efficient control of and response to asynchronous events, 25 interrupts are provided in the MP. Twenty-four of the interrupts are presented to the MP as level-4 interrupts. Errors from the subunits, error reporting and message completion from the data link controllers, time intervals, status changes, and errors are all presented to the microprocessor as interrupts. Two types of level-4 interrupts are provided: a high-priority set of interrupts for reporting errors from the subunits, and a low-priority set (for all other interrupts) that is disabled during the

I/O time interval. The twenty-fifth interrupt arrives at the MP as a level-5 (higher priority) interrupt. This interrupt is generated by the central processor intervention (CPI) gate array and is used to indicate a time multiplex switch (TMS) switch.

2.12 Each MP possesses a sanity timer, which is reset under software control. Failure to reset the timer, or resetting the timer too often, results in a reset (nonmaskable interrupt) being applied to the MP. The active MP resets the timer in the standby MP. A timeout of the sanity timer in the standby MP results in the standby MP leaving the standby state, and under software control, entering the out of service (OOS) or active state. The minimum interval requirement is disabled in the off-line side.

2.13 The MP receives two message timeslots from each DLI. The MP can select any two of these timeslots for message communication with the message switch (MSGS). Messages over these message time slots adhere to the BX.25 communication protocol. Communication with the central processor (CP) is entirely under DMA control in the MP.

2.14 A central processor intervention (CPI) path to each MP is provided to be used as a hardwired path to force an IM into a known state from the CP. The MP has a minimum of control over the path of the CPI message and no control over the designated action taking place. The seven possible CPI actions are:

1. Force side 0 of the MP active, also forces side 1 inactive.
2. Force side 1 of the MP active, also forces side 0 inactive.
3. Clear the force active set by one of the above CPI functions.
4. Force a reset to the MP(s).
5. Disable the sanity timers in both MPs.
6. Enable the sanity timers in both MPs.
7. Level-5 interrupt to MP indicating a TMS switch.

2.15 A mate power fail (MPF) detection capability is provided to prevent the active MP from mutilating the mate's memory when the active MP sustains a power failure. The circuitry prevents an MP that has lost power from writing the mate and forces the mate active.

2.16 A 32-bit counter is used for a stable billing clock. Either DLI 0 or DLI 1 can drive the 32-bit counter with an enable bit provided for each DLI clock. A software strobe point, used for diagnostics, can advance the counter at a software rate if the two clocks are disabled.

B. Bootstrapper (BTSR)

2.17 The BTSR function in the IMPU2 is realized using a single circuit pack code (TN878). The BTSR receives serial data from a dedicated PIDB and performs data transfers into the MP memory. Six bits per PIDB time slot are used for transferring pump data. With 32 PIDB time slots per frame, data is downloaded into the MP memory at a rate of 192 kbytes/second. Any subset of the 32 PIDB time slots may also be used for a pump, with the "E" bit of a time slot distinguishing used/unused time slots.

2.18 The BTSR receives pump data in the form of 2-Kbyte blocks. Each block of data is immediately preceded by a 16-byte header containing start code, block size, starting address and hash sum check (on the header) for that block.

2.19 The BTSR is a simplex entity that interfaces to the IMPU2 update bus, thereby gaining access to either MP. During the transfer of a block of data, the BTSR places the MP(s) being pumped into total direct memory access (DMA) hold and performs 16-bit word DMA transfers into the MP(s) memory. For the duration of the block, the BTSR also assumes maintenance of the MP sanity timer(s). The active MP is allowed to run between blocks of data.

2.20 The BTSR also provides a resident diagnostic to facilitate the early detection of hardware failures when in the nonpump state.

TIME SLOT INTERCHANGE UNIT (TSIU2)

2.21 The TSIU2 has five subfunctions: the time slot interchanger (TSI), the dual link interface (DLI), the data interface (DI), the signal processor (SP), and the control interface (CI).

2.22 The TSI is the time division switch. It contains two 512 by 512 time slot interchangers, one for data from the TMS to the peripheral units and one for data from the peripheral units to the TMS. The two 512 by 512 switches are connected such that time slots may be looped, thereby providing the capability to connect peripheral time slots (for intramodule calls). The TSI also provides a data port to the local digital service unit (LDSU).

2.23 The DLI is the interface to the NCT links. It recovers timing information from these links to provide timing for the IMPU2-TSIU2. The DLI contains the transmit and receive circuitry needed to interface to the optic links. It also provides the IMPU2 an interface to the message time slot on each NCT link.

2.24 The DI provides the data interface to peripheral units. It reformats time slot information and does a two-to-one concentration on peripheral time slots. Two DIs are connected to the TSI, each providing the TSI with 256 time slots per frame. Each DI provides 16 PIDBs for connection to peripheral units.

2.25 The SP does the hit timing and processing on the signaling and control bits (A-G) from peripheral time slots. It provides the MP access to these bits and provides a first-in/first-out (FIFO) type queue to report state changes of these bits. It also allows the MP to source these bits to the peripheral units.

2.26 The CI provides the interface between the MP and the various peripheral units for control information. Each CI provides 23 PICBs for these connections. The IMPU2 may be equipped with two CIs (per side) to provide a total of 46 PICBs.

A. Dual Link Interface (DLI)

2.27 The DLI functions are implemented on a single circuit pack code (TN877). The DLI provides the following functions for the TSIU2.

2.28 The DLI provides the interface to the NCT Links for the IMPU2-TSIU2. The DLI recovers clock and data from the incoming NCT links and distributes the resultant clocks and data to the TSIU2 and IMPU2. In the opposite direction, the DLI receives outgoing data from the TSIU2 and IMPU2, which is then multiplexed and sourced to outgoing NCT links. In each IM, two DLIs operate in a master/slave (active/standby) configuration.

2.29 The DLI consists of two link interface circuits (LIA,LIB), a clock circuit, and a control circuit. Each LI interfaces with one pair of NCT links (outgoing and incoming), which provides 256 time slots to and from the IM. Of these 256 time slots, 255 time slots are for voice and data paths to and from the TSIU2, with the remaining

time slot reserved for communications between the central processor and the IMPU2 (this time slot is the message time slot). The incoming 32.768 megabit/second data stream from the NCT links enters the receive (RCV) circuitry in the LI, where it passes through a clock recovery circuit that derives a 32.768-MHz clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the phase lock loop (PLL) in the clock circuit. The RCV circuit "frames up" on the incoming data stream via a pseudo-random sequence inserted into the data stream at the source end of the NCT links (the TMS in a multimodule office and the MICU in a single-module office). The incoming data stream is then converted to time slots and written into the BUFFER circuit (a RAM capable of containing one frame of data).

2.30 The TSI interface and message interface operate from clocks derived from the output of the PLL (these are the same clocks sent to the TSIU2 and IMPU2 by the DLI). When time slots are read from the BUFFER, parity is checked and regenerated. Normal voice and data time slots are sent to both TSIs via nibble buses operating at 8.192 megabits/second. The message time slot is sent to both the active and standby sides of the IMPU2 via serial data links to the synchronous data link controller (SDLC). These data links operate at 48 kilobits/second.

2.31 In the return direction, data is selected from one of the TSIs at the TSI interface, and from one side of the IMPU2 at the message interface for transmission to the TMS (or MICU in a single-module office), via the outgoing NCT link. These time slots are then multiplexed to provide a full frame of 256 time slots. In the transmit (XMIT) circuit, parity is checked and regenerated. The pseudo-random framing sequence, which is generated in the control circuit, is inserted (one framing bit per time slot). Finally, the time slots are converted to a 32.768-MHz data stream and transmitted over the outgoing NCT link.

2.32 The clock circuit selects a clock reference from one of the two LIs (master mode), or from the mate DLI (slave mode). This selected clock is used as a reference for the PLL, which in turn, provides a reference voltage to the voltage controlled crystal oscillator (VCXO). The output of the VCXO is a 32.768-MHz clock, which is divided by the clock circuit and distributed to the remainder of the DLI, the mate DLI, the TSI, and the IMPU2.

2.33 The control circuit provides control for the various functions performed by the LIs and clock circuit. Errors from these circuits are latched into error source registers (ESRs) that reside in the control circuit. These control registers and ESRs are accessible for writing and reading by either side of the IMPU2 via the IMPU2-DLI control interface. This interface is a 1.875 MHz serial data link. The data bits that make up the commands are clocked in by a clock that is provided by the IMPU2, and the command is executed on reception of a "go" signal received over a separate lead from the IMPU2. Parity over address and parity over data is checked in the control circuit. The control circuit provides a serial data link back to both sides of the IMPU2 for read operations, and an interrupt lead back to both sides of the IMPU2 to indicate that an error condition exists. Each bit of the ESRs can be inhibited from causing an interrupt via ESR mask registers.

2.34 The control circuit is contained in a custom NMOS device (328B). The clock circuit is implemented in SSI/MSI devices, along with the PLL and VCXO daughter boards that are used in the 5E1.2 version of the DLI (TN834 and

TN835). The circuitry that composes the RCV circuit and the portions of the TSI interface and message interface that send data to the TSI and IMPU is implemented in an LS1500 functional logic array (FLA), coded 374C. The XMIT circuits for both LIs and their corresponding portions of the TSI interface and message interface are implemented in one LS1500 FLA (374B). The DLI is contained on a single TN circuit pack (TN877). Each DLI is in a failure group separate from the rest of the IM and will be powered by a separate power converter (495FB). The power converters will interface to an SN412 control and display circuit pack.

B. Time Slot Interchanger (TSI)

2.35 The TSI consists of five circuit packs: TN865, TN127, TN887, TN315, and TN866. The primary data path of the TSI delivers 512 peripheral time slots from the DIs to the receive TSI RAM to be stored in consecutive order. Time slots are then translated from the receive RAM and can be delivered to both DLIs on any of the 512 network time slots. In the opposite direction, 512 network time slots from the DLIs are written consecutively into the transmit TSI RAM. Time slots are then translated from the transmit RAM on chosen peripheral time slots as instructed under software control and delivered to the DIs. Any peripheral time slot written into the receive TSI RAM can be read out onto multiple (up to all) network time slots toward the DLIs. The same fanout capability is provided by the transmit TSI RAM. A maximum delay in each direction of one frame (125 usec) can be introduced by the time slot interchange.

2.36 Two DIs are connected to the TSI. One DI is dedicated to even TSI time slots, and one is dedicated to odd TSI time slots. Each DI provides 256 time slots to the receive TSI RAM. The 16-bit time slots in nibble format are sent to the TSI by the DIs (PCM, A-G, and parity). The seven signaling and control bits, A-G, are transmitted with the PCM bits through the receive TSI RAM and are also sent to the SP.

2.37 The TSI transmits 16-bit time slots in nibble format to the DIs. Of the A-G bits sent to the DIs, the E-G bits are always sourced from the SP. The A, B, C, and D bits can be sourced either from the SP or passed through from the transmit TSI RAM. All PCM data sent to the DIs passes through the attenuation ROM. The attenuation ROM allows one of 32 values of digital loss to be inserted in the PCM data path on a per-time-slot basis. The loss values are 0dB through 15.5dB in .5dB increments. The integrity of the data path (TSI-to peripheral unit-to TSI) is protected by a walking parity scheme administered by the TSI, which inverts the parity sense of every ninth TSI time slot.

2.38 The TSI receives 512 time slots from the DLI via two 256 time slot nibble buses. The TSI selects which DLI (DLI0 or DLI1) is the source of time slots to the TSI.

2.39 The TSI transmits 512 time slots toward both DLIs in the TSIU2. The time slots consist of 16 bits in nibble format. The E bit of each time slot sent to the DLIs is set on a per-time-slot basis via a TSI control RAM written by the IMPU2. The A-D bits of each time slot sent toward the DLIs are either passed through from the receive TSI RAM or sourced from a TSI control RAM.

2.40 Two forms of connections are possible between the transmit and receive RAMs. The first connection allows intramodule paths to be set up by looping time slots on the DLI side of the TSI memories. A connection of this type will block an incoming time slot from the DLIs. The other connection allows intra-DLI connections to be made. A connection of this type will block an incoming peripheral time

slot from reaching the receive TSI RAM, but the blocked peripheral time slots will still have access to the SP and local DSU.

2.41 The alternate data RAM (ADR) provides the IMPU2 and local DSU with access to the contents of all 512 time slots. Via the ADR, the IMPU2 can write constants (e.g., idle code) to be sent to the DIs and DLIs and sample time slots at various points within the TSI. The ADR also provides IMPU2 access to the E bits received from the DLI. Parity errors on time slots received by the TSI from the DIs are reported to IMPU2 via the ADR. Data stored in the ADR (e.g., tones from the DSU) can be sent to the DIs, receive TSI RAM, or transmit TSI RAM. The TSI time slots written to the ADR can be sourced on a per-time-slot basis from four different locations in the TSI. This permits maintenance access and allows time slots from both DIs and DLIs to be sent to the local DSU.

C. Data Interface (DI)

2.42 The DI function has been reduced to a single TN circuit pack for the TSIU2. This reduction has been achieved by a custom bipolar LSI integrated circuit (358A). Two of these custom devices are used on the TN876 to realize the same function as the TN836/TN837 circuit packs. The operation of the new DI is identical to that of the previous design.

2.43 The DI interfaces the TSI to the various peripheral units that may be attached to the IM. In the incoming direction, it performs a multiplexing function by combining the time slot traffic of several peripheral units onto a single bus for the TSI; in the outgoing direction, it demultiplexes a single bus from the TSI to the various peripheral units.

2.44 The DI communicates with each peripheral unit over a peripheral interface data bus (PIDB). Each of these buses consists of four signals: serial data in, serial data out, a 4.096-MHz clock, and an 8-KHz sync. The data in and out operate at 4.096 megabits/second, carrying 32 time slots per frame, with 16 bits per time slot. Up to 16 PIDBs may be connected to the DI, with each PIDB carrying traffic to a service group in one of the peripheral units.

2.45 The DI passes data to and from the TSI over nibble buses. These buses operate at 8.192 megabits/second carrying 256 time slots per 125 usec frame (two DIs, each connecting 256 TSI time slots, are needed to carry traffic for the 512 time slot TSI). With 512 peripheral side time slots (16 PIDBs x 32 time slots) and 256 TSI side time slots, the DI can perform a two-to-one concentration function.

2.46 All PIDBs operate in synchronization; in the time of a single PIDB time slot, eight time slots are sent and received from the TSI. After a single time slot from all 16 PIDBs has been clocked into the DI, up to eight of those are chosen, via control information received from the TSI, to be inserted into the eight time slots to the TSI. The time slots not selected are blocked and lost. If less than eight are chosen, "1s" are sent on the nibble bus to the TSI in the time slots for which no PIDB time slot was connected.

2.47 In the outgoing direction, the TSI provides eight time slots to the DI during a single PIDB time slot period. These eight time slots are connected, again using control information received from the TSI, to eight of the 16 PIDBs. PIDBs not selected to receive TSI data transmit idle code to the peripheral units.

2.48 All eight TSI time slots need not be connected to a PIDB time slot. If less than eight are to be connected to PIDBs, the control information from the TSI associated with the "unused"

TSI time slots informs the DI to ignore that incoming time slot. All unselected PIDBs transmit idle code. In this case, more than eight will do so.

2.49 In addition to the nibble bus in and out of the DI from the TSI, the DI also receives from the TSI an 8.192-MHz clock, an 8-KHz sync pulse, four address leads, a board select lead, and two leads used for diagnostics. The 8.192-MHz clock provides all the timing for processes internal to the DI and also is used to generate the 4.096-MHz clock for the peripheral units. The 8-KHz sync pulse is used to synchronize properly the DI to the network and to generate the sync pulse to the peripheral units. The address leads indicate, on a per-time-slot basis, to which PIDB a given TSI time slot is to connect. The address is used by the DI both for the TSI-to-PIDB demultiplex function, and for the PIDB-to-TSI multiplex operation. The board select lead informs the DI, again on a per-time-slot basis, whether to connect the TSI time slot to the PIDB as determined by the address, or to ignore that time slot and make no connection to it. The diagnostic leads are used to loop data received from the TSI through the DI circuit and back to the TSI. These leads also provide the capability to have the DI loop idle code back to the TSI rather than the received TSI data. Maintenance of the DI, as well as the PIDB and parts of the peripheral units, is performed by the TSI via the walking parity scheme.

D. Control Interface (CI)

2.50 The CI function is contained on the UN71 circuit pack. The CI provides the control interface between the MP and the various peripheral units. This interface is used for control information to and from the IMPU.

2.51 The peripheral interface is a PICB. Up to 23 PICBs are available with each CI. Either one or two CIs may be equipped in the IMPU2 providing a maximum of 46 PICBs. Each PICB contains five twisted-wire pairs that carry clock, output data, input data, MP select information, and peripheral unit service requests.

2.52 The interface to the MP is via the IMPU2 subunit interface bus. This bus is a parallel 16-bit bidirectional data bus with a 6-bit address bus. The CI contains several registers that are accessible by the MP via this bus.

2.53 The CI performs four functions for the IMPU2:

1. Permits the MP to write 16 bits of information to a peripheral unit register (maximum of 256 destination registers).

2. Permits the MP to read 16 bits of information from a peripheral unit register (maximum of 256 source registers).

3. Receives, latches, and reports service requests from peripheral units.

4. Detects and reports CI operational errors.

2.54 The CI reads and writes peripheral registers via an exchange of serial messages over the PICB. A distribute operation writes 16 bits of data into a peripheral unit destination register. A scan operation reads 16 bits of data from a peripheral unit source register.

2.55 The MP will initiate all scan and distribute operations. In all scan and distribute operations, the peripheral unit will send a reply message back to the CI. In the reply message, there is a 3-bit ASW code. These bits are used to report errors

detected by the peripheral unit. If errors are detected during a scan or distribute order by either the CI or a peripheral unit, the error will be reported by latching a bit in the error source register. The interrupt lead to the MP will be asserted if an error occurs. The ability to inhibit this interrupt on a per-PICB basis is provided.

2.56 In addition to performing scan and distribute orders, the CI reports peripheral unit service requests by latching an active state on the PICB interrupt lead into the interrupt source registers. Inhibit registers (remote interrupt inhibit registers) are provided such that these service requests may be handled by interrupts or polling.

E. Signal Processor (SP)

2.57 The SP for the IMPU2 uses three circuit pack codes: TN212, TN213, TN214.

2.58 The SP performs hit timing on all signaling and control bits received from the TSI. This hit timing is performed by scanning the data at a 3-msec rate. A time slot is considered to have changed to a new state only if the bit persists in that state for two consecutive scans. This represents only a very low level of filtering. The MP will perform additional hit timing to filter false originations, split pulses, etc.

2.59 Hit timing is accomplished by comparing data in the input data buffer (IDB) with data contained in the last look RAM (LLR). The LLR contains the values of the signaling and control bits contained in the IDB during the previous 3-msec scan. Every 3-msec, all 512 time slots are read sequentially from the IDB and the LLR. Both 8-bit words are converted to serial and compared in an exclusive-OR circuit, bit by bit. If a bit has remained the same for two consecutive 3-msec scans, it passes the hit timing algorithm.

2.60 The state of all signaling and control bits received by the SP from the TSIU2 is stored after hit timing in an immediate access RAM (IAR). The IAR has the same data as the last report RAM (LRR). Through the IAR, the MP has access to the most recent hit timed state of all signaling and control bits of all time slots received by the TSI from the peripheral units.

2.61 The SP is capable of storing (in an MP-readable FIFO) all signaling and control bits whose state, after hit timing, has changed. The MP must specify on a per-time-slot basis which signaling and control bits of which time slot this change report is to be made. This allows the MP to ignore changes on certain bits of certain time slots.

2.62 State change calculations are based on the result of the hit timing circuit, the ignore RAM, and the LRR. The ignore RAM, set by the MP, indicates on which bits of which time slot state change reports should be made. The LRR contains the previously calculated states of all signaling and control bits after hit timing. If a new time slot bit has passed the hit timing algorithm (i.e., has not changed during the last 3 msec), it is compared to the state stored in the LRR. If a change has occurred, the LRR is updated. If the bit being processed is not set to ignore in the ignore RAM and there is a change from the state contained in the LRR, the new bit value is written into the report FIFO. All changes for one time slot are collected before the FIFO is written. The FIFO is readable by the MP.

2.63 The signaling and control bits (A, B, C, D, E, F, and G) are transmitted to the TSIU2 for all 512 peripheral side time slots every 125 usec. These signaling bits are

read from a 512 time slot RAM designated as the M-RAM. The M-RAM is both writable and readable by the MP.

LOCAL DIGITAL SERVICE UNIT (LDSU)

2.64 The LDSU is a peripheral that provides the heavily used functions of tone generation and tone decoding. The local DSU provides the tone recognition functions required by 5ESS call processing. The following tone types must be recognized by the DSU:

(a) TOUCH-TONE* signals (16 tone pairs)

(b) Multifrequency signals (15 tone pairs)

2.65 The DSU must be capable of generating the following tones required by the 5ESS Switch:

(a) Call progress tones

- audible ring
- dial tone
- high tone
- low tone
- call waiting
- receiver off-hook (ROH)

(b) Multifrequency signals (15 tone pairs), TOUCH-TONE signals (16 tone pairs), and CCIS continuity check tones (1780 and 2010 Hz).

2.66 Each IM is equipped with a single LDSU, and that LDSU is dedicated, providing tone generation and tone decoding only for lines and trunks terminating on that IM. Tone generation and tone decoding are segregated from the rest of the DSU functions in the global digital service unit (GDSU). Distributing these functions to each module, rather than providing them in a centralized pool shared by all modules, greatly reduces the amount of intermodule message traffic, since these services are heavily used in call processing.

2.67 The LDSU is connected to the LDSUB and PICB and receives time slot data from the alternate data RAM in the TSI. Access to the LDSU is gained by creating TSI paths from peripheral side time slots into the alternate data RAM. The 64 time slots used by the LDSU are not part of the 512 TSI time slots, and thus the appearance of an LDSU on each IM does not reduce the switching capacity of the TSI.

FAN UNIT

2.68 The fan unit provides air flow for maintaining correct operating temperatures.

2.69 Three separate fans are used in the fan unit. Only two are required to provide sufficient air flow, thereby ensuring that correct operating temperatures are maintained in the event of a fan failure.

2.70 Circuitry to detect and report a fan failure to the IMPU2 is provided. A fan failure alarm can be retired manually, or under software control.

FUSE/FILTER UNIT

2.71 The fuse panel normal input is -48 volts, with the return (RTN) isolated from frame ground in the equipment frame. Each fuse panel has four circuits that are fed from a 20-ampere fuse in the power

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distributing cabinet, or from the power plant. by way of the filter panel. Each of the four circuits feeds 12 load-fuse positions, for a total of 48 available load fuses. The first two circuits are fed from the A or 0 bus, and the other two circuits are fed from the B or 1 bus. Alarms that are generated when a fuse operates are sent to the plug-in circuit pack (ED-5D521-30,G1) where they are combined to illuminate a light-emitting diode for the appropriate bus (0 or 1), and to send from the fuse panel an electrical signal to indicate the bus with the fuse operated.

2.72 The physical construction of the fuse panel consists of a duplicated pattern, whereby the panel 0 side and 1 side consist of three 24 D fuse blocks, an alarm collection circuit pack, a connecting terminal strip, and a bracket providing a light-emitting diode for alarm indication. Each side is fed by a pair of power feeders, with each feeder powering 12 fuse positions. This arrangement provides 24 load fuses for the 0 bus and 24 for the 1 bus for a total of 48 load-fuse positions per cabinet. An auxiliary fuse panel can be added to the existing fuse panel to provide four additional fuses for each feeder. With this addition, the combined total fuse capacity is 16 load fuses per feeder or 64 load fuses per cabinet.

ALARMS

2.73 Alarms receive special treatment because, in some cases, the circuit used requires the use of more than one alarm per feeder from the power distribution plant. Therefore, on each feeder of the 12 load positions provided, eight have one alarm signal, and the other four have a separate alarm signal. If these separate alarms are required, they can be obtained through proper selection of lead-fuse assignments. The separate alarms are then available through selection of the corresponding alarm terminal numbers of the alarm circuit pack. If separate alarms are not required, the alarm terminals at the alarm circuit pack can be connected together, as required.

3. INTERFACES

EXTERNAL INTERFACES

A. Peripheral Interface Control Bus (PICB)

3.01 A PICB consists of 5-wire pairs that are used for balance data transmission and signaling. The clock pair carries a 2.048-MHz gated clock signal to the peripheral units; the data out pair carries serial information to the peripheral units from the CI; the data in pair carries serial data from the peripheral units to the CI; the select lead carries signaling information that is used to select the active side CI; the interrupt pair transmits service requests from the peripheral units.

3.02 The cable length of the PICB may vary but has a maximum limit of 20 feet.

3.03 Data is to be gated in and out of the peripheral unit on the negative edge of the clock. The reply must be received by the CI within 21.5 usecs from the first clock pulse to avoid a timeout error.

B. Peripheral Interface Data Bus (PIDB)

3.04 A PIDB provides the physical link for traffic between the DI of the IM and any peripheral unit connecting to the DI. It consists of four balanced, differentially-driven, RS422 compatible twisted-wire pairs.

3.05 The PIDB carries 4.096 megabit/second serial data from the DI to the peripheral units, a 4.096-MHz clock and 8-KHz sync to the peripheral units, and

4.096-megabit/second serial data to the DI from the peripheral units. The twisted pair carrying data from the periphery is terminated at the DI. The PICB cable may vary in length but has a maximum limit of 20 feet.

3.06 The 4.096-MHz clock has a 244 ns period. The low or high portion of the 4.096-MHz clock may change +20 ns for a single cycle at any time due to a DLI clock reference switch at the TSI. The duty cycle of the clock, excluding this +20 ns is 50 percent. The 8-KHz sync is a normally high signal ("1" state) that pulses low for one 4.096-MHz clock period every 125 us. If the clock switch occurs during the 8-MHz sync pulse, the duration of the pulse may also change a +20 ns.

3.07 The peripheral units should clock PIDB data in from the DI on the falling edge of the 4.096-MHz clock data out onto the PIDB on the rising edge of that clock.

3.08 During the sync pulse, the peripheral should clock PIDB time slot No. 29, bit seven in from the PIDB on the negative edge of the 4.096-MHz clock, and clock out PIDB time slot No. 31, bit 15 onto the PIDB using the positive edge of the clock. Note the 2-1/2 time slot skew between incoming and outgoing information; this is due to the skew required by the TSI and DI to perform their functions.

3.09 A peripheral unit service group will receive a PIDB from each side of the duplex TSIU2. In a fully operational IM, data will flow over both PIDBs. Using control information received from the IMPU2 via the CI, the peripheral unit will select only one PIDB from which to receive information. However, it will transmit the same data back over both PIDBs. The skew of the two PIDB clocks received from the duplex IM can be up to +80 ns.

C. NCT Links

3.10 The NCT links receive and transmit the serial data at a 32.768-MHz rate. The DLI will track the received serial data up to +1 KHz of the nominal frequency (±32 ppm). Each frame consists of 256 16-bit time slots. Bits zero through seven are PCM data bits in the 255 voice and data time slots. Bits A through E are signaling bits. The G bit is the bit position into which the pseudo-random framing sequence is inserted. The F bit is toggled at the beginning of each frame and is used for fault detection in the DLI/TMS interface (in a multimodule office), or the DLI/IMPU2 interface (in a single-module office). The P bit is such that the 16 bits of the time slot have odd parity. In the message time slot, bits zero through five are the data bits that contain data to/from the IMPU2, and bit seven is the central processor intervention (CPI) bit.

D. Alarm Interface

3.11 The alarm interface is divided into two failure groups, side 0 and side 1. The alarm input lead monitors the 70-type indicator fuses used in the fuse block. If a fuse is blown here, -48 volts is connected to the Z scan point alarm input, located in the TSIU2, and causes the scan point to be activated. The Z scan point monitors a group of fuses that protects power to the peripheral units.

E. Power Input

3.12 The power input to the frame is -48 volts, with the return (RTN) isolated from frame ground in the equipment cabinet. Each fuse/filter panel has two circuits that are fed from a 20-amp fuse in the power distributing cabinet or from the power plant.

INTERNAL INTERFACES

A. DLI to Controller Bus

3.13 The DLI to controller bus contains two interfaces between the DLI and IMPU2, the message interface and control interface. The message interface sends and receives message time slot data to/from the IMPU2. The control interface receives control data from the IMPU2 to set the modes of operation in the DLI. It also sends the status of the DLI registers back to the IMPU2.

3.14 After the message time slot has been extracted from the normal data path through the LI, parity is checked and generated over the six bits that will be sent over the 48-KHz data links to the SDLCs in both sides of the IMPU2. The generated parity is also sent to the SDLCs in both sides of the IMPU2 over separate data leads. At the same time, the CPI bit is sent to the CPI gate arrays in both sides of the IMPU2. Two clocks are sent to both sides of the IMPU2 from the clock circuit in the DLI. These clocks are used by the IMPU2 to clock the received message time slot data and parity into the SDLCs. In the return direction, the IMPU2 uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each LI contains a message interface to and from both sides of the duplex IMPU2.

3.15 The IMPU2-DLI control interface is composed of three signal leads, a clock lead from each side of the IMPU2 to the DLI, and two signal leads from the DLI to each side of the IMPU2. A control lead originates from each side of the IMPU2 to indicate which side is sending commands to the DLI. Another control lead comes from each IMPU2 side to control when a read or write command is executed by the DLI. A 1.875-MHz clock is sent by each IMPU2 side, along with the data, which specifies the command to be executed. The entire write operation is specified in a serial 16-bit command in which the first eight bits contain the data to be written, followed by a spare bit and a parity bit for the eight bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four bits that specify the register to be written. During a read operation, only six bits are sent by the IMPU2 to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits that determine the register to be read. Following the execution of the read command as initiated by the MPGO signal, eight bits of data, plus one parity bit (parity over the data) are sent back to both sides of the IMPU2 on separate signal leads with the results of the read operation. Interrupt leads that indicate error conditions exist in the ESRs of the DLI are also a part of the IMPU2-DLI control interface. These signals are asynchronous to the IMPU2 and have no specified timing relationship.

B. IMPU2 to LDSU

3.16 The LDSU communicates control information to/from the IMPU2 via a PICB. Each service group provides a duplex PICB interface to the duplicated IMPU2. A duplex-to-simplex conversion is performed at the interface by decoding a select lead on each bus, so the LDSU listens to the active side only of the IMPU2. Reply messages are sent to both IMPU2 halves. However, the interrupt signal sent to the IMPU2 is sent only to the active IMPU2 half.

C. TSIU2 to LDSU

3.17 The TSIU2 communicates to the LDSU over two dedicated serial ports connected to the TSI. The TSI transmits and receives 32 serial time slots to and from each of two service groups in the LDSU. Any of these 64 time slots can be selected as a source of PCM data for any time slot

going to the DLIs or DIs. Similarly, the TSI can send the 16-bit word of any time slot received from the DLIs or DIs out on any of the 64 time slots to the LDSU. The data format and timing of the LDSU interface is of the PIDB type consisting of four balanced, differentially-driven, RS-422 compatible twisted-pair wires. Signals are provided by pulse out, 32 time slot serial output data, and 32 time slot serial input data.

3.18 The twisted pairs carrying data from the LDSU to the TSI are terminated with a discrete resistor providing a differential mode termination of 220 ohms and a common mode termination of 55 ohms. The 8-KHz sync pulse is normally "high", and goes "low" for one clock period (244 nsec) every frame (125 usec). The clock period can change +20 nsec for one period during a DLI clock reference switch by the TSI. Both data and sync (if sync is coincident) will reflect the period change of the clock switch.

3.19 In a normally functioning IM, each service group in the LDSU will receive two of the PIDB-like interfaces described above, one from each side of the duplex TSI, with only one active at any given time. Identical data will be present on both buses to a given service group.

D. IMPU2 Subunit Interface Bus

3.20 The IMPU2 subunit interface bus is used as the control interface to the TSI, SP, and CI from the IMPU2. It uses a 16-bit bidirectional data bus and a 6-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two parity leads (bidirectional also), one each for the low byte and high byte of data. The parity is computed such that the sum of bits set to a logic one in each byte (including the parity bit) is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

3.21 There are five control leads to each subunit. Two of these, the read and write signals, are shared by all subunits. These two signals are used to distinguish between read and write operations to a subunit and are used by the selected subunit to gate the data to/from the data bus. The other three controls are board select, ready, and interrupt. Each individual subunit has separate board select, ready, and interrupt leads. The ready lead is used by the subunit to extend the IMPU2 bus cycle for subunits with slower response time, and the interrupt lead is used by the subunit interrupt in the IMPU2.

3.22 In addition, the CIs receive a lead called NAE that is used to force the select wire pair in the PICB on the nonactive side to a nonconductive state.

E. Alarms

3.23 The alarms are divided into four failure groups: DLI side 0, DLI side 1, controller side 0, and controller side 1. The DLI alarm consists of a signal from the fuse block for monitoring blown fuses. The alarm input lead monitors the 70-type indicator fuses used in the fuse block. When a fuse is blown, the fuse connects -48 volts to the alarm input lead on the control and display pack in the TSIU2. This lead lights the alarm LED on the control and display pack and activates the Y scan point.

3.24 The controller alarm interface has the same alarm connection as the DLI alarm interface, plus the addition of a Z scan point monitor. The Z scan point monitors a group of fuses that protects power to the peripheral units. If a fuse is blown here, the Z scan point on the control and display pack is activated.

F. BTSR Peripheral Interface Data Bus

3.25 The BTSR PIDB interface provides the data path to the BTSR for fast pump. A PIDB consists of four differentially-driven signals used for data transfer. The data out and data in signals are used for data transmission of data between the BTSR and the DI. A 4.096-MHz clock is provided for clocking data into/out of the BTSR. Data is clocked into the BTSR on the falling edge of clock. Data is clocked out of the BTSR on the rising edge of clock. A PIDB frame consists of 32 16-bit timeslots. The BTSR provides a 28.5 time slot skew between data in and data out to meet TSIU2 requirements. The 8-KHz synchronization signal is used for synchronizing the BTSR with the DI.

G. Memory Data, Address, and Control

3.26 This bus connects all additional memory circuit packs, which are located in a separate shelf, to the MP's dynamic memory controller (TN875). It consists of the following:

1. Forty bidirectional data leads, composed of 32 data bits (four bytes) plus eight bits of hamming and parity.

2. Twenty bidirectional address lines plus two parity leads. There are 8-row address leads, 8-column address leads, a row parity and column parity lead, and four array selects to select a 64K array.

3. Fourteen memory control signals used to select memory boards, initiate memory cycles, control memory data bus direction, indicate refresh operations, strobe data into memory, and provide upward compatibility with future memory board designs.

H. Controller Power

3.27 All controller power converters are connected to the fuse block via a hot lead -48 volt and a ground potential lead 48RTN.

I. Fan Alarm

3.28 A fan failure is reported to the MP via a scan point from the fan unit. A fan alarm can be retired by the MP using a distribute point to the fan unit.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

VOLTAGES

1. -48 volts +4.5 -6.25 volts

AMBIENT TEMPERATURE

1. 0° to 70° centigrade (at circuit pack)

2. 0° to 50° centigrade (office aisle ambient)

2. FUNCTIONS

2.01 The function of this unit is described in Section 1 of this Circuit Description.

3. CONNECTING CIRCUITS

LINE TRUNK PERIPHERAL CABINET SD5D113-01

MESSAGE SWITCH CABINET SD5D116-01

TIME MULTIPLEXED SWITCH CABINET SD5D117-01

POWER DISTRIBUTION PANEL SD82518-02

(a) Circuit Description, Fuse/Filter Panel - SD-5D053-01

(b) Circuit Description, Interface Module Control Cabinet - SD-5D118-02

(c) Circuit Description, Digital Service Unit - SD-5D035-01

(d) Circuit Description, Time-Slot Interchanger Unit - SD-5D041-01

(e) Circuit Description, Interface Module Processor Unit - SD-5D040-02

(f) Circuit Description, Fan Unit - SD-5D019-01

4. LIST OF ACRONYMS

ADR	alternate data RAM
ASW	all seems well
BTSR	bootstrapper
CI	control interface
CP	central processor
CPI	central processor intervention
DI	data interface
DLI	dual link interface
DMA	direct memory access
DSCU	digital service circuit unit
DSU	digital support unit
EPROM	erasible programmable read-only memory
ESR	error source register
FFU	fuse/filter unit
FIFO	first in, first out
FLA	functional logic array
FU	fan unit
GDSU	global digital service unit
IAR	intermediate access RAM
IDB	input data buffer
IM	interface module
IMC	interface module control
IMPU	interface module processor unit
LDSU	local digital service unit
LDSUB	local digital service unit bus
LI	link interface
LLR	last look RAM
LRR	last report RAM
LSI	large scale integration
MICU	message interface & clock unit
MP	module processor
MPF	mate power fail
MSGS	message switch
NCT	network control and timing
NMOS	N-channel metal oxide semi-conductor
OOS	out of service
PCM	pulse code modulation
PICB	peripheral interface control bus
PIDB	peripheral interface data bus
PLL	phase lock loop
RAM	random access memory
RCV	receive
ROH	receiver off hook
RTN	return
SDLC	synchronous data link controller
SP	signal processor
SSI/MSI	small/medium scale integration
TMS	time multiplex switch
TSI	time slot interchange
TSIU	time slot interchange unit
VCXO	voltage-controlled crystal oscillator
XMIT	transmit

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