5ESS® SWITCHING EQUIPMENT
SWITCHING MODULE PROCESSOR UNIT, MODEL 2
CIRCUIT

B. Changes in Apparatus

The following changes are documented for International features:

1. The SMP12 Split Memory wiring option with added 8Mbyte memory pack TN1409 in a SMPU2 with out MEU.
2. The SMP23 with additional Split Memory wiring option.
3. The SMP23 to SMP23X wiring option with added TN1408B, TN1416, TN1417 and TN1418 in a SMPU2 with MEU.
4. The SMP12 to SMP23X wiring option with added TN1407[B], TN1408B, TN1416, TN1417, TN1418 and the memory packs TN1409 and TN1419 in a SMPU2 with out MEU.

D. Description of Change

1. Change B.1 transmits wiring information to add three 4Mbyte board selects to the three memory slots which are reserved for the TN1409. The TN1409 is used in emulate mode as 2x TN2012. This change increases the memory of the SMP12 unit with the TN1527 memory controller from 20Mbyte to 32Mbyte with 2x TN2012 and 3x TN1409.
2. Change B.2 transmits additional SMP23 wiring information to add address lead A22I1 and 8MB0 board indicator for the TN1409. This TN1409 memory pack is used in normal addressing mode using the MEU in Split Memory configuration. The address leads A02I1 and A02I0 are reused by the TN1408 for A22I1 and 8MB0, respectively, due to a lack of spare pins on the TN1408. This change increases the memory of the SMP23 unit with the TN1408 memory controller from 16Mbyte to 32Mbyte with 8x TN56 and 2x TN1409 using the Memory Expansion Unit (MEU).
3. Change B.3 transmits wiring information to add the SMP23X unit identifier, system address SA25 and update address UA25 and UA26 (UA26 is added for future growth). Boards to be used are the upgraded TN1408B memory controller, TN1416 core support and the new circuit packs TN1417 RAM/ROM, TN1418 fast pump bootstrapper and TN1419 16Mbyte memory pack. The TN1419 is used in emulate mode as 2x TN1409. This change increase the memory of the SMP23X unit from 32Mbyte to 64Mbyte with 8x TN56, 2x TN1409 and 2x TN1419 using the Memory Expansion Unit (MEU).
4. Change B.4 transmits information to convert SMP12 with Split Memory to a SMP23X in a SMPU2 with out MEU. The wiring information to be added is:
   1. CACHE0 and rewire STKERR0 and A02I0.
   2. The address lead A22I1 and 8MB0 board indicator for the TN1409/TN1419.
   3. The SMP23X unit identifier, system address SA25 and update address UA25 and UA26 (UA26 is added for future growth).

   Boards to be used are the upgraded TN1408B memory controller, TN1416 core support and the new

circuit packs TN1417 RAM/ROM, TN1418 fast pump bootstrapper and TN1419 16Mbyte memory pack. The TN1419 is used in emulate mode as 2x TN1409. Note that the added 4Mbyte board selects of change D.1 are reused as 8Mbyte board selects for the TN1419 because the TN1408B will drive all the board select leads as an 8Mbyte one in this SMP23X memory configuration. This change increases the memory of the SMP23X unit from 32Mbyte to 64Mbyte with 2x TN1409 and 3x TN1419.

F. Changes in CD Sections

1. Add sections to table of contents on page 1:
   TN1407 - PROCESSOR CORE BOARD
   TN1408B - MEMORY CONTROLLER BOARD
   TN1416 - CORE SUPPORT
   TN1417 - RAM/ROM
   TN1418 - FAST PUMP BOOTSTRAPPER
   TN1409 - 8 MBYTE DYNAMIC MEMORY
   TN1419 - 16 MBYTE DYNAMIC MEMORY

2. Add in paragraph 2.14
   TN1407 - PROCESSOR CORE BOARD

   All references to TN1407 should read TN1407/TN1407B
   Note: the TN1407B functionality is the same as for the TN1407, except the hardware device changes of the external cache.

3. Add after paragraph 2.21
   TN1408B - MEMORY CONTROLLER BOARD

   This circuit pack provides all the functions of the TN1527 but provides the memory interface between the memory packs (TN56, TN2012, TN1409 and TN1419) and the core board (TN1407 or TN1407B) in the SMP23X option. This pack also provides the Split Memory feature with two or three types of memory packs located in fixed slots per SMPU2 or SMPU2 with MEU memory configuration, respectively. The maximum memory address capability is 64Mbyte. The Memory Auxiliary Register provides the SMP23X unit identifier bit.

4. Add after paragraph 2.16
   TN1416 - CORE SUPPORT

   This upgraded circuit pack provides all the functions of the TN1533 but provides the implementation of address bit SA25 to address 64Mbyte of dynamic memory. Also SA25 is included for the parity check/generate function in the system low address byte.

5. Add after paragraph 2.19
   TN1417 - RAM/ROM

   The TN1417 is an enhanced version of the TN874B RAM/ROM board with new functionality. The write protect address range is extended to 128Mbyte, protectable in 1Kbyte blocks for the address range 0 - 16Mbyte and 32 - 128Mbyte, and 4Kbyte blocks for the address range 16 - 32Mbyte. The stack protect function is removed from the TN1417 because the TN1407 provides the overlaying user stack memory with static RAM. An ID register and Unit register is added to control the identification of the circuit pack and unit, respectively.
   A future improvement of the TN1417 is the addition of registers to control the MCCP (Memory Card Circuit Pack) with PCMCIA interface for one FLASH memory card.

6. Add after paragraph 2.30
   TN1418 - FAST PUMP BOOTSTRAPPER

   The TN1418 is an enhanced version of the TN878 Fast Pump Bootstrapper with improved

functionality and the capability to address 64Mbyte of system memory. For future memory growth the address capability is already extended to 128Mbyte. Although the TN1418 is designed with new functions and firmware, the TN1418 is still downwards compatible with the TN878.
Improvements are e.g. the handling of the top-byte of the header start address, the on-board pump data buffering, block transfer of the buffered pump data blocks to the system memory to reduce the update bus seizure time and the implementation of a PCMCIA interface for two FLASH memory cards for future applications.
All the on-board functions, e.g. hardware/firmware update from FLASH card, are under firmware control and a command message structure is used between the SMP and the bootstrapper. Note that these messages are only used to provide new function to the SMP but none of these functions are yet provided in SM software.

7. Add after paragraph 2.24
TN1409 - 8 MBYTE DYNAMIC MEMORY

This memory pack is used in the SMP12 and SMP23[X] unit with Split Memory option. It provides 8Mbyte of Dynamic Memory with 80x 1Mbit DRAM chips. When selected the memory array permits memory read/write accesses or refresh cycles. A selected array returns 32 bit data, 8 bit parity/hamming code and a generated row/column address parity bit.
Besides the normal addressing mode the TN1409 is capable to emulate 2x TN2012 or 4x TN56.

8. Add after paragraph 2.24
TN1419 - 16 MBYTE DYNAMIC MEMORY

This memory pack is used in the SMP23X unit with Split Memory option. It provides 16Mbyte of Dynamic Memory with 40x 4Mbit DRAM chips. When selected the memory array permits memory read/write accesses or refresh cycles. A selected array returns 32 bit data, 8 bit parity/hamming code and a generated row/column address parity bit.
Besides the normal addressing mode the TN1419 is capable to emulate 2x TN1409 or 4x TN2012.

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SWITCHING MODULE PROCESSOR UNIT, MODEL 2
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 This change adds the TN1407, TN1408, and wiring options to the features and options table to provide the SMP23 feature.

D. Description of Change

D.1 This change transmits information for the SMP23 feature for the Switching Module Processor Unit, Model 2. This change increases the memory of the SMP unit from 16Mbytes to 32Mbytes using the memory expansion unit (MEU).

F. Changes in CD Sections

F.1 Added TN1407 - PROCESSOR CORE BOARD and TN1408 - DYNAMIC MEMORY CONTROLLER sections to table of contents page.

F.2 Add after paragraph 2.14, TN1407 - PROCESSOR CORE BOARD.

This core board is used for the SMP23 option, it provides 128K of text cache directly mapped, uses the MC68020 microprocessor, runs at 10MHz (system clock), and provides 512Kbytes of static RAM overlaying user stack memory.

F.3 Add after paragraph 2.21, TN1408 MEMORY CONTROLLER BOARD.

This pack provides all the functions of the TN1527, but provides the memory interface between the memory packs (TN56, TN2012) and the core board (TN1407) in the SMP23 option. This pack also provides a feature in International for Split Memory with additional wiring changes. Split Memory feature allows the use of a TN1409 (8Mbytes board) to increase the SMP unit to 32 Mbytes without the memory expansion unit.

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SWITCHING MODULE PROCESSOR UNIT, MODEL 2
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added wiring option "YD" (Note 316).

D. Description of Change

D.1 A wiring option was added to reroute the 1GOIA1 net away from the system data bus leads.

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5ESS® SWITCHING EQUIPMENT
SWITCHING MODULE PROCESSOR UNIT, MODEL 2
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added
Option "YD", FS1,2 - APP FIG. 2

B.2 Superseded	Superseded by
Option "ZR", FS1,2	Option "YD", FS1,2

D. Description of Change

D.1 This change adds firmware option "YD" (MC5X265A1B) and rerates firmware option "ZR" (MC5X261A1B) Discontinued Availability (D.A.).

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5ESS™ SWITCHING EQUIPMENT
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CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The interface module processor unit, model 2 (IMPU2) provides the operating environment for the software and the interfaces to various subunits in the 5ESS switch.

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* This CD covers drawing issues through 16M.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The IMPU2 provides the intelligence for the interface module (IM). There are two module processors (MP) within the IMPU2 operating in a duplex configuration, such that either MP can singly perform the IMPU2 functions.

2.02 The module processor (MP) is able to operate in each of the following states: active, standby, or out of service (OOS). In the active state, the MP is performing call processing, executing code, and controlling the dual link interfaces (DLI) and the interface units. In the standby state, the MP is not executing code, but allows the active MP access to its internal buses. In the OOS state, the MP is able to execute code but can not access the DLI.

2.03 The normal MPs operating mode is one MP active and the other MP standby. Active means the A flip-flop is set and executing code. Circuitry is provided to insure that neither a standby or OOS MP can access a DLI.

2.04 Under normal (no faults) operating conditions, the active MP keeps all data areas in the standby controller up to date, such that the standby MP can, at any time be made active. Should a fault occur in the active MP, the standby MP is made active, and the active MP made OOS. Such a forced switch can be performed without mishandling calls. It is also possible to perform a controlled switch of the active/standby states of the MPs without resulting in mishandled calls.

2.05 The IMPU2 contains a fast-pump capability used for initialization of the MP memory. The bootstrapper (BTSR) provides the interface between the fast-pump data link and the MP. The BTSR receives serial data from a dedicated peripheral interface data bus (PIDB) and performs data transfers into the MP memory.

SECTION II - DETAILED DESCRIPTION

1. FUNCTIONAL DESIGNATIONS

1.01 The single shelf interface module processor unit has two subfunctions: the module processor (MP) and the bootstrapper (BTSR).

1.02 The MP provides the intelligence for the IM. There are two MPs within the IMPU2 operating in a duplex configuration, such that either MP can singly perform the IMPU2 functions.

1.03 The BTSR provides the interface between the fast-pump data link and the MP. The BTSR receives serial data from a dedicated peripheral interface data bus (PIDB) and performs data transfers into the MP memory.

2. FUNCTIONS

MODULE PROCESSOR - FS 1, 2, 3, 4

2.01 The module processor function in the IMPU2 is realized using five circuit packs plus memory. The initial circuit packs were TN871, TN872, TN873, TN874, TN875, and TN28 memory planes. With the additions of features and improvements most of the initial circuit packs have evolved into new codes as shown below:

```
TN871------> TN871B
TN872
TN873
TN874------> TN874B
TN875------> TN875B------->TN875C
TN28-------> TN56-------->TN2012
```

Using the above module processor packs and the TN56 memory planes a maximum of 16Mbytes of memory may be addressed. However, the need for more memory prompted the introduction of the TN2012 memory plane and three new circuit pack codes. Using TN2012 memory planes, the 1MPU2 shelf may be equipped with a maximum of 20Mbytes of memory. In

order to address memory past 16Mbytes the following circuit packs are needed: TN1397 in place of TN871B, TN1533 in place of TN873, TN1527 in place of TN875C. With the use of a Memory Expansion Unit (MEU) the IMPU2 may be equipped with a maximum of 32Mbytes of memory. A circuit pack that was derived from the TN872 is the TN1617. This circuit pack is basically a modified TN872 and its initial application is 5E4(2) full.

2.02 The normal operating mode of the MPs is active/standby. In this mode, one of the processors is actively executing code, called the running state. In addition, the processor is called active if its A flip flop is set. The other MP is in the standby state, and is dormant. While dormant, the internal busses of the MP can be controlled by the mate[2] allowing it read and write access to the dormant MP. Whenever a MP becomes dormant, it releases control of its internal busses to its mate. This operating mode permits the running MP to keep an up to date copy of its memory in the dormant MP.

2.03 The MP can operate in the following hardware states:

(a) Running as previously described, the microprocessor is actively controlling its internal busses. While running, the mate is unable to gain access to this microprocessor's busses.

(b) When dormant, the microprocessor is in a DMA hold condition, granting the mate access to all the internal busses.

(c) The DMA transfer mode allows the DMA unit to transfer data bytes to/from the message time slot links. The DMA unit controls the internal busses. If the update mode is enabled the data writes also occur in the mate.

2.04 Active and standby are software states, distinct from the hardware states. An active MP must be running and have access to the DLIs. A standby MP is dormant with its mate active and keeping its memory up to date.

2.05 Three types of memory are provided in the MP: 128K EPROM, 8K of static RAM, and dynamic RAM used for the operational programs and data. The EPROM provides program storage for power up initialization and fault recovery. The static RAM provides data storage independent of the dynamic RAM. This is an important feature when exercising the dynamic memory system. 8K of address space is reserved for I/O access via memory reference instructions.

2.06 The dynamic memory system may use TN28, TN56 or TN2012 memory planes. Each of these memory planes is 1024K bytes 2048K bytes and 4096K bytes respectively. Detection and correction of single bit memory errors and detection of double bit errors are provided by hamming parity across all of the memory. Memory word size is 40 bits, which includes 4 bytes of data, parity over each byte, and 4 bits of hamming. The mapping to the microprocessor's 16-bit word size is accomplished on the memory controller pack.

2.07 A write protection capability is provided on the MP memory. Each 1K byte of data memory is protectable. Each 4K block of text memory is also protectable. All of the text can be protected with a single bit. Any attempts by software to write into a write protected area results in a reset

---

2. Mate refers to the other MP in the IMPU2.

(nonmaskable interrupt) being applied to the MP and the write being blocked. The selection of whether a particular 1K byte data block or a 4K byte text block of memory is write protected is made under software control. Additionally a mechanism for implementing stack protection is available. When activated, the memory region from 0x80000 to 0x100000 becomes write protected, except for a 2K block assigned to the currently running process. Stacks are available in 2K bytes only, allowing a total of 256 separate stacks.

2.08 To allow efficient control of and response to asynchronous events, 25 interrupts are provided in the MP. Twenty-four of the interrupts are presented to the MP as level 4 interrupts. Errors from the subunits, error reporting and message completion from the data link controllers, time intervals, status changes and errors are all presented to the microprocessor as interrupts. Two types of level 4 interrupts are provided: A high priority set of interrupts for reporting errors from the subunits, and a low priority set for all other interrupts which is disabled during the I/O time interval. The twenty-fifth interrupt arrives at the MP as a level 5 (higher priority) interrupt. This interrupt is generated by the central processor intervention (CPI) gate array and is used to indicate a time multiplex switch (TMS) switch.

2.09 Each MP possesses a sanity timer, reset under software control. Failure to reset the timer or resetting the timer too often results in a reset (nonmaskable interrupt) being applied to the MP. The active MP resets the timer in the standby MP. A timeout of the sanity timer in the standby MP results in the standby MP leaving the standby state and under software control, entering the OOS or active state. The minimum interval requirement is disabled in the off line side.

The MP receives two message timeslots from each DLI. The MP can select any two of these timeslots for message communication with the message switch (MSGS). Messages over these message time slots adhere to the BX.25 communication protocol. Communication with the central processor (CP) is all under DMA control in the MP.

2.10 A central processor intervention (CPI) path to each MP is provided to be used as a hardwired path to force an IM into a known state from the CP. The MP has a minimum of control over the path of the CPI message and no control over the designated action taking place. The seven possible CPI actions are:

(a) Forced side 0 of the MP active, also forces side 1 inactive.

(b) Force side 1 of the MP active, also forces side 0 inactive.

(c) Clear the force active set by one of the above CPI functions.

(d) Force a reset to the MP(s).

(e) Disable the sanity timers in both MPs.

(f) Enable the sanity timers in both MPs.

(g) Level 5 interrupt to MP indicating a TMS switch.

2.11 A mate power fail (MPF) detection capability is provided to prevent the active MP from mutilating the mate's memory, when the active MP substains a power failure. The circuitry prevents an MP which has lost power from writing the mate and forces the mate active.

2.12 A 32 bit counter is used for a stable billing clock. Either DLI 0 or DLI 1 can drive the 32 bit counter, with an enable bit provided for each DLI clock. A software strobe

point, used for diagnostics, can advance the counter at a software rate, if the two clocks are disabled.

TN871 - PROCESSOR CORE BOARD

2.13 The TN871/TN871B board provides the following functions for the MP:

(a) A Motorola 68000 microprocessor with associated clock generator, local bus controller, status generator, ready logic, and interrupt interface. The microprocessor utilizes a 9 MHz clock. The microprocessor utilizes a 9MHz clock. The TN871B can switch to a 10MHz clock, and, when used in conjunction with the TN875C Memory Controller, will provide processor speed-up capabilities. That is, the processor can execute code up to 30 percent faster. Wait states are required for all bus cycles. Other boards in the MP can request the additional wait states required for refreshing dynamic RAM, I/O operations, and for certain sequences of dynamic RAM cycle. During refreshing, which requires 5-6% of the available memory bandwidth, any reads of dynamic memory by the microprocessor are delayed until after the refresh operation is completed.

(b) Bus control for the three major bidirectional busses: system data bus, microprocessor data bus, and update address and data bus.

(c) Parity generation and checking for the three major busses. Parity checking is performed on read data.

(d) Wait logic to generate appropriate wait states for EPROM, static RAM, I/O, update, and memory operations.

(e) DMA and dormant request logic to property time requests and grants for bus cycles. A timing circuit to detect invalid or prolonged DMA states.

(f) Diagnostic latches which record address and data on system bus during a nonmaskable interrupt (NMI).

(g) The special function register which allows the forcing of address and parity errors, the source for hamming write inhibit signal, the force text bit which will force a data access into the text memory space, and the control bits for accessing and modifying the write protect map.

(h) Ready timer circuitry. The ready timer generates an NMI, if the processor wait line is not released after 56 μsec.

(i) Interface to the non-interfering match and trace set (NMAT).

TN1397 - PROCESSOR CORE BOARD

2.14 The TN1397 is another version of the TN871B circuit pack. The only difference is the microprocessor chip. The TN1397 uses the MC68012 and the TN871B uses the MC68000.

TN873 - PROCESSOR SUPPORT BOARD

2.15 The TN873 contains the following functions:

(a) Address decoding to enable EPROM, static RAM, I/O, and dynamic RAM.

(b) Address parity checking for system address bus, SA1-AS23.

(c) Subunit interface, including subunit data, address, read and write and not ready leads. Also the subunit board select checker.

(d) Bus control register, which enables DMA activity, update, and entering standby state.

(e) Sanity timer, I/O timer and ready timer circuits. The sanity timer has a safe window from 233 to 699 msec where it may be reset. The I/O timer must be enabled to perform most I/O operations. 114 usec is allowed for I/O cycles before the timer generates an NMI.

(f) Hardware and software error source registers and abort logic for bad address parity. Main reset source register and its masking.

(g) Processor status registers 1 and 2, reflecting the status of the reset counter, and operations on the system bus prior to an NMI.

(h) The I/O data bus interface and the parity generation and checking on the I/O data bus. The translation from 16 bits to 8 bits, necessary for the LSI 8 bit peripherals, is made here.

TN1533 - PROCESSOR SUPPORT BOARD

2.16 TN1533 is another version of the TN873 circuit pack to use in generic 5E4(2).

TN872 - COMMUNICATIONS BOARD

2.17 The TN872 has the following functions:

(a) The DMA unit and support logic. The DMA unit provides four independent channels each with separate byte count and address registers. Each channel can transfer up to 64K bytes of data in one block starting anywhere within a 64K address space. DMA transfers can only be accomplished within the memory data space. No DMA transfer is allowed in text space.

(b) The two synchronous data link controllers (SDLC) for handling the message links, using the BX.25 protocol, between the DLI and MP. Circuitry is provided to connect either SDLC device to either of the serial links. Parity is generated and checked on each of the SDLC data links. The SDLC devices have receive and transmit interrupts to simplify normal (or abnormal) message completion.

(c) The A flip-flop circuitry used to determine which MP has access to either DLI. Only one MP can have its A flip-flop set, when both MPs are running. A MP cannot set its A flip-flop, if the mate's A flop-flop is set, and the mate is running. A NMI clears the A flip-flop. The active processor can set the A flip-flop on a dormant mate.

(d) Circuitry to provide 3 clocks for software timing. Normally one is programmed for a 10 msec interrupt, one for miscellaneous functions, and the third counts the number of 10 msec interrupts (or whatever the first counter is programmed).

(e) The circuitry for controlling the MPs 25 interrupts. The interrupt from the CPI gate array is given the highest priority. The error interrupts from the DLIs, the subunits, and those resulting from mate processor errors are given the next highest priority, allowing them to interrupt the

microprocessor during the I/O timer interval. All other interrupts must wait for the I/O timer interval to complete. Buffers are provided to allow the processor to read the interrupt request lines from the DLIs and subunits directly.

(f) Billing counter and associated circuitry.

(g) Interface circuitry to the DLI control, status, and error source registers.

TN1617 COMMUNICATIONS BOARD

2.18 TN1617 is another version of the TN872 circuit pack. The only difference between these two circuit packs is as follows: On the TN1617 the combined SDLC receive and transmit interrupts from the low priority PIC IREQ6 was removed. A new combined SDLC receive interrupt was added to the low priority PIC IREQ0. This board is used to reduce the message queuing delay for messages between the message switch and the SMP.

TN874/TN874B - RAM/ROM BOARD

2.19 The TN874 is required for speed-up and EMA. The TN874/TN874B board is equipped with the following:

(a) The 128K of EPROM. Parity is used over both address and data to ensure correct data addressing.

(b) The 8K of static RAM. Parity is generated and checked over address and data.

(c) Write data parity checking for the 16-bit system data bus. Writes to memory are aborted if bad parity is detected on the data bus, and an NMI applied to the MP.

(d) The write protect circuitry for all of the address space provided, the data space (which includes EPROM, static RAM, and I/O), and text space. Writes to static or dynamic memory are aborted, if the write protect bit was set for that block. Writes to EPROM can be detected by setting the write protect bit in the write protect control register. The I/O space also has write protect bits associated with it. Writes are not aborted to the I/O space, if a write protect bit is set, but a write protect error is generated.

(e) Control for the alarm control/display packs which sense and control various points within the IM. Scans for request out of service and craft lights for request in progress and out of service are controlled here.

(f) The CPI gate array and associated circuitry.

(g) Stack protect and associated circuitry. When activated, the memory region from 0x80000 to 0x100000 becomes write protected, except for a 2K block assigned to the currently running process. Stacks are available in 2K bytes only allowing a total of 256 separate stacks.

TN875/TN875B/TN875C - MEMORY CONTROLLER BOARD

2.20 The TN875/TN875B/TN875C acts as the interface between the processor and the dynamic memory. When used in conjunction with the TN871B the

TN875C will provide processor speed-up. The TN875B or TN875C are needed when the TN56 memory planes are used. The TN875/TN875B/TN875C board provides the following:

(a) Supports 8 and 16 bit read and write operations with a 32-bit word.

(b) Automatically performs the read-modify-write cycle required to maintain the check bits for all write operations.

(c) Performs an automatic rewrite of corrected data into memory, when a correctable error is detected.

(d) Provides pipelining of write operations so the processor is not unduly delayed while the read-modify-write operation is in progress.

(e) Provides address decoding to select individual memory circuit packs.

(f) Checks that the memory circuit packs are properly selected and receive correct address information on each access.

(g) Blocks write operations if incorrect data parity is received, if a memory address check fails, or if the write protect circuit indicates that the write must not be allowed.

(h) Refresh circuitry. An entire row (address bits 2 - 10) on all memory boards are refreshed simultaneously. A refresh operation occurs approximately every 8 μsec. A 64 μsec timer is reset after each refresh operation; a timeout causes an NMI to be applied to the processor.

(i) Text/Data selection. When in the separate instruction/data mode, A24 serves as the text/data distinguisher. When A24 is a 0, data space is under interrogation. When A24 equals 1, text space is being accessed. When not in SID, mode A24 is ignored.

(j) The hamming gate arrays used for error detection/correction. These gate arrays generate a modified hamming code over 32 bits (8 bits of parity generated) to give double bit error detection and single bit detection/correction.

TN1527 - MEMORY CONTROLLER BOARD

2.21 The TN1527 is another version of the TN875C which acts as the interface between the processor and the dynamic memory. When used in conjunction with the TN1397 the TN1527 will provide processor speed-up.

TN28 MEMORY BOARD

2.22 The TN28 is a 1 Mbyte dynamic RAM memory board. Data is organized into 4 byte words with an additional 8 bites of hamming and parity associated with each word.

TN56 MEMORY BOARD

2.23 The TN56 is a 2Mbyte dynamic RAM memory board. Data is organized into 4 byte words with an additional 8 bits of hamming and parity associated with each word.

TN2012 MEMORY BOARD

2.24 The TN2012 is a 4Mbyte dynamic RAM memory board.

CONTROLLER POWER - FS 5, 6

2.25 The controller power circuit consists of one SN412 or SN516 control and display pack, and three 495FB converters. The SN412 or SN516 circuit pack and one of the 495FB

converters are located in the timeslot interchange unit model 2 (TSIU2). The other two converters are located in the SMPU and MEBU shelves.

SN516 CONTROL AND DISPLAY PACK

2.26 The SN516 control and display pack replaced the SN412 pack. It provides the following function for the MCTU:

1. The human interface allows an operator to power on, power off, request a unit either in service or out of service, and manually override momentarily.

2. Alarm display, allows the operator to read the status of the power circuits by observing an LED display that indicates the following:

   (a) OFF - A red LED, when lit, indicates that power is off.

   (b) ALM - A red LED, when lit, indicates a power fault on the unit fuse or converter alarms. Note, in the alarm state, all power may not be off in the unit. Once an operator powers down the unit for repairs, the OFF LED will light and the ALM LED will extinguish.

   (c) OOS - A yellow LED controlled by the system and is lit whenever the unit is out of service.

   (d) RQIP - A green LED, controlled by the system, lights whenever a request to restore or remove a unit has been received by the system. If this request is denied, the LED will flash for 5 to 10 seconds.

   (e) ROS - A green LED lights whenever the ROS/RST switch is in the request out of service position.

3. Converter control interface, allows the human interface and software interface to control the power converter or converts.

4. Software interface; all 5ESS units will require some interface between their power and the system software. This interface is in the form of scan points to report alarms and signal distributor points to light status LEDs (out-of-service, request-in-progress).

495FB POWER CONVERTER

2.27 The purpose of the converter is to provide a means of converting nominal -48 volt input to a well regulated and isolated +5 volt output for applications in the IMPU2 circuits. The power unit is pulse-width controlled for regulation, self-oscillating and at a fixed frequency. The unit is also self protected by several types of alarms. The 495FB provides +5 volts at 250 watts.

BOOTSTRAPPER - FS 7

2.28 The BTSR function in the IMPU2 is realized using a single circuit pack (TN878). The BTSR receives serial data from a dedicated peripheral interface data bus (PIDB) and performs data transfers into the MP memory. Six bits per PIDB time slot are used for transferring pump data. With 32 PIDB time slots per frame, data is downloaded into the MP memory at a rate of 192 Kbytes/second. Any subset of the 32 PIDB time slots can also be used for a pump with the E bit of a time slot distinguishing used/unused time slots. The BTSR receives pump data in the form of 2 Kbyte blocks. Each block of data is immediately preceded by a 16 byte header containing start code,

block size, starting address, and hash sum check (on the header) for that block.

2.29 The BTSR is a simplex entity which interfaces to the IMPU2 update bus, thereby gaining access to either MP. During the transfer of a block of data, the BTSR places the MP(s) being pumped into total direct memory access (DMA) hold and performs 16 bit word DMA transfers into the MP(s) memory. For the duration of the block the BTSR also assumes maintenance on the MP sanity timer(s). Between blocks of data, the active MP is allowed to run. The BTSR also provides a resident diagnostic to facilitate the early detection of hardware failures, when in the non-pump state.

TN878 - BOOTSTRAPPER BOARD

2.30 The TN878 circuit pack contains the following functions:

(a) Data assembler circuitry. This circuitry distinguishes between active/idle PIDB time slots, strips off the 6 valid data bits from active PIDB time slots and reassembles them into 16 bit words. This circuitry also checks parity for a PIDB time slot and returns the same parity for that time slot on the next frame.

(b) An Intel 8748 microcomputer. The microcomputer is used for BTSR initialization, data block header processing, MP sanity timer maintenance, and execution of resident diagnostic.

(c) An advanced micro device 9517 DMA controller used for transfer of pump data

(d) Address latches for generating the 24 bits of address required.

(e) Control register for software configuration of BTSR. This includes PIDB selection, MP selection(s), and diagnostic selections.

(f) Parity checking/generation circuitry. Three bits of parity are generated over address and two bits of parity over data.

(g) Test RAM and associated circuitry used for diagnostic purposes. Simulated timeslots can be sourced from the test RAM and switched in at the data assembler. Test blocks of data can be loaded into the test RAM and pumped into the MP memory.

(h) Update bus interface circuitry.

3. INTERFACES

EXTERNAL INTERFACES

3.01 All input and output points to the unit are listed in CAD 1. They are grouped by function and then alphabetized by net name.

MEMORY DATA, ADDRESS, AND CONTROL (CAD 3, 4)

3.02 This bus connects all additional memory circuit packs, which are located in a separate shelf, to the MPs dynamic memory controller (TN875). It consists of the following:

(a) 40 bidirectional data leads. This is composed of 32 data bits (4 bytes) pulse 8 bits of hamming and parity.

(b) 20 bidirectional address lines, plus two parity leads. There are 8 rows address leads, 8 column address leads, a row parity and column parity lead, and four array selects to select a 64K array.

(c) 14 memory control signals used for selecting memory boards, initiating memory cycles,

controlling memory data bus directions, indicating refresh operations, strobing data into memory, and providing update compatibility with future memory board designs.

CONTROLLER BUS TO DLI (CAD 9, 10)

3.03 The controller bus to DLI contains two interfaces between the IMPU2 and the DLI, the message interface and control interface. The message interface sends and receives message timeslot data to/from the DLIs. The control interface sends control data from the MP to set the modes of operations in the DLIs. It also sends the status of the DLIs to the MP.

3.04 After the message time slot is extracted from the normal data path through the DLI, parity is checked and generated over the six bits that are sent over the 48 KHz data links to the synchronous data link controller (SDLC) in both MPs. The generated parity is also sent to the SDLCs in both MPs over separate data leads. At the same time, the CPI bit is sent to the CPI gate arrays in both MPs. Two clocks are sent to both MPs from the clock circuit in the DLI. These clocks are used by the MP to clock the received message time slot data and parity into the SDLCs. In the return direction, the MP uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each DLI contains two message interfaces to and from both sides of the duplex MP.

3.05 The IMPU2-DLI control interface is composed of three signal leads and one clock lead from each side of the IMPU2 to the DLI and two signal leads from the DLI to each side of the IMPU2. A control lead originates from each side of the IMPU2 to indicate which side is active and sending commands to the DLI. Another control lead comes from each MP side to control when a read or write command is executed by the DLI. A 1.875 MHz clock is sent by each MP side, along with the data which specifies the command to be executed. The entire write operation is specified in a serial 16-bit command in which the first eight bits contain the data to be written, followed by a spare bit and a parity bit for the eight bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four address bits which specify the register to be written. During a read operation, only six bits are sent by the MP to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits which determine the register to be read. Following the execution of the read command as initiated by the .MPGO signal, eight bits of data plus one parity bit (parity over the data) are sent back to both MPs on separate signal leads with the results of the read operation. Interrupt leads that indicate error conditions exist in the ESRs of the DLI are also a part of the IMPU2-DLI control interface. These signals are asynchronous to the MP and have no specified timing relationship.

SUBUNIT BUS (CAD 5, 6)

3.06 The IMPU2 subunit interface bus is used as the control interface to the TSI, SP, and CI from the MP. It utilizes a 16-bit bidirectional data bus and a 6-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two parity leads (also bidirectional), one each for the low byte and high byte of data. The parity is computed such that the sum of bits, set to a logic one in each byte (including the parity bit), is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

3.07 There are five control leads to each subunit. Two of these, the read and write signals, are shared by all subunits. These two signals are used to distinguish between read and write operations to a subunit and are used by the selected subunit to gate the data to/from the data bus. The other three controls are board select, ready, and interrupt. Each individual subunit has separate board select, ready, and interrupt leads. The board select enables the desired subunit. The ready lead is used by the subunit to extend the MP bus cycle for subunits with slower response time. And the interrupt lead is used by the subunit to interrupt the MP. In addition, the CIs receive a lead called NAE, which is used to force the select wire pair in the PICB on the non-active side to a nonconductive state.

CONTROLLER POWER CAD (12, 13)

3.08 All controller power converters are connected to the fuse block via a hot lead -48V and a ground potential lead 48RTN.

FAN UNIT SCAN AND SD POINTS (CAD 19, 20)

3.09 A fan failure is reported to the MP via a scan point from the fan unit. A fan alarm can be retired by the MP, using a distribute point to the fan unit.

BTSR PIDB INTERFACE (CAD 17)

3.10 The BTSR PIDB interface provides the data path to the BTSR for fast pump. A PIDB consists of 4 differentially driven signals used for data transfer. The data out and data in signals are used for serial transmission of data between the BTSR and the data interface (DI). A 4.096 MHz clock is provided for clocking data in/out of the BTSR. Data is clocked into the BTSR on the falling edge of the clock signals. Data is clocked out of the BTSR on the rising edge of the clock signals. A PIDB frame consists of thirty-two 16-bit timeslots. The BTSR provides a 28.5 time slot skew between data in time slots and data out time slots to meet TSIU2 requirements. The 8 KHz synchronization signal is used for synchronizing the BTSR with the DI. A PIDB cable can vary in length, but has a maximum length of 20 feet.

ITS TEST ACCESS (CAD 15)

3.11 The intergrated test system (ITS) interface pack (TN319) provides the means of accessing a host system (UNIX) from the IMPU2. Use of ITS permits a user to interactively examine and modify the execution of an application program.

ITS accommodates step-by-step execution of target programs, the setting of breakpoints, and the running of error detection programs.

UPDATE BUS

3.12 The update bus runs between both MPs and is used by the active MP for keeping all data areas in the standby MP up to date, by the BTSR when pumping an MP, and as a test access point for monitoring the activity of the MPs.

The update bus consists of the following:

(a) 25 bidirectional address lines with parity. The address space is treated as 1024K 16-bit words with separate byte selects. Even parity is used over the update bus.

(b) 18 bidirectional data and parity lines, 16 bits data and 2 bits parity.

(c) 2 bidirectional byte select signals. These selects indicate which data byte is affected by the data transfer. Both selects active indicate a 16-bit operation while one active indicates an 8-bit operation.

(d) 6 test set status signals.

(e) 2 cross coupled reset signals, one causing a maskable reset in this MP (an input); the other, a maskable reset in the mate MP (an output).

(f) 2 status signals indicating the running/dormant status of each MP. One signal (when active) indicates this MP is in the dormant state. The other signal (when active) indicates the mate MP is in the dormant state.

(g) 4 error status signals. Two indicate the occurrence of a subunit or processor error in this MP; two indicate the occurrence of a subunit or processor error in the other MP.

3.13 The positive edge of UADCLKB latches the update address in the mate MP. A high level on UWAIT0 indicates a ready state of the memory system in the dormant controller. Control signals URD0 and UWR0 are used for sending read/write data to/from the mate.

3.14 The refresh strategy allows each MP autonomous control of refreshing. Writes to the mate are done on a delayed asynchronous basis. For each write operation, the address and data is latched at the mate MP to allow the write to proceed until the next mate memory operation from the running MP. In the update mode, only writes are done in both the signals. Between each write there normally are several read operations for either opcode fetching or data reads. The low duty cycle of writes provides a large average time per write for the dormant memory system. Allowing the write to proceed on the mate after it has completed its function in the running controller, requires that before starting any memory operations directed to the mate MP, it is necessary to check the ready status of the mate memory system. The ready logic delays the running MP, until the mate's memory is ready whenever the running MP attempts to initiate a mate memory operation.

3.15 A read from the mate's memory waits until the read data is available before proceeding to the next instruction. Three wait cycles are added to the memory operation to ensure sufficient time for a ready signal to be returned from the mate during the read. The read is further delayed one clock cycle before reaching the microprocessor to insure proper deskewing of the read data and ready. The write data and memory address are latched at the mate controller, because the update bus must still reflect the microprocessor operations between successive mate writes.

NMAT TEST ACCESS (CAD 16)

3.16 The noninterfering match and trace interface provides access to either MP via the update bus. The test set can also take active control of the update bus to control either MP. All memory operations are reported to the test set for its tracing and breakpoint features via the update bus. The six test set status signals available in the update bus are used to indicate whether the current operation on the update bus is a read, write, or opcode fetch. They are also used for forcing an MP into the dormant state independent of all resets or forcing an MP to release the update bus to allow the test set to use it for controlling the MP.

UNIT LAYOUT

3.17 The IMPU2 consists of a single shelf of circuit packs. The shelf is divided into duplicated halves, right and left side. The right half is an exact duplicate of the left, with the only exception being physical location. The physical location of each circuit pack is a mirror image of the other half, rather than maintaining the same physical relationship between circuit packs. Each half is a single failure group. Three center locations in the shelf are used for test access, ITS, and the BTSR respectively.

One simplex side of the IMPU2 consists of the following circuit packs:

IMPU2 FAILURE GROUP

Pack Code	Quantity
TN871/B	1
TN872	1
TN873	1
TN874/B	1
TN875/B/C	1
TN28/TN56	1-5
495FB	1

It must be noted that the TSIU2 is part of the IMPU2 failure group, and the BTSR board is in its own failure group, since there is only one TN878 BTSR board per IMPU2.

3.18 Extended Memory Addressing (EMA) unit layout per simplex side.

Pack Code	Quantity
TN1397	1
TN1533	1
TN872	1
TN874B	1
TN1527	1
TN2012	1-5
495FB	1

This configuration is used when more than 16 Mbytes of dynamic memory are needed. Some minor backplane wiring changes are also needed to achieve E.M.A.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltages

(a) -48 +4.5V -6.25V

1.02 Ambient Temperature

(a) 0° to 70° Centigrade (at circuit pack).

(b) 0° to 50° Centigrade (office aisle ambient).

2. FUNCTIONAL DESTINATIONS

Designation (FDESG)	Meaning
0MEM2	Side 0, Memory Board 2
0MEM3	Side 0, Memory Board 3
0MEM4	Side 0, Memory Board 4
0MEM5	Side 0, Memory Board 5
0MPC	Side 0, Module Processor Core Board
0MPCOM	Side 0, Module Processor Communication Board
0MPDMC	Side 0, Module Processor Dynamic Memory Controller
0MPROMRA	Side 0, Module Processor RAM/ROM Board
0MPS	Side 0, Module Processor Support Board
1MEM1	Side 1, Memory Board 1
1MEM2	Side 1, Memory Board 2

1MEM3	Side 1, Memory Board 3
1MEM4	Side 1, Memory Board 4
1MEM5	Side 1, Memory Board 5
1MPC	Side 1, Module Processor Core Board
1MPCOM	Side 1, Module Processor Communication Board
1MPDMC	Side 1, Module Processor Dynamic Memory Controller
1MPROMRA	Side 1, Module Processor RAM/ROM board
1MPS	Side 1, Module Processor Support Board
BTSR	Bootstrapper Board

3. FUNCTIONS

The function of this unit is described in Section I of this Circuit Description.

4. CONNECTING CIRCUITS

4.01 When these circuits are listed on the keysheet, the connecting information thereon should be followed:

(a) Time-Slot Interchange Unit, Model 2 - SD5D045

(b) Fan Unit - SD5D019

(c) Fuse Panel - SD5D034

(d) Fuse/Filter Panel - SD5D053

SPECIAL REFERENCES

[1] Circuit Description, Time-Slot Interchanger Unit - SD5D041-01.

[2] Circuit Description, Time-Slot Interchange Unit Model 2 - SD5D045-01.

[3] G. H. Kallas, B. R. Krapec, J. D. Loop, S. McRoy, J. A. Novak, P. M Wempe, S. A. Zeile, "Module Controller and TSI Unit DS - Issue 2", June 23, 1981.

[4] R. A. Wilson, "Central Processor Intervention (CPI) Gate Array Description", April 8, 1981.

[5] J. D. Loop, "Combining Software Test System (STS) and Monitor - Debugger (MD) in the Improved Module Processor (IMP)", April 29, 1981.

[6] Circuit Description, Interface Module Processor Unit - SD5D040-02.

[7] C. M. Herse, "Fast Pump Hardware in the Interface Module", May 21, 1982, 55612-820521.01MF.

[8] J. D. Loop, "A Billing Clock Implementation Proposal for the Interface Module Processor", August 30, 1982, 55612-820830.02MF.

SECTION IV - REASON FOR REISSUE

B. Changes in Apparatus

B.1 ADDED

Option ZQ for MC5X260A1B App. Fig. 2
Option ZR for MC5X261A1B App. Fig. 2
Option ZS for MC5X113A1 App. Fig. 2
Option ZT for MC5X113A1B App. Fig. 2
Option ZP for MC5X248A1B App. Fig. 2
Option ZN for MC5X248A1 App. Fig. 2

B.2 ADDED

Option ZU for TN1397 CKT pack
App. Fig. 8
Option ZV for TN1533 CKT pack
App. Fig. 8
Option ZW for TN1527 CKT pack
App. Fig. 8
Option ZX for Backplane Wiring
App. Fig. 8

B.3 ADDED

Wiring Option ZY, FS 1, FS 2.

D. Description of Changes

D.1 Corrected errors in options "ZN" and "ZP" which appeared on Drawing Issue 13AC. Amended the list options and notes associated with the speed-up feature. Amended list 19 of J5D003AY-1.

D.2 Transmits hardware information to provide the extended memory address (EMA) feature.

D.3 Provides wiring option for the SMPU-2 when used in a 30 channel multimodule RSM (MMRSM).

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