5ESS® SWITCHING EQUIPMENT
MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2
CIRCUIT

B. Changes

No Change in Apparatus

D. Description of Changes

D.1 The note 323 of SD5D151-01 gets updated to include DLI switch settings when the ISCN feature is used.

F. Changes in CD Sections

F1. No changes to the CD.

AT&T NETWORK SYSTEMS

NAC150300-DE-FNG

5ESS® SWITCHING EQUIPMENT
MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2
CIRCUIT

4. REASONS FOR REISSUE

B. Changes in Apparatus

Added the option "YL" to provide UN395, PI2 circuit pack, App. Fig. 11.

D. Description of Changes

The addition of this option allows the MCTU2 unit to interface with the PH3 circuit packs in the PSU. This allows a packet throughput of up to 100 MHz.

F. Changes in CD Sections

Add the following to the table of contents on page 1:
Under Section II - Detailed Description Item 7 change to read:
Packet Interface - TN1042 ... 19
Packet Interface 2 - UN395 ... 19

Add the following to Section II Functional Designations on page 3: Change Item 7 under paragraph 1.01 to read: packet interface (PI), (PI2).

Update paragraph 1.08 on page 4 by appending the following to the current description:

Packet Interface Model 2 - UN395
The PI2 is essentially an enhanced version of the PI with improved performance and the ability to support multiple PSU/PSU2 complexes. The PSU2 is being developed for improved packet throughput for existing PSU features (ISDN), and for a feature for wireless referred to as code division multiplexed access (CDMA). The PI2 is architecturally the same as the PI and provides the basic PI function, which is to buffer signaling packets between the PSU/PSU2 and SMP20.

The current PI supports one 10Mbps PSU complex. The PI2 can support up to two PSU complexes at a 10MBps packet bus rate (PSU) or at a 100MBps packet bus rate (PSU2).

Add the following to paragraph 1.10 on page 4, so that the paragraph reads:

The PWRCTRL provides the SMP, CI DI, TSI, SP, and PI/PI2 a common +5 volt power supply in the MCTU2.

Add the following to paragraph 2.16, subparagraph b., page 11, so that line 4 reads:

(TSI, SP, CI, and PI/PI2).

Append the following information to paragraph 7.02, page 20:

The PI2 provides the buffering of signaling packets between the PSU complexes (PSU, PSU2) through the packet bus (PB), and from the SMP2 through the SUIB. Resident on the PI2 is a 68040 based core design, which administers the transmission and reception of signaling packets to and from the PSUs through PBMAC devices and the arbitration of the sending and receiving packets to the SMP2 through a 1M byte FIFO dual port static RAM.

Replace section I, paragraphs 10.19 and 10.20, on page 25 with the following:

I. PACKET SWITCH UNIT (PSU/PSU2) INTERFACE

10.19 The PB is a duplexed bus connecting the PI/PI2 to the PSU or PSU2 complex. A PI only supports a 10MBps PB, where the PI2 supports both 10MBps and 100MBps PBs. The following paragraphs describe the 10MBps and 100MBps packet bus interface.

For the 10MBps interface, six differentially-balanced signals are used:

a. clear to send,

b. transmit/receive data,

c. request to send,

d. receive clock,

e. transmit clock, and

f. carrier sense.

For 10MBps communication, the PSU provides the receive clock which is looped on the PI/PI2 back to the PSU (transmit clock). If the PI/PI2 is transmitting a signaling packet to the PSU, the PI/PI2 will issue a request to send. The PSU responds by sending carrier sense and clear to send, and the PI/PI2 transmits the signaling packet. If the PSU is transmitting signaling packets to the PI/PI2, the PSU sends carrier sense and receive data to the PI/PI2.

10.20 For the 100MBps interface, eight differentially-balance signals are used:

a. clear to send,

b. transmit data (2),

c. receive data (2),

d. request to send,

e. receive clock, and

f. transit clock.

For 100MBps communication, the PSU2 provides the receive clock, which is looped on the PI2 back to the PSU2 (transmit clock). If the PI2 is transmitting a signaling packet to the PSU2, the PI2 will issue a request to send. The PSU2 responds by sending clear to send, and the PI2 transmits the signaling packet. If the PSU2 is transmitting signaling packets to the PI2, the PSU2 sends receive data to the PI2.

Change Section B, paragraph 11.03, line 4 to read: (TSI, SP, CI, PI/PI2).

Add the following to REFERENCES on page 32: s. CPSM - UN395

Change line 19 of paragraph 12.02 on page 30 to read: 04-112 (0,1)PI/PI2 TN1042 or UN395

Insert the following information between lines 29 and 30 of Section 2, paragraph 2.01, on page 30:

PI2 Packet Interface UN395

Add the following information to item g., Section 4, Paragraph 4.03, on page 31:

PSU2 - SD5D523-01

AT&T BELL LABORATORIES

DEPT NA5350300-DE-FNG

CD-5D151-01
ISSUE 2M
APPENDIX 7B
DWG ISSUE 16B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

Added the option and apparatus figures YJ and 23.

D. Description of Changes

This change adds the UN517B firmware to support the administrative workstation option (AWO) application and makes it compatible with generic 5EE6.1.

AT&T BELL LABORATORIES

DEPT 55535-DE-FNG

CD-5D151-01
ISSUE 2M
APPENDIX 6B
DWG ISSUE 15B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

Added the options YD, YE, YF, YG, YH and YI. Added apparatus figures 17, 18, 19, 20, 21, and 22.

D. Description of Changes

This change introduces the circuit packs and panel boards to be used in administrative workstation option (AWO) application.

F. Changes in CD Section

Added reference that network control and timing (NCT) links are replaced by Ethernet interface, and that TN1838 clock facility circuit pack provides recover timing.

AT&T BELL LABORATORIES

DEPT 55535-DE-FNG

CD-5D151-01
ISSUE 2M
APPENDIX 5B
DWG ISSUE 14B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

Added option auto power recovery to apparatus figures 5, 8, and 12. Added option YC to apparatus figure 13.

D. Description of Changes

This change introduces automatic power recovery and optical data links (ODL50s) that are compatible with International Special Committee on Radio Interference Subsection 22 (CISPER 22).

AT&T BELL LABORATORIES

DEPT 55535-DE-FNG

CD-5D151-01
ISSUE 2M
APPENDIX 4M
DWG ISSUE 13M
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

Added a new fuse table.

D. Description of Changes

Unit is to be provided with new fuses when a modular fuse filter unit is used as the power source.

AT&T BELL LABORATORIES

DEPT 55535-DE-FNG

CD-5D151-01
ISSUE 2M
APPENDIX 3B
DWG ISSUE 12B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

Added the following options to apparatus figure 5: ZB, ZC, ZM, and ZV.

D. Description of Changes

This change introduces a new circuit pack, UN517B, and microcode to support this circuit pack.

AT&T BELL LABORATORIES

DEPT 55535-DE-FNG

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT MODEL 2 CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added option "ZM" to provide MC5X285AZ Microcode (UN517) for 5EE4(1) generic in APP.FIG.5. Added option "ZO" to APP.FIG.8 for C.E.P.T. voltage requirements. (TN1077C Circuit Pack)

D. Description of Change

D.1 The MC5X285AZ is assigned to the UN517 to accommodate the 5EE4(1) generic. Introduce the TN1077C Circuit Pack to meet C.E.P.T. voltage requirements.

F. Changes in CD Sections

F.1 Add references to Section I 3.01 to TN1077C Circuit Pack.

AT&T BELL LABORATORIES

DEPT 55422-PRS-DML

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

B. Changes in Apparatus

B.1 Options "ZK" and "ZL" are assigned to the TN1086 and the TN1086B respectively.

D. Description of Change

D.1 Introduce the TN1086B circuit pack, which provides the new feature of equipping an SM with both 24 and 30 channel capability.

F. Changes in CD Sections

F.1 Add references to TN1086B in Section II, paragraph 4.01.

AT&T BELL LABORATORIES

DEPT 55422-DPD-JCB

5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGE UNIT, MODEL 2 CIRCUIT

TABLE OF CONTENTS PAGE

TABLE OF CONTENTS PAGE

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This document is a circuit description of the Module Controller and Time slot interchange Unit, model 2 (MCTU2). The MCTU2 has been developed for improved processor performance and is the sole reason for its introduction. Improved performance was achieved by redesigning the processor complex using the Motorola 68020 microprocessor.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 5ESS Switch is a digital time division switch with a time-space-time architecture. The Time Multiplexed Switch (TMS) provides a centralized space division switching function and connects to various Switching Modules (SMs) that perform time division switching and interface to transmission facilities.

2.02 The MCTU2, six-fan unit and Fuse/Filter Unit (FFU) are common to all SMs. Various peripheral units[1] are equipped in the SM as needed. The MCTU2 resides within an SM and provides the following:

a. a Switching Module Processor (SMP) to provide the operating environment for software and interfaces to sub-units,

b. a fast pump capability used for initialization of SMP memory,

c. a time division switch under control of the SMP,

d. preprocessing on the signaling and control bits of the time slot data,

e. an interface to Network Control and Timing (NCT) links,

f. an interface to peripheral units for control information from the SMP,

g. an interface to peripheral units for Pulse Code Modulation (PCM) data, and

h. a Digital Service Circuit (DSC) to provide detection/generation of tones used for signaling.

2.03 The MCTU2 is a duplex unit containing two sides (side 0 and

---

1. Global Digital Service Unit, Metallic Service Unit, Digital Line and Trunk Unit, Line Unit, Trunk Unit, Packet Switch Unit, etc.

1). The active processor updates the mate (nonactive) processor to provide the ability to switch from side to side. Under no-fault conditions, switching to the mate side is accomplished without introducing errors. Error-checking circuitry and diagnostic aids are used extensively to facilitate maintenance of the MCTU2.

SECTION II - DETAILED DESCRIPTION

1. FUNCTIONAL DESIGNATIONS

1.01 The MCTU2 has nine subfunctions:

1. Switch Module Processor (SMP),
2. Dual Link Interface (DLI),
3. Time Slot Interchanger (TSI),
4. Signal Processor (SP),
5. Data Interface (DI),
6. Control Interface (CI),
7. Packet Interface (PI),
8. Digital Service Circuit (DSC), and
9. PoWeR ConTRoL (PWRCTRL).

1.02 The SMP provides the operating environment for software and interfaces to the TSI sub-units. The SMP can operate in the active, standby, or Out Of Service (OOS) mode. In the active state, the SMP performs call processing, executes code, and controls the DLIs and interface units. In the standby state, the SMP does not execute code but allows the active processor access to its internal buses. In the OOS state, the SMP is able to execute code but can not access the DLIs. The normal operating mode of the SMP is with one processor active and the other processor standby. An "active" SMP means that its "A" flip-flop is set and that it is executing code. Circuitry is provided to ensure that neither a standby nor OOS processor can access a DLI. Under normal (no faults) operating conditions, the active processor keeps all data areas in the standby controller up to date, such that the standby processor can, at any time, be made active. Should a fault occur in the active processor, the standby processor will be made active and the active processor made OOS.

1.03 The DLI provides the interface to NCT links. It recovers timing information from these links to provide timing for the MCTU2. The DLI contains the transmit and receive circuitry needed to interface to the optical links. It also provides the SMP with an interface to the Message Time Slot (MTS) on each NCT link. Because the DLI is in the same failure group as the TMS, cross coupling is necessary for all connections between the DLIs and the duplex MCTU2. The DLI selects one of two NCT links connected to it or the mate DLI as a reference timing source. Under SMP control, the TSI selects one of the two DLIs as a clock source and distributes this clock to the rest of the MCTU2.

1.04 The TSI is the time division switch, and it contains two 512 x 512 time slot interchangers, one for data from the TMS to peripheral units and one for data from peripheral units to the TMS. The two 512 x 512 switches are connected such that time slots may be looped, thereby providing the capability to connect peripheral time slots to other peripheral time slots for intramodule calls. The TSI also provides a data port to the DSC.

1.05 The SP performs the hit timing and processing on signaling and control bits (A-G) from peripheral time slots. It provides the SMP access to

these bits and provides a First In First Out (FIFO) type queue to report state changes of these bits. It also allows the SMP to source these bits to peripheral units.

1.06 The DI provides the data interface to peripheral units. It reformats time slot information and does a 2:1 concentration on peripheral time slots. Two DIs are connected to the TSI, each providing the TSI with 256 time slots per frame. Each DI provides sixteen Peripheral Interface Data Buses (PIDBs) for connection to peripheral units.

1.07 The CI provides the interface between the SMP and the various peripheral units for control information through Peripheral Interface Control Buses (PICBs). Each CI provides twenty-three PICB connections. The MCTU2 may be equipped with two CIs (per side) to provide a total of forty-six PICBs.

1.08 The PI provides the interface to the Packet Switch Unit (PSU). The PI and associated PSU is used in an SM for the Integrated Services Digital Network (ISDN). The PI and PSU provide a centralized high-bandwidth interface to support packetized data and signaling messages. By centralizing packet processing in the PSU, efficient signaling, maintenance, and administrative interfaces are maintained and the distributed architecture of the 5ESS Switch is enhanced.

1.09 The DSC is responsible for creating and transmitting call-progress tones, multifrequency signals, tone-dialing signals, and common channel interoffice signaling continuity check tones. It also does dial-pulse collection, tone decoding, and detection of multifrequency signals. To provide reliable operation, the Digit Service Function is composed of two service groups that share the load, so that a single fault can, at most, reduce the capacity by fifty percent. The DSC uses AT&T-I digital signal processing chips for its required services.

1.10 The PWRCTRL provides the SMP, CI, DI, TSI, SP, and PI a common +5 volt power supply in the MCTU2.

1.11 The sections that follow deal with the nine previously mentioned MCTU2 subfunctions in more detail.

2. SWITCHING MODULE PROCESSOR

2.01 The normal operating mode of the SMP is active/standby. In this mode, one of the processors, actively executing code, is said to be in the running state. In addition, the processor is called "active" if its "A" flip flop is set. The other processor is in the standby "dormant" mode. While dormant, the internal buses of the SMP can be controlled by the mate[2], allowing it read and write access to the dormant processor. Whenever a processor becomes dormant, the microprocessor releases control of the buses to the update bus. This operating mode allows the running processor to keep an up-to-date copy of its memory in the dormant processor.

2.02 The SMP can operate in the following hardware states:

a. The microprocessor is actively controlling the buses of its side. While running, the mate is unable to gain access to the running processor's buses.

---

2. Mate refers to the other processor in the SMP.

b. When dormant, the microprocessor is in a Direct Memory Access (DMA) hold condition, granting the mate access to all internal buses via the update bus.

c. The DMA transfer mode allows the DMA unit to transfer data bytes to/from the message time slot links. The DMA unit controls the internal buses. If the update mode is enabled, the data writes also occur in the mate.

2.03 Active and standby are software states, distinct from hardware states. An active processor must be running and have access to the DLIs. A standby processor is dormant with its mate active and keeping its memory up to date.

2.04 Two types of memory are provided in the SMP: Erasable Programmable Read-Only Memory (EPROM) and Dynamic Random Access Memory (DRAM). The EPROM provides program storage for power-up initialization and fault recovery. There is 8K of address space reserved for Input/Output (I/O) access via memory reference instructions. The SMP uses up to six TN1374 or TN1376 memory boards. The TN1374 contains 4 Mbytes of DRAM and the TN1376 8 Mbytes. This allows a maximum of 48 Mbytes of System Memory to be equipped in the MCTU2. The SMP may use a combination of TN1374s and TN1376s, but the off-line processor must contain the same amount of memory as the on-line processor. Detection and correction of single bit memory errors and detection of double bit errors is provided by Hamming parity across all of memory. Memory word size is thirty-nine bits, which includes 4 bytes of data and seven bits of Hamming.

2.05 A write-protection capability is provided on SMP memory. Each 1K byte of Random Access Memory (RAM) is protectable. Any attempt by software to write into a write-protected area results in a reset (nonmaskable interrupt) to the SMP and the write being blocked. Additionally, a mechanism for implementing stack protection is available. When activated, the memory region from 0x80000 to 0x180000 becomes write-protected, except for a 2K or 4K block assigned to the currently running process. Stacks are available in 2K or 4K bytes, allowing a total of 256 or 512 separate stacks.

2.06 To allow efficient control of, and response to asynchronous events, twenty-five interrupts are provided per side in the SMP. Twenty-four of the interrupts are presented to the SMP as level-4 interrupts. Errors from sub-units, error reporting and message completion from serial data link controllers, time intervals, status changes, and errors are all presented to the processor as interrupts. Two types of level-4 interrupts are provided: a high-priority set for reporting maintenance errors from sub-units and a low-priority set for operational interrupts. The twenty-fifth interrupt arrives at the SMP as a level-5 (higher priority) interrupt. This interrupt is generated by the Central Processor Intervention (CPI) circuitry, and is used to indicate a TMS switch.

2.07 Each processor possesses a sanity timer, reset under software control. Failure to reset the timer or resetting the timer too often causes a reset (nonmaskable interrupt) to be applied to the SMP. The active processor resets the timer in the standby processor. A timeout of the sanity timer in the standby processor results in the standby processor leaving the standby state and, under software control, entering the OOS state. The minimum interval requirement is disabled in the off-line side.

2.08 The SMP receives two message time slots from each DLI. The SMP can select any two of these time slots for message communication with the MeSsaGe Switch (MSGS). Messages over the message time slots are formatted similar to an X.25 communication protocol. Communication with the Administrative Module (AM) utilizes SDLC and DMA devices in the SMP.

2.09 A Central Processor Intervention (CPI) path from the AM to each SMP can be used as a hard-wired path to force an SM into a known state. The SMP has a minimum of control over the path of the CPI message, and no control over the designated action taking place. The seven possible CPI actions are:

1. force SMP side 0 active, side 1 OOS,
2. force SMP side 1 active, side 0 OOS,
3. clear the force active set by one of the above CPI functions,
4. force processor(s) reset(s),
5. disable the sanity timers in both processors,
6. enable the sanity timers in both processors, and
7. cause a level 5 interrupt to the SMP indicating a TMS switch.

2.10 A Mate Power Fail (MPF) detection capability is provided to prevent the active processor from mutilating the mate's memory when the active processor sustains a power failure. The circuitry prevents a processor that has lost power from writing the mate and forces the mate active.

2.11 A 32-bit counter is used for a stable billing clock. Either DLI 0 or DLI 1 can drive the 32-bit counter, with an enable bit provided for each DLI clock. A software strobe point, used for diagnostics, can advance the counter at a software rate if the two clocks are disabled.

2.12 The SMP function in the MCTU2 is realized using the following five circuit packs:

1. the processor core (CORE) contained on the UN515 or UN520 circuit packs,
2. the processor Core Support 1 (CS1) contained on the UN516 circuit pack,
3. the processor Core Support 2 (CS2) contained on the UN517 circuit pack,
4. the processor APPLication 1 (APPL1) contained on the UN518 circuit pack, and
5. the processor MEMory (MEM) contained on one to six TN1374 or TN1376 circuit packs.

2.13 A. Core - UN515/UN520

The processor core board contains the Motorola MC68020 microprocessor along with the following functions:

a. System Bus - provides a permanent master of a common bus to all SMP circuit packs. Although the core may grant the bus to DMA requests, it generates the timing for all bus cycles. The system bus is comprised of Address, Data, and Control signals. All system bus signals are prefixed with an 'S' to aid in identification. All control signals are assumed to be active low signals unless otherwise indicated. Three high-level

address ranges are decoded and distributed over the system bus:

1. system ROM enable, active for addresses in the range 0x0 to 0x1FFFF;
2. system I/O enable, active for addresses in the range 0x20000 to 0x21FFF; and
3. system RAM enable, active for addresses in the range 0x22000 to 0xFFFFFFF (256 Mbytes).

b. Update Bus - provides the connection between two core circuit packs to form a duplex processing complex. One core is the master and the other is the slave. The update bus master is commonly referred to as the Active processor and the slave is known as the Mate processor. The update bus is a bi-directional bus comprised of address, data, and control signals. It is used to provide communication between the system bus of two processor complexes. One processing side is the master of the update bus initiating and controlling all transactions over the bus. The update bus master is called the Active processor. The slave is known as the Mate processor. In the Normal mode of operation, the Active processor has its update bus enabled, and all writes on the system bus of the Active Processor are transferred onto the system bus of the Mate processor via the update bus. This insures that all data structures and peripherals are identical between both processors. The Active processor also has the ability to read memory and peripherals in its mate. The update Address bus consists of a full 32-bit address with even parity calculated across each byte. When a processor has becomed slaved to the update bus, a state known as Total Hold, the update Address bus is a reflection of the Active processor's system Address bus. The update Data bus is a full 32-bit data bus with even parity across each byte of data. Byte, Word, and Long Word operations are permitted. However, the address spectrums between the Active and Mate processors must have the same size peripherals at the same addresses. The control for the update bus is accomplished over fourteen signals. The six-byte selects and parity that are present on the system bus are reflected on the update bus. Three ready leads, similar to the three readys on the system bus, are present to allow for sizing of the update Data bus. The signal Mate UPdate ENable (MUPEN) is used to control the sequencing for turning on the update data bus. The signal Mate Parity ERRor (MPERR) is used to generate a parity error in the mate processor if the active processor detects a parity error on a mate-only read. The last two signals are UREAD and UWRITE. Once a processor has entered Total Hold, either of these signals being activated will result in a bus cycle being run on the mate's system bus, using the address, data, and byte selects from the update bus.

c. External Instruction Cache - the MC68020 microprocessor contains a 256-Byte internal instruction cache. The core circuit pack augments this small internal cache with an external 16 Kbyte four-way set associative instruction cache. The UN520 also contains an external data cache to enhance real time performance. Each bank is organized as 1K by four bytes, for a total of 4 Kbytes per bank. The replacement algorithm is a Least Recently Used (LRU) algorithm which

provides a higher cache hit ratio than the more commonly implemented random replacement algorithms. The line size of the cache is four bytes. The external instruction cache does not prefetch instructions, rather, once an instruction is found not to be in the cache, a bus cycle is generated to main memory to fetch the instruction. As the data is presented to the microprocessor, the LRU algorithm determines which bank contains the oldest data and saves the instruction in the appropriate bank while updating the time stamp on all four banks. On a cache hit, the requested address is checked to verify that it is in the cache, the Data Size ACKnowledge (DSACK) to the microprocessor is pulled, and new date codes are generated for each bank. The bank that contained the data is marked newest, and each of the other four banks are aged accordingly to maintain one bank at each date.

d. Interrupt Processing - provides five different interrupt sources and encodes these sources into four levels of interrupts.

e. System Bus Control - manages the requests from the microprocessor, DMA sources, or the update bus to perform bus cycles on the system bus. Timing margins and system bus protocol are maintained to insure proper transfer of data.

f. Update Bus Control - provides two major functions. The first is as update bus master to generate the appropriate timing to request the mate processor to perform operations. The second function is as a mate processor, to receive cycle requests from an active processor and relay those requests to the system bus control.

g. Power Up Reset - provides the microprocessor and other MCTU2 circuit packs a proper reset sequence on initial power application. The circuit also insures that if the microprocessor halts, a system reset is applied to re-start the system.

h. DMA Arbitration - provides three levels of DMA for the SMP:

   i. Currently the SDLC devices and the Bootstrapper share the lowest priority channel.

   ii. The second channel is available for future expansion.

   iii. A third and highest priority DMA request is used to implement the slaving to the update bus. The signal DORmant ReQuest (DORRQ) slaves the system bus to the update bus. This state is referred to as dormant.

i. Parity Generation - provides system and update address parity generation for all bus cycles that were initiated by the MC68020 microprocessor. If the bus cycle is initiated by either DMA or the update bus, the responsibility for address parity generation resides with the initiator of the bus cycle. The core sources data parity for all write cycles that are initiated by the MC68020 microprocessor. Data parity is checked on data returned to the microprocessor on read cycles that were initiated by the microprocessor. The overriding philosophy on data parity is that it is generated by the source of the data and checked by the destination. For write cycles, the core sources data to other circuit packs, and on reads, other packs

provide data to the core, or more specifically, the microprocessor.

2.14 B. Core Support 1 - UN516

The processor Core Support 1 provides the following functions for the SMP:

a. Active Circuitry - The active circuit determines which SMP side has access to the DLI and peripherals circuits.

b. Running/Dormant Logic - This circuitry is comprised of the Stop Mate Strobe, the Clear Dormant Strobe, and the Dormant Request Logic.

c. CPI - The Central Processor Intervention circuitry provides a direct hard-wired communication path from the central processor to each controller in the SM.

d. Write Protect Control - The write protect status and control register provides the software interface for write protect. This register is used to enable/disable or determine the status of write protect in the SM.

e. Stack Protect Circuitry - A hardware stack protection mechanism providing 1M byte of usable stack space allocated in combinations of 256 4K stacks or 512 2K stacks.

f. Hardware ESR - This register is intended to capture hardware-related errors reported by various check circuits. Each error may be masked by a corresponding bit in its mask register. Any unmasked error that occurs will set the hardware error bit in the reset source register.

g. Software ESR - This register is intended to capture software-related errors reported via hardware check circuits. Each error may be masked by a corresponding bit in its mask register. Any unmasked error will set the software error bit in the reset source register.

h. Memory ESR - This register reports errors in the DRAM and may be masked by setting the corresponding bit in its mask register. Unmasked errors will set the MEM error bit in the hardware error source register.

i. C-Stat 1 & 2 - These registers provide information about the status of the controller.

j. Sanity Timer - The sanity timer provides an integrity check to insure sanity of the SM.

k. I/O Timer - The I/O timer is used to provide a degree of protection of the I/O registers.

l. Reset Source - This register aggregates errors in the system that result in processor resets (level 7 NMI).

m. Bus Control Register & Shadow BCR - The BCR is used to enable critical operations in the processor.

n. NMI Interrupt - This circuitry priorities and collects processor resets.

o. Power Monitor - This circuit provides signal distribute points to display unit status indicators and scan points to report unit power status.

p. Response Circuit - The response circuit will detect invalid cycles and, if unmasked, set a bit in the software error source register.

2.15 C. Core Support 2 - UN517

The processor Core Support 2 provides the following functions for the SMP:

a. 10 ms Timer - provides a signal that indicates when 10 milliseconds of time has elapsed. It also provides a counter that indicates the number of 10 ms periods that have elapsed.

b. Miscellaneous Timer - provides a programmable timer that may be used for two specific purposes within SMP. The user may program the controller to generate an interrupt of any period of time. The second use of the miscellaneous Timer Circuit is to provide a clock for the DLI 2x4 switch to provide a clock during certain maintenance test states.

c. Billing Counter - provides a clock from which the time of day is generated as a stable billing clock.

d. Shadow Data Register - captures the full 32-bit System Data Bus for every non-cache bus cycle. If a hardware, software, or correctable bit error occurs during a bus cycle, then the Shadow Data Register is frozen on that bus cycle. This data remains frozen in the Shadow Data Register until the Reset Source Register is cleared of the hardware, software, or correctable bit error.

e. Shadow Address Register - captures the full 32-bit system address bus for every non-cache bus cycle. When a hardware, software, or correctable bit error occurs on a bus cycle, the contents of the Shadow Address Register is frozen. The contents remain in the Shadow Address Register until the Reset Source Register is cleared of all three errors.

f. Shadow Operations Register - captures the state of certain leads during every non-cache bus cycle. The data that it captures is information that pertains to the type of bus cycle that was taking place. Whenever a hardware, software, or correctable bit error occurs in the Reset Source Register, the contents of the Shadow Operations Register is frozen. The contents remain frozen until the Reset Source Register is cleared of these three errors.

g. Special Function Operational Register - provides bits that have a specific designated function associated with each one of them. Software will set the required bit and then, on the next data access bus cycle, that function will be performed. When a bit is set in the Special Function Operational Register, all interrupts and DMA activity are blocked until the special function occurs. The types of special functions that are provided are:

   i. mate processor operation,

   ii. local processor operation,

   iii. read of the write protect status,

   iv. update of the write protect status, and

   v. enable or disable of the write protect bits.

h. Special Function Maintenance Register - provides different bits that are used to check out the integrity of the error detection circuits within SMP. The types of

maintenance functions that are provided are:

i. test multiple response detection circuit,

ii. allow special maintenance functions to the external cache,

iii. allow checking of the data parity circuits,

iv. allow checking of the address parity circuits,

v. force sub-unit mismatch error,

vi. allow circuits to ignore bad parity, and

vii. allow the memory to start self test.

i. SMITS/DUS Test Interface - provides the necessary address, data, control, and status leads to a spare slot within the MCTU2. The two test circuits used are the Switch Module Integrated Test System (SMITS) and the DEMON Utility System (DUS). Neither of these test circuits will be connected directly to any of the SMP's internal busses.

j. EPROM - provides 128 Kbytes of non-volatile EPROM that is organized as 32K x 32 bits. Each byte will be protected by its own parity bit.

k. Interrupt Controller - provides twenty-four maskable interrupts that generate a level 4 interrupt to the CORE circuit pack. Of the twenty-four interrupts, sixteen are maintenance having the highest priority and eight are operational.

l. Write Protect Status and Control Register - provides a disable for the entire write protect circuit and indicates the status of the selected data block. Two other bits in this register are used to mask out CPI interrupts and to enable/disable the stack protect mechanism.

m. Stack Control Register - provides a detection and inhibit for any writes to the stack region of memory outside the active stack.

n. Cache Control Register - provides maintenance control of the external cache and the capability to disable/enable both the external and/or internal cache.

2.16 D. Application 1 - UN518

The processor Application 1 provides the following functions for the SMP:

a. DLI interface - provides the CORE access to the DLI registers. Each DLI failure group has a unique address range which can be accessed from either processor side. A processor's "A" flip-flop must be active and the DLI enable bit must be set for a processor to access a DLI. A "running" processor which attempts to access a DLI without it's "A" flip-flop being set will generate a DLI access error. All processor operations to the DLI require that the I/O timer be unlocked. The DLI/SMP interface is serial. The processor executes normal byte operations to DLI addresses, and a parallel to serial conversion is automatically performed by the APPL1 hardware.

b. Sub-Unit Interface - provides the communication path from the SMP to the sub-units resident in the MCTU2 (TSI, SP, CI, and PI). The sub-unit bus consists of sixteen bits of data and six bits of

address, plus parity for both data and address. Operations to the sub-units are 16-bit locked reads or writes. Byte operations over the sub-unit bus are not supported. Each of the eight sub-units receives its own select and wait to request additional time. The APPL1 board translates the sub-unit wait signals into the system-ready signal used on the system bus. The control signals read and write are distributed to all sub-units. If a sub-unit fails to release its wait lead, the processor will take a ready timeout. All sub-unit wait leads are captured in the sub-unit ready register at the end of each sub-unit cycle for examination following the processing of an error. A sub-unit mismatch error is generated if, during a sub-unit operation, two decoders decode a different sub-unit.

c. Message Time Slot (MTS) Interface - provides a cross-coupled interface to/from the DLI for communication to the Administrative Module (AM). The MTS interface includes 2 Intel 8273 Synchronous Data Link Controllers (SDLC), a DMA controller, and DMA map registers. The SDLCs interface to the DMA controller. The SDLCs control the data links using a protocol similar to X.25, while the DMA handles the transferring of the data directly between memory and the SDLC. Each DLI has two full duplex serial links to the SMP. A 2x4 switch is provided to allow any SDLC to be connected to either data link. The DLI switch register contains the configuration control for the switch. Only one SDLC may be connected to a data link at a time. An invalid switch error is generated if both SDLCs are connected to the same data link. Parity is generated and checked on each SDLC data link to facilitate diagnosis of the link. The SDLC devices have receive and transmit interrupts to the processor to simplify normal and abnormal message completion.

d. BooTStRapper (BTSR) Interface - provides a 192 Kbit/sec data interface from the AM for pumping the dynamic RAM on power-up or in full initialization situations. The BTSR interface provided by APPL1 consists of a PIDB interface, BTSR data assembler, data FIFO, a 9517 DMA controller and associated DMA map register, and BTSR control register. A block of pump data is immediately preceded by a header which contains initialization information for the block. Header information includes start code, starting address, block size, and a hash-sum check over the header. The header utilizes the first four 32-bit words of a pump block. The BTSR performs the following functions:

   i. assembly and DMA transfer of 32-bit words assembled from any subset of thirty-two PIDB channels,

   ii. detection of the start of a pump block,

   iii. FIFO buffering of incoming data with FIFO overflow indication,

   iv. generation of a single level 6 interrupt following the first four FIFO loads of a pump block, and

   v. diagnostic strobe point used to increment internal time slot bit counter for verification of correct PIDB synchronization.

e. The SMP pump function utilizes a cycle stealing implementation which allows the processor to execute code between transfers of pump data. The BTSR can be configured to pump the local, mate, or both SMP sides, providing complete flexibility for pump configurations.

f. DMA Interface - provides the MTS and the BTSR with a DMA interface for transfer data to and from SMP memory.

g. System Bus Interface - provides the module processor access to APPL1 internal registers and application interfaces. The System Bus is a non-multiplexed, 32-bit address, 32-bit data path bus.

2.17 E. Memory - TN1374/TN1376

The processor memory is contained on one to six TN1374/TN1376 circuit packs. The TN1374 contains 4M of memory while the TN1376 contains 8M. Each TN1374 memory circuit pack contains a 1M x 39 bit dynamic memory array. The TN1376 uses two 1M x 39 bit memory arrays. They both provide the following functions for the SMP:

a. A System Bus Control Interface - provides an interface to the System Bus control signals so that a bus cycle may be started and completed.

b. A System Bus Address Interface - allows the memory board to interface to the System Address Bus.

c. A System Bus Data Interface - provides the circuitry to allow the memory board to interface to the System Bus data leads.

d. Dynamic Memory Access Control - provides a 1 Mbit by 32-bit memory array, and the necessary control logic to access each 32-bit word. The System Bus Control Interface will provide the signals to begin the memory cycle. An arbitration and control circuit generates the necessary control signals to perform a memory access on a processor cycle or a memory refresh, and guarantees that all timing specifications for the DRAMs will be met. All dynamic memory cycles are read-modify-write cycles. Each dynamic memory board contains a refresh timer, which insures that refreshes occur at the specified rate to maintain good data.

e. Write Protect - allows the software to individually write protect each 1K block of RAM memory. RAM memory is defined as those addresses that fall within the range of 0x22000-0xFFFFFFF. The write protect functions that are performed on the individual RAM memory boards are:

i. provide a write protect bit for every 1K of memory that is equipped on a memory board,

ii. allow software to set or reset each write protect bit through the use of the Special Function Operational Register,

iii. allow software to read the status of each write protect bit through the use of the Special Function Operational Register,

iv. block the write cycle from taking place if this RAM location is write protected, and

v. disable the write protect checking function when the "Disable Write Protect" lead from the controller portion of

write protect is active. The writes are allowed and no errors are generated. This is only true for RAM memory.

f. Error Detection and Correction - uses a modified Hamming scheme (seven bits) to provide data integrity by allowing single-bit error correction and double-bit error detection. The seven Hamming check bits are stored in dynamic RAM along with the corresponding data word. On every dynamic memory access, the check bits are read to determine if an error has occurred. Each RAM board may be placed in "Correct-on-the-Fly" mode, where data words are corrected before they are sent to the system bus on a read. Normally, however, error detection and correction occurs after the data has already been sent to the system bus.

g. I/O Accesses

h. Diagnostic Self Test - provides a diagnostic self test to test every memory location. The self test will perform several passes through memory under diagnostic software control. For example, an 8-bit data pattern is written to the memory array. Then the memory array is read and compared to the original data pattern.

3. DUAL LINK INTERFACE - TN1077B

3.01 The Dual Link Interface (DLI) function consists of one circuit pack per MCTU2 side and provides an interface to the NCT links. The DLI recovers clock and data from incoming NCT links and distributes the resultant clocks and data to the MCTU2. In the opposite direction, the DLI receives outgoing data from the MCTU2. The outgoing data is then multiplexed and sourced to outgoing NCT links. In each SM, two DLIs operate in a master/slave (active/standby) configuration.

3.02 The DLI consists of two Link Interface (LI) circuits: a clock circuit and a control circuit. Each LI interfaces with one pair of NCT links (outgoing and incoming) that provide 256 time slots to and from the SM. Of these 256 time slots, 255 are for voice and data paths to and from the MCTU2 and the remaining time slot is reserved for communications between the AM and the SMP. (This time slot is referred to as the message time slot.) The incoming 32.768 megabit/second data stream from the NCT link enters the receive (RCV) circuitry in the LI where it passes through a clock recovery circuit that derives a 32.768MHz clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the Phase Lock Loop (PLL) in the clock circuit. The RCV circuit "frames up" on the incoming data stream via a pseudo-random sequence inserted into the data stream at the source end of the NCT link. The incoming data stream is then converted to time slots and written into a buffer circuit (a RAM capable of containing one frame of data).

3.03 The TSI interface and message interface operate from clocks derived from the output of the PLL. When time slots are read from the buffer, parity is checked and regenerated. Normal voice and data time slots are sent to the duplex TSIs via nibble busses operating at 8.192 megabits/sec. The message time slot is sent to both the active and standby sides of the SMP via serial data links to the Synchronous Data Link Controller (SDLC). These data links operate at 48 kilobits/sec. The message time slot select switches (955B) provide the capability to select one of 256 time slots as the message time slot for NCT links A or B. When

the MCTU2 is in a Remote Switching Module (RSM) environment, these switches are removed and the message time slot is selected by SMP software. However, in a minimally equipped RSM (two T1 lines), the switches are not removed, but the message time slots are forced to zero and one.

3.04 In the return direction, data is selected from one of the TSIs at the TSI interface and from one side of the SMP at the message interface for transmission to the TMS via the outgoing NCT link. These time slots are then multiplexed to provide a full frame of 256 time slots. In the transmit (XMIT) circuit, parity is checked and regenerated. The pseudo-random framing sequence that is generated in the control circuit is inserted (one framing bit per-time-slot). Finally, the time slots are converted to a 32.768MHz data stream and transmitted over the outgoing NCT link.

3.05 The clock circuit selects a clock reference from one of the two LIs (master mode) or from the mate DLI (slave mode). This selected clock is used as a reference for the PLL which, in turn, provides a reference voltage to the Voltage Controlled Crystal Oscillator (VCXO). The output of the VCXO is a 32.768MHz clock that is divided by the clock circuit and distributed to the remainder of the DLI, mate DLI, TSI, and SMP.

3.06 The control circuit provides control for the various functions performed by the LIs and clock circuit. Errors from these circuits are latched into error source registers (ESRs) that reside in the control circuit. These control registers and ESRs are accessible for writing and reading by either side of the SMP via the SMP-DLI control interface. This interface is a 1.875MHz serial data link. The data bits that make up the commands are clocked in by the SMP, and the command is executed on the reception of a "go" signal received over a separate lead from the SMP. Parity over address and parity over data are checked in the control circuit. The control circuit provides a serial data link back to both sides of the SMP for read operations and an interrupt lead back to both sides of the SMP to indicate that an error condition exists. Each bit of the ESR can be inhibited from causing an interrupt via ESR mask registers.

3.07 Each DLI is in a failure group separate from the rest of the MCTU2 and is powered by a board-mounted power module (984A). The power converter will interface to the control and display functions that are integrated onto the TN1077B. In an RSM environment, the DLI will also include the Facilities Interface Unit (FIU) in its service group. In an Optically Remote switching Module (ORM) environment, the DLI will also include the Transmission Rate Converter Unit (TRCU) in its service group.

4. TIME SLOT INTERCHANGER/SIGNAL PROCESSOR - TN1086

4.01 The Time Slot Interchanger/Signal Processor function consists of one circuit pack (TN1086) per MCTU2 side that incorporates both the TSI and SP functions. An overview of the TSI/SP operation is presented here.

A. TSI

4.02 The primary data path delivers 512 peripheral time slots from the DIs to the RCV TSI RAM to be stored in consecutive order. Time slots are then translated from the RCV RAM and can be delivered to both DLIs on any of the 512 network time slots. In the opposite direction, 512 network time slots from the DLIs are written consecutively into the XMIT TSI RAM.

Time slots are then translated from the XMIT RAM, on chosen peripheral time slots as instructed under software control, and delivered to the DIs. Any peripheral time slot written into the RCV TSI RAM can be read out onto multiple (up to all) network time slots toward the DLIs. The same fanout capability is provided by the XMIT TSI RAM. A maximum delay in each direction of one frame (125us) can be introduced by the TSI.

4.03 Two DIs are connected to the TSI: one is dedicated to even TSI time slots, and one is dedicated to odd TSI time slots. Each DI provides 256 time slots to the RCV TSI RAM. Sixteen-bit time slots in nibble format are sent to the TSI by the DIs (PCM, A-G, and parity).

4.04 The TSI transmits 16-bit time slots in nibble format to the DIs. Of the A-G bits sent to the DIs, the E-G bits can either be sourced from the SP or from the alternate data RAM in the TSI. The A, B, C, and D bits can either be sourced from the SP or passed through from the XMIT TSI RAM. All PCM data sent to the DIs passes through the Attenuation ROM. The attenuation ROM allows one of thirty-one values of digital loss to be inserted in the PCM data path on a per-time-slot basis. The loss values are 0dB through 15dB in 0.5dB increments. The integrity of the data path (TSI to peripheral unit to TSI) is protected by a walking parity scheme, administrated by the TSI, that inverts the parity sense of every ninth TSI time slot.

4.05 The TSI receives 512 time slots from the DLI via two 256-time-slot nibble busses. The TSI selects which DLI (side 0 or 1) is the source of time slots to the TSI. This is accomplished by AUtomatic TIme Slot Switching (AUTISS), that allows the TSI to switch its network data source on a per-time-slot basis between the active and standby sides of the system based on a validity marker (E-bit signaling stream) in each time slot. If AUTISSing occurs for 256 consecutive frames, the TSI outputs a 125us pulse that can be used to alert system software to the switching activity.

4.06 The TSI transmits 512 time slots toward both DLIs in the MCTU2. The time slots consist of sixteen bits in nibble format. The E bit of each time slot sent to the DLIs is set on a per-time-slot basis via a TSI control RAM written by SMP software. The A-D bits of each time slot sent toward the DLIs are either passed through from the RCV TSI RAM or sourced from a TSI control RAM.

4.07 Two forms of connections are possible between the XMIT and RCV RAMs. The first connection allows intramodule paths to be set up by looping time slots on the DLI side of TSI memories. A connection of this type will block an incoming time slot from the DLIs. The other connection allows intra-DLI connections to be made. A connection of this type will block an incoming peripheral time slot from reaching the RCV TSI RAM, but the blocked peripheral time slots will still have access to the SP and LDSU.

4.08 The Alternate Data RAM (ADR) provides the SMP and LDSU with access to the contents of all 512 time slots. By means of the ADR, the SMP can write constants (e.g., idle code) to be sent to the DIs and DLIs, and to sample time slots at various points within the TSI. The ADR also provides SMP access to the E bits received from the DLI. Parity errors on time slots received by the TSI from the DIs are reported to the SMP via the ADR. Data stored in the ADR (e.g., tones from the LDSU) can be sent to the DIs, to the RCV TSI RAM, or to the XMIT TSI RAM. The TSI time slots written to the ADR

can be sourced on a per-time-slot basis from four different locations in the TSI. This permits maintenance access and allows time slots from both DIs and DLIs to be sent to the LDSU.

B. SP

4.09 The SP performs hit timing on all signaling and control bits received from the TSI. This hit timing is performed by scanning the data at a 3 ms rate. .A time slot is considered to have changed to a new state only if the bit persists in that state for two consecutive scans.

4.10 Hit timing is accomplished by comparing data on the incoming selected TSI time slot with data contained in the Last Look RAM (LLR). The LLR contains the values of signaling and control bits from the selected TSI time slot during the previous 3 ms scan. Every 3 ms, all 512 time slots are hit-timed, and if a bit has remained the same for two consecutive three-ms scans, it passes the hit timing algorithm.

4.11 The state of all signaling and control bits received by the SP from the TSI are stored after hit timing in the Last Report RAM (LRR). Through the LRR, the SMP has access to the most recent hit timed state of all signaling and control bits of all time slots received by the TSI from the peripheral units, and all signaling and control bits whose state, after hit timing, has changed. The SP is also capable of storing (in an SMP-readable FIFO) the peripheral time slot number.

4.12 State change calculations are based on the result of the hit timing circuit, the ignore RAM, and the LRR. The ignore RAM, set by SMP software, indicates on which bits of which time slot state change reports should be made. The LRR contains previously calculated states of all signaling and control bits after hit timing. If a new time slot bit has passed the hit timing algorithm, i.e., has not changed during the last 3 ms, it is compared to the state stored in the LRR. If a change has occurred, the LRR is updated. If the bit being processed is not set to the ignore RAM and if there is a change from the state contained in the LRR, the new bit value is written into the report FIFO. All changes for one time slot are collected before the FIFO is written. The FIFO is readable by the SMP.

4.13 The signaling and control bits (A, B, C, D, E, F, and G) are transmitted to the TSI for all 512 peripheral-side time slots every 125us. These signaling bits are read from a 512 time-slot RAM designated as the M RAM. The M RAM is both writable and readable by the SMP.

C. TSI-SP Interface

4.14 The TSI sends the seven signaling bits (A-G) of all 512 time slots received from the DIs to the Signal Processor. The time slots consist of two consecutive 4-bit nibbles and are accompanied by an 8.192-MHz clock and a 6-ms sync pulse. In the opposite direction, the TSI receives the seven signaling bits (A-G) from the SP for all 512 outgoing peripheral time slots. The TSI has the ability to send the E, F, and G bits from either the ADR or the SP to the DIs. The A through D bits are selectable as a group. They can either be passed through the TSI from the DLI or can be selected to be sourced by the SP. Even parity is used on the even time slot bytes, and odd parity is used on the odd time slot bytes.

5. DATA INTERFACE - TN1377/TN1524

5.01 The Data Interface (DI) function consists of two circuit packs per MCTU2 side and provides an interface between the TSI and various peripheral units in the SM. In a u-Law application, the TN1377 circuit pack is used. In an A-Law application, the TN1524 will be used in place of TN1377. This circuit pack is identical in function, with the only difference being that it sources a different idle code bit pattern.

5.02 In the incoming direction, the DI performs a multiplexing function by combining time slot traffic of several peripheral units onto a single bus for the TSI. In the outgoing direction, it demultiplexes a single bus from the TSI to various peripheral units. The DI communicates with each peripheral unit over a Peripheral Interface Data Bus (PIDB). Each of these busses consist of four signals: serial data in, serial data out, a 4.096MHz clock, and an 8KHz sync. The data in and out operate at 4.096 megabits/second, carrying thirty-two time slots per frame, with sixteen bits per-time-slot. Up to sixteen PIDBs may be connected to the DI, with each PIDB carrying traffic to a service group in one of the peripheral units. The DI passes data to and from the TSI over nibble busses. These busses operate at 8.192 megabits/second carrying 256 time slots per 125us frame (two DIs, each connecting 256 TSI time slots, are needed to carry traffic for the 512-time-slot TSI). With 512 peripheral side time slots (16 PIDBs x 32 time slots) and 256 TSI side time slots, the DI can perform a 2:1 concentration function. All PIDBs operate in synchronization. In the time of a single PIDB time slot, eight time slots are sent and received from the TSI. After a single time slot from all sixteen PIDBs has been clocked into the DI, up to eight of those are chosen (via control information received from the TSI) to be inserted into eight time slots to the TSI. The time slots not selected are blocked and lost. If less than eight are chosen, "1s" are sent on the nibble bus to the TSI in the time slots for which no PIDB time slot was connected.

5.03 In the outgoing direction, the TSI provides eight time slots to the DI during a single PIDB time slot period. These eight time slots are connected, again using control information received from the TSI, to eight of the sixteen PIDBs. PIDBs not selected to receive TSI data transmit idle code to peripheral units. All eight TSI time slots need not be connected to a PIDB time slot. If less than eight are to be connected to PIDBs, the control information from the TSI associated with the "unused" TSI time slots informs the DI to ignore that incoming time slot. All unselected PIDBs transmit idle code. In this case, more than eight will do so.

5.04 In addition to the nibble bus in and out of the DI from the TSI, the DI also receives from the TSI an 8.192MHz clock, an 8KHz sync pulse, four address leads, a board select lead, and two leads used for diagnostics. The 8.192MHz clock provides all the timing for processes internal to the DI; it is also used to generate the 4.096MHz clock for the peripheral units. The 8KHz sync pulse properly synchronizes the DI to the network and generates the sync pulse to peripheral units. The address leads indicate, on a per-time-slot basis, to which PIDB a given TSI time slot is to connect. The address is used by the DI for both the TSI-to-PIDB demultiplex function, and the PIDB-to-TSI multiplex operation. The board-select lead informs the DI, again on a per-time-slot basis, whether to connect the TSI time slot to the PIDB, as

determined by the address, or to ignore that time slot and make no connection to it. The diagnostic leads are used to loop data received from the TSI through the DI circuit and back to the TSI. These leads also provide the capability of having the DI loop idle code back to the TSI rather than the received TSI data. Maintenance of the DI, as well as of the PIDB and parts of the peripheral units, is performed by the TSI by means of the walking parity scheme.

6. CONTROL INTERFACE - UN71B

6.01 The Control Interface (CI) function consists of one or two circuit packs per MCTU2 side and provides an interface between the SMP and various peripheral units for control information. This interface is called a Peripheral Interface Control Bus (PICB). Up to twenty-three PICBs are available with each CI. Either one or two CIs may be equipped in the MCTU2, thereby providing a maximum of forty-six PICBs. Each PICB contains five twisted-wire pairs that carry clock, output data, input data, SMP select information, and peripheral unit service requests.

6.02 The CI to SMP interface is through the Sub-Unit Interface Bus (SUIB). This bus is a parallel, sixteen-bit bidirectional data bus with a six-bit address bus. The CI contains several registers that are accessible by the SMP through this bus. The CI performs four functions for the SMP:

a. permits the SMP to write sixteen bits of information to a peripheral unit register (maximum of 256 destination registers),

b. permits the SMP to read sixteen bits of information from a peripheral unit register (maximum of 256 source registers),

c. receives, latches, and reports service requests from peripheral units, and

d. detects and reports CI operational errors.

6.03 The CI reads and writes peripheral registers through an exchange of serial messages over the PICB. A distribute operation writes sixteen bits of data into a peripheral unit destination register. A scan operation reads sixteen bits of data from a peripheral unit source register.

6.04 The SMP will initiate all scan and distribute operations. In all scan and distribute operations, the peripheral unit will send a reply message back to the CI. In the reply message there is a three-bit All Seems Well (ASW) code. These bits are used to report errors detected by the peripheral unit. If errors are detected during a scan or distribute order by either the CI or a peripheral unit, the error will be reported by latching a bit in the error source register. The interrupt lead to the SMP will become active if an error occurs; the ability to inhibit this interrupt on a per-PICB basis is provided.

6.05 In addition to performing scan and distribute orders, the CI reports peripheral unit service requests by latching an active state on the PICB interrupt lead into the interrupt source registers. Inhibit registers (remote interrupt inhibit registers) are provided such that these service requests may be handled by interrupts or polling.

7. PACKET INTERFACE - TN1042

7.01 The Packet Interface (PI) function consists of one circuit pack per MCTU2 side and provides an interface between the SMP and the

Packet Switch Unit (PSU). The PSU implements Integrated Services Digital Network (ISDN) capabilities on the 5ESS Switch. The main function of the PI is to buffer signaling packets between the PSU Protocol Handlers (PHs) via the Packet Bus (PB) and the SMP via the SUIB.

7.02 Resident on the PI is circuitry that interfaces to the SUIB and a Port Processor (PP), which transmits and receives packets between the SMP and PHs. The PP design is common to the PI and PH. The signaling packets are FIFO buffered in a 1M byte dual-port memory of the PP circuitry. The PP controls Port A of the dual-port memory and transfers the signaling packets across the PB. Port B of the dual port memory transfers signaling packets to and from the SMP over the SUIB.

8. DIGITAL SERVICE CIRCUIT - TN833

8.01 The Digital Service Circuit (DSC) function consists of one circuit pack per MCTU2 side and provides tone decoding, tone generation, voice path assurance and other features. The Digital Service is implemented on one circuit called the Digital Service Circuit (DSC). Four slots in the MCTU2 are reserved for DSCs; each position represents a service group with the ability to provide a combination of all of these features. Initially, only two service groups will be used; one in each shelf of the unit. The other two spaces are reserved for use in the event that future additional features provided by the Digital Service Function would require a larger number of resources. The Digital Service Function operates in a load-shared configuration, rather than in an active-standby mode. This means that each in-service board will handle a portion of the load. If two boards are active and one of these should fail, the capacity to perform Digital Service features is decreased by fifty percent.

8.02 Each service group has a separate interface to the TSI and the CI. The interface to the TSI is via the LDSU Bus (LDSUB). This interface is functionally the same as a PIDB. However, the data on the LDSUB has direct access to the TSI and does not pass through the DI. Data, typically PCM tones, and signaling bits are transmitted in both directions over the LDSUB, while clock and sync are only transmitted to the LDSU. The interface to the CI is through a standard PICB. It carries the control and status information for the board and also provides the path used to download the resident software from the SMP to the DSC.

8.03 The Digital Service is one of many functions which may be overlaid on the flexible architecture of the DSC. The major functional components of the design are:

a. Logical Processor (LP),

b. memory,

c. Unified Control Interface (UCI),

d. Serial Data Interface (SDI), and

e. Digital Signal Processor (DSP).

8.04 The DSC may be viewed as a multi-processor system where the LP, an Intel 80188, provides the logical control for the board and orchestrates the actions of the DSPs. The architecture of the DSPs is particularly suited to the tasks of performing the algorithms needed to provide digital services. The LP determines what jobs need to be accomplished, typically per a request from the SMP, then configures the DSPs to fulfill those requests. The LP is also responsible for performing audits

and checks of both the hardware and software on the board.

8.05 The LP executes programs stored in 256K bytes of DRAM while the DSPs execute programs out of 4K bytes of on-chip RAM. The DRAM address range is divided into four write-protectable regions. On memory writes, parity is generated over seven bits of address and eight bits of data, and is stored in a single 256K x 1 DRAM. When the data is read from the memory, the parity is again generated and then checked against what had previously been stored. Parity and write-protect errors are reported to the SMP and the LP through the UCI.

8.06 The primary function of the UCI is that of a control interface. It provides error reporting and communication between the DSC and the SMP through the PICB. It is the source of interrupts to the SMP for peripheral service requests. This is accomplished through several maskable sources contributing to a single summary scan register. The summary scan register is sixteen bits wide; eight bits request normal service and eight bits indicate detected errors. It includes mailboxes and FIFOs for message passing. The mailbox consists of a RAM and a set of maskable mailbox flags. Using these, the SMP may communicate bi-directionally with the LP in a synchronous manner. The FIFOs consist of two FIFO controllers used to read and write first-in-first-out buffers in the UCI RAM. This provides asynchronous communication between the SMP and the LP. A fault insertion register is provided for maintenance.

8.07 Two SDI devices are used on the DSC. The SDIs are essentially micro-time-multiplexed-switches. They provide the interface between the DSC and the TSI through the LDSUB. They provide data paths between the DSPs and the TSI. The SDIs transmit and receive thirty-two time slots of data from each DSP and the TSI. The column of multiplexers responsible for switching the data is controlled by an internal RAM which is accessible only to the LP. When the LP assigns a DSP to a task it must be able to direct the data to or from that DSP.

8.08 The DSC performs complex functions as a whole, but it may be viewed as a set of individual pieces, each performing a more specific and straight-forward task. There is a control processor, a set of number-crunching DSPs, a bank of memory and its associated control, and, finally, the control and data interfaces.

9. POWER CONTROL

9.01 One power control (PWRCTRL) function is contained per MCTU2 side and provides a common +5 volt controlled power supply for the SMP, CI, DI, TSI/SP, and PI functions. The PWRCTRL function is contained on the 414AA Power Converter and the Control & Display circuitry contained on UN516.

A. Power Converter - 414AA

9.02 The purpose of the converter is to provide a means of converting nominal -48 volt input to a well regulated and isolated +5 volt output for applications in the MCTU2 circuitry. The power units are pulse width controlled for regulation, self-oscillating, and operate at a fixed frequency. The unit is also self-protected by several types of alarms. The 414AA provides +5 volts at 400 watts to the SMP, TSI/SP, DI, CI, and PI functions in the MCTU2.

B. Control & Display - Implemented on UN516

9.03 The UN516 provides the following control & display functions:

a. The human interface allows an operator to power on, power off, request a unit either in service or out of service, and manually override momentarily.

b. Alarm display allows the operator to read the status of the power circuits by observing a Light Emitting Diode (LED) display that indicates the following:

OFF — A red LED, when lit, indicates that power is off.

ALM — A red LED, when lit, indicates a power fault on the unit fuse or converter alarms. Note that in the alarm state, all power may not be off in the unit. Once an operator powers down the unit for repairs, the OFF LED will light and the ALM LED will extinguish.

OOS — A yellow LED, controlled by the system, is lit whenever the unit is Out Of Service (OOS).

RQIP — ReQuest In Progress (RQIP). A green LED, controlled by the system, lights whenever a request to restore or remove a unit has been received by the system. If this request is denied, the LED will flash for 5 to 10 seconds.

ROS — A green LED lights whenever the ROS/RST switch is in the Request Out of Service (ROS) position.

c. Converter control interface allows the human interface and software interface to control the power converter.

d. Software Interface - all 5ESS units will require some interface between their power and the system software. This interface is in the form of scan points to report alarms and signal distributor points to light status LEDs (OOS, RQIP).

10. EXTERNAL INTERFACES

10.01 In SD-5D151-01, external interfaces consist of cables connecting MCTU2 functions to other 5ESS equipment and are referenced as CAD 1 with individual element identifiers.

A. Craft Intervention Interface

10.02 This interface is used when the MCTU2 is used in an RSM or an ORM environment. The element identifiers DP and HH of CAD 1 are the interconnections between the SMP and the Multi Module RSM (MMRSM) alarm and status unit (ED-5D586-10). The MMRSM alarm and status unit allows the following user operations of the SMP:

a. force either side of the SMP active,

b. monitor the status of communication between the Remote Modules and the host by indicating the state of the links between them, and

c. monitor the status of the SMP by indicating the current state of sanity in each processor.

B. DLI Control and Display Interface

10.03 In an RSM environment, the FIU will become part of the DLI service group via cables installed at the locations specified in element identifier AO and EG of CAD 1.

10.04 In an ORM environment, the TRCU will become part of the DLI service group via cables installed at the locations specified in element identifier AO and EG of CAD 1.

10.05 In an SM environment, 982JJ shorting bergs will replace these cables to provide a path from the DLI converter back to its control and display functions.

C. DLI Fuse Alarm Interface

10.06 The DLI fuse alarm interface consists of signals between the DLI alarm circuitry, FFU, and the CS1 circuit pack of the SMP. The interface is used to monitor blown fuses. When a DLI 70-type indicator fuse is blown, the fuse connects -48 volts to a signal used to light a red alarm LED on the FFU, on the cabinet bezel, and on the DLI circuit pack. The DLI alarm circuitry informs the SMP of the fuse alarm through two scan points. The SMP monitors the scan points and will take appropriate recovery actions if they become active. The SMP can test continuity of the DLI fuse alarm circuitry and its connection to the FFU through a combination of three distribute points. The element identifiers in CAD 1 for DLI fuse alarms are AP and EH.

D. Revertive Pulsing Interface

10.07 If the SM is equipped for revertive pulsing, the DSC circuit packs are removed from the MCTU2 and a Digital Service Unit (DSU) is installed in the SM. The MCTU2 DSC slots are cabled to the DSU. The element identifiers in CAD 1 for DSU cabling are AE, AF, AG, AH, DW, DX, DY, and DZ.

E. Fan Unit Scan and Distribute Interface

10.08 A fan failure is reported to the SMP through a scan point from the Six-Fan Unit to the CS1 circuit pack. When a fan fails, a scan lead becomes active and is used to light a red alarm LED on the Six-Fan Unit and a yellow alarm LED on the cabinet bezel. The SMP monitors this scan point and will take appropriate recovery actions if the scan point becomes active. A fan alarm can be retired by SMP software using a distribute point, or manually by a push button located on the rear of the Six-Fan Unit. The Six-Fan Unit scan and distribute interface appears in element identifier DR and HJ of CAD 1.

F. MCTU2 Controller Fuse Alarm Interface

10.09 The controller fuse alarm interface consists of signals between CS1 alarm circuitry and the FFU. The interface is used to monitor blown fuses. When an MCTU2 controller 70-type indicator fuse is blown, the fuse connects -48 volts to this signal, which is used to light a red alarm LED on the FFU, on the cabinet bezel, and on the CS1 circuit pack. The mate SMP monitors the scan points and will take appropriate recovery actions if they become active. The SMP also monitors fuse alarms from peripheral units through a Z scan point. The SMP monitors the Z scan point and will take appropriate recovery actions if it becomes active. The SMP can test continuity of the MCTU2 controller and peripheral fuse alarm circuitry, and its connection to the FFU through a combination of three distribute points. The element identifiers in CAD 1 for controller fuse alarms are DQ and HI.

G. Peripheral Interface Data Bus (PIDB)

10.10 A PIDB provides the physical link for PCM data between the DI and any connected peripheral unit. It consists of four balanced, differentially driven, RS422[3] compatible, twisted wire pairs. The PIDB cable may vary in length, but it has a maximum limit of 20 ft.

10.11 The PIDB carries 4.096 megabit/second serial data from the DI to the peripheral units, a 4.096MHz clock and 8KHz sync to the peripheral units, and 4.096 megabit/second serial data to the DI from the peripheral units. The twisted pair carrying data from the periphery is terminated at the DI.

10.12 The 4.096MHz clock has a 244-ns period. The duty cycle of the clock, excluding this ±20 ns is 50% ±5%. The 8KHz sync is a normally high signal ("1" state) that pulses low for one 4.096MHz clock period every 125us. The peripheral units should clock PIDB data in from the DI on the falling edge of the 4.096MHz clock, and clock data out onto the PIDB on the rising edge of that clock.

10.13 During the sync pulse, the peripheral should clock PIDB time slot No. 29, bit 7 in from the PIDB on the negative edge of the 4.096MHz clock, and clock out PIDB time slot No. 31, bit 15 onto the PIDB using the positive edge of the clock. Note the 2 1/2 ns time slot skew between incoming and outgoing information. This is caused by the skew required by the TSI and DI to perform their functions.

10.14 A peripheral unit service group will receive a PIDB from each side of the duplex MCTU2. In a fully operational SM, data will flow over both PIDBs. Using control information received from the SMP via the CI, the peripheral unit will select only one PIDB from which to receive information. However, it will transmit the same data back over both PIDBs. The skew of the two PIDB clocks received from the duplex SM can be up to ±60 ns.

10.15 The elements identifiers of PIDB interfaces in CAD 1 are: AQ, AR, AS, AT, AU, AV, AW, AX, AY, AZ, BA, BB, BC, BE, BF, BG, BH, BI, BJ, BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU EI, EJ, EK, EL, EM, EN, EO, EP, EQ, ER, ES, ET, EU, EV, EW, EX, EY, EZ, FA, FB, FC, FE, FF, FG, FH, FI, FJ, FK, FL, and FM.

H. Peripheral Interface Control Bus (PICB)

10.16 A PICB consists of five balanced, differential driven, RS422 compatible, twisted pairs. The clock pair carries a 2.048MHz gated clock signal to the peripheral units. The data out pair carries serial information to the peripheral units from the CI. The data in pair carries serial data from the peripheral units to the CI. The select pair carries signaling information which is used to select the active side CI, and the interrupt pair transmits service requests from the peripheral units to the CI.

10.17 Although the cable length of the PICB may vary, it has a maximum limit of 20 ft. Data is to be gated in and out of the peripheral unit on the negative edge of the clock. To avoid a timeout error, the reply must be received by the CI within 21.5us from the first clock pulse.

---

3. Electronic Industries Association (EIA) RS-422 standards for balanced voltage digital interfaces.

10.18 The elements identifiers of PICB interfaces in CAD 1 are: BX, BY, BZ, CA, CB, CC, CE, CF, CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CR, CS, CT, CU, CV, CW, CX, CY, CZ, DA, DB, DC, DE, DF, DG, DH, DI, DJ, DK, DL, DM, DN, DO, FP, FQ, FR, FS, FT, FU, FV, FW, FX, FY, FZ, GA, GB, GC, GE, GF, GG, GH, GI, GJ, GK, GL, GM, GN, GO, GP, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, HA, HB, HC, HE, HF, and HG.

I. Packet Switch Unit Interface

10.19 The Packet Bus (PB) is a duplexed bus connecting the PI to the PSU. The PB consists of the following six differentially balanced signals:

a. Clear To Send,

b. Transmit/Receive Data,

c. Request To Send,

d. Receive Clock,

e. Transmit Clock, and

f. Carrier Sense.

10.20 The PB operates at 10 Mbits/s and allows PSU to communicate with the PI. The receive clock is continuously sent from the PSU. If the PI is sending a packet to the PSU, the PI will issue a request to send. The PSU responds by sending carrier sense and clear to send. If the PSU is transmitting to the PI, the PI responds by sending carrier sense. The element identifiers of the PSU interface in CAD 1 are: BV, BW, FN, and FO.

J. DLI-TRCU Interface

10.21 This interface is used when the MCTU2 is in an ORM environment. The four NCT links between the TRCU and the DLIs are implemented with a short (less than 2 feet), shielded, twisted-pair cable.

10.22 The NCT to D3 Rate Converter (NDRC) circuit pack in the TRCU produces an 8KHz reference signal by dividing down the incoming 45 MHz clock. This signal is sent to the DLI to be used as a reference for its phase locked loop. Each of the four NDRC circuit packs provides an 8KHz reference signal with only one being selected by the two DLIs. In the NDRC circuit pack, those references not selected are synchronized to the reference that is selected.

10.23 Two leads from its associated DLI provide an indication to an NDRC circuit pack of whether its reference has been selected as the phase locked loop input. One of these leads indicates whether a particular DLI is master or slave, and the other indicates whether the A or B link is being used as a reference.

10.24 The NDRC circuit pack also produces an out-of-frame output. This output indicates whether the NDRC circuit pack can frame up on the incoming 45 Mb/s signal. This signal is sent to the DLI, where it is used to force the phase locked loop to free run if the 8KHz signal to which it is locking is produced by a clock derived from a bit-stream that the NDRC circuit pack can not frame up on. The power control and display function for the power converters in the TRCU is provided by the power control and display circuitry in the DLI's.

K. Fiber Optic NCT Link Interface

10.25 This interface is used when the MCTU2 is in an SM, TRM, or RSM environment. The serial data received and transmitted over the NCT links is at a 32.768MHz rate. The DLI will track the received serial data up to ±1KHz of the nominal frequency (±32 PPM). Each frame consists of 256 sixteen-bit time slots. Bits 0 through 7 are PCM data bits in the 255 voice

and data time slots. Bits A through E are signaling bits. The G bit is the bit position into which the pseudo-random framing sequence is inserted. The F bit is toggled at the beginning of each frame and is used for fault detection in the DLI-TMS interface. The P bit is such that the sixteen bits of the time slot have odd parity. In the message time slot, bits 0 through 5 are the data bits that contain data to or from the SMP; bit 7 is the CPI bit.

10.26 The fiber optic NCT links for the SM and RSM appear in element identifier HK, HL, HM, HN, HO, HP, HQ, HR, HW, HX, HY, and HZ of CAD 1. The fiber optic NCT Links for the Two Mile Optically Remote Switching Module (TRM) appear in element identifier HS, HT, HU, and HV of CAD 1.

L. Unit Power Interface

10.27 All power for the MCTU2 is connected to the FFU by means of -48 volt feed and a -48V return (ground potential). Power feed and return lugs appear in element identifier XX and YY of CAD 1.

M. Ground Lugs

10.28 Ground connections between the two backplanes of the MCTU2 appear in element identifier WW of CAD 1.

11. INTERNAL INTERFACES

11.01 In SD-5D151-01, internal interfaces consist of backplane wiring and/or cables between the two backplanes of the MCTU2. All cross-coupled interfaces (signals between side 0 and 1) are connected through CAD 2.

A. SMP Memory Interface

11.02 Each SMP memory board receives a dynamic memory base address from the backplane and knows its own size, so that it is capable of determining which address range is located in SMP memory on this board during RAM accesses. The boards compute a "next base address" by adding the size to the base address. This "next base address" is passed on the backplane to the next memory board as its base address. The first memory board will receive all zeros from backplane grounds as its next base address. Each memory board also receives a four-bit board address, which it uses to determine the addresses of the I/O registers located on the board.

B. SMP Sub-Unit Interface Bus

11.03 The Sub-Unit Interface Bus (SUIB) is used as the SMP control interface to the sub-units (TSI, SP, CI, PI). The SUIB is not cross-coupled to both MCTU2 sides. It utilizes a sixteen-bit bidirectional data bus and a six-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two bidirectional parity leads, one each for the low byte and high byte of data. The parity is computed such that the sum of bits set to a logic one in each byte (including the parity bit) is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

11.04 The SUIB has five control leads. Two of these, the read and write signals, are shared by all sub-units. These two signals distinguish between read and write operations to a sub-unit and are used by the selected sub-unit to gate the data to and from the data bus. The other three controls are board select, ready, and interrupt.

Each individual sub-unit has separate board select, ready, and interrupt leads. The board select lead enables the desired sub-unit, the ready lead allows the sub-unit to extend the SMP bus cycle for sub-units with slower response time, and the interrupt lead allows the sub-unit to interrupt the SMP. In addition, the CIs receive a lead called NAE that is used to force the select wire pair in the PICB on the non-active side to a nonconductive state.

C. SMP-DLI Message Interface

11.05 The SMP-DLI message interface consists of two cross-coupled 48 kilobits/sec X.25 message links and a Central Processor Intervention (CPI) link.

11.06 The message time slot is extracted from the NCT link by the DLI, and parity is then generated over the six bits of data. The generated parity and message time slot data is sent to the Synchronous Data Link Controller (SDLC) in both sides of the SMP over separate data leads. At the same time, the Central Processor Intervention (CPI) bit is sent to the CPI gate arrays in both sides of the SMP. Two clocks are sent to both sides of the SMP from the clock circuit in the DLI. These clocks are used by the SMP to clock the received message time slot data and parity into the SDLCs. In the return direction, the SMP uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each DLI contains a message interface to and from both sides of the duplex SMP.

D. SMP-DLI Control Interface

11.07 The SMP controls the DLI through a cross-coupled interface and consists of six signals. A module processor active lead originates from the SMP to indicate which side is sending commands to the DLI. A module processor read/write lead comes from the SMP to control when a read or write command is executed by the DLI. A 1.875MHz clock is sent by the SMP along with serial data that specifies the command to be executed. The entire write operation is specified in a serial sixteen-bit command in which the first eight bits contain the data to be written, followed by a spare bit and a parity bit for the eight bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four address bits that specify the register to be written. During a read operation, only six bits are sent by the SMP to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits that determine the register to be read. Following the execution of the read command, as initiated by the module processor go signal, eight bits of data plus one parity bit (parity over the data) are sent back to both sides of the SMP on separate signal leads with the results of the read operation. An interrupt lead indicating that error conditions exist in the ESRs of the DLI are also a part of the SMP-DLI control interface. The interrupt signal is asynchronous to the SMP and has no specified timing relationship.

E. TSI-DLI Interface

11.08 The TSI and DLI interface with one another through cross-coupled four-bit nibble buses. The TSI transmits the 512 time slots to both DLIs in the MCTU2. In the opposite direction, the TSI provides a switch, set under SMP control, to select 512 time slots from one of the two DLIs. This provision allows the TSI to be configured to receive its time slots from the active DLI, and, under normal (no fault) conditions, to switch

between the two DLIs on a per-time-slot basis without introducing data errors. The interface consists of two 256 time slot busses to and from each DLI. Each bus transmits sixteen-bit words made up of four consecutive four-bit nibbles. The parity bit is set such that the sum of bits (including parity) set to a logic one is odd. Each DLI supplies the TSI with an 8.192-MHz clock, an 8KHz sync pulse, and a 6 ms sync pulse in addition to data. The TSI is required to perform an error-free switch when selecting a DLI timing source. To accomplish this switch, the maximum DLI clock skew between the duplicated DLIs can not exceed 20 nsec.

F. TSI-DI Interface

11.09 The interface between the TSI and the DI consists of a nibble bus in each direction carrying call traffic, control information from the TSI to the DI, clock, and sync. The TSI-DI interface is not cross-coupled to both MCTU2 sides.

11.10 Two DIs are connected to the TSI, each supplying 256 time slots in nibble format. The nibble busses carry a time slot on four consecutive nibbles and operate at 8.192Mbits/sec; 256 time slots per frame are transmitted in each direction to each DI. These busses use a walking parity scheme for fault detection. In this scheme, the parity is normally odd, but in every ninth time slot, the parity is even.

11.11 The control information includes a four-bit PIDB address that selects the source and destination for the 512 time slots associated with the DIs and a DI board select lead. This lead tells the DI to connect the TSI time slot with which it is associated to the specified PIDB, or to ignore the time slot and make no PIDB connection to it.

11.12 Two additional leads are used to diagnose the DI. One lead informs the DI to loop the TSI data received on that time slot through itself and back to the TSI on the same time slot of the next frame. The other lead directs the DI to replace the received TSI data with PIDB idle code.

11.13 The clock lead nominally is an 8.192MHz clock (122 ns period). The 8KHz sync is a normally "high" signal with an active "low" pulse of one 8.192MHz period in duration occurring every 125us (once per frame).

G. TSI-DSC Interface

11.14 The TSI-DSC interface is cross-coupled between side 0 and 1 of the MCTU2. The TSI transmits and receives thirty-two serial time slots to and from each DSC service group. Any of these sixty-four time slots can be selected as a source of PCM data for any time slot going to the DLIs or DIs. Similarly, the TSI can send the sixteen-bit word of any time slot received from the DLIs or DIs out on any of the sixty-four time slots to the local DSC. The data format and timing of the local DSC interface is of the PIDB type, consisting of four balanced, differentially driven, RS-422 compatible, twisted-pair wires. Signals provided by this interface are a 4.096MHz clock out, an 8KHz sync pulse out, thirty-two-time-slot serial output data, and thirty-two-time-slot serial input data.

H. Unit Test Interface

11.15 This interface is used when the MCTU2 is in a unit or lab test environment. The MCTU2 contains two circuit pack slots used for testing. These slots may be powered from the +5 volt MCTU2 power converter or from an external source connected to the unit by backplane lugs.

11.16 The test slot in side 0 is used for unit test or software testing, depending on what type of circuit pack is present. The DEMON Utility System (DUS) pack (UN514) is used during unit hardware testing. The SM Integrated Test System (SMITS) pack (TN889) is used during software testing. Use of SMITS permits a user to examine and modify the execution of a program. SMITS accommodates step-by-step execution of target programs, the setting of breakpoints, and the running of error detection programs. Additional test cables are required when using DUS or SMITS.

11.17 The test slot in side 1 accommodates the Communication Link Monitor (CLM) and is used for hardware and software testing of the communication path between the MSGS and the SMP. Additional test cables are required when using CLM.

I. DLI Time Slot Select Switch Interface

11.18 Each DLI has two message time slot registers for the A and B NCT links. Each message time slot register has two modes of operation: software programmable and backplane programmable. The backplane programmable mode is selected by plugging 955B message time slot select switches onto the MCTU2. The backplane switches ground the message address enable lead, allowing the switches to indicate an eight-bit binary number corresponding to the NCT link time slot used for transmitting messages to and from the SMP and AM. After the switches are removed, the address enable lead is pulled high and the message time slot number can be programmed by the SMP writing to the message time slot address registers of the DLI.

11.19 When the MCTU2 is in a Remote Switching Module (RSM) environment, these switches are removed and the message time slot is selected by SMP software. However, in a minimally equipped RSM (two T1 lines), the switches are not removed, but the message time slots are forced to zero and one.

J. Wiring for PI Growth

11.20 If required in future applications, the MCTU2 contains a spare slot in each shelf for an additional PI circuit pack. This circuit pack slot contains identical wiring to the first PI slot, and is connected to the SUIB.

K. Wiring for DSC Growth

11.21 If required in future applications, the MCTU2 contains a spare slot in each shelf for an additional DSC circuit pack.

12. UNIT LAYOUT

12.01 The MCTU2 is considered to be a single-shelf unit containing two versions of backplanes (ED-5D649-30 and ED-5D650-30). It functions as a duplexed entity, with two units required, each with a different backplane code. Side 0 is contained in the lower shelf. Side 1 is contained in the upper shelf. ED-5D649-30 and ED-5D650-30 have been updated from issue G2AB to G3AB to provide for new features and options. G2AB requires manual wiring options for use with an ASU and for equipping a UN520. In the G3AB backplane, the manual wire options are eliminated and are provided in printed wire.

12.02 Equipment locations for all component codes in the MCTU2 are shown below.

EQL	FDESIG	COMPCODE
04-012	(0,1)PWRCONV	414AA
04-026	(0,1)CS1	UN516
04-034	(0,1)CS2	UN517
04-042	(0,1)CORE	UN515/UN520
04-050	(0,1)MEM1	TN1374/UN1376
04-058	(0,1)MEM2	TN1374/UN1376
04-064	(0,1)MEM3	TN1374/UN1376
04-070	(0,1)MEM4	TN1374/UN1376
04-076	(0,1)MEM5	TN1374/UN1376
04-082	(0,1)MEM6	TN1374/UN1376
04-088	(0,1)APPL1	UN518
04-096	(0,1)C10	UN71B
04-104	(0,1)CI1	UN71B
04-112	(0,1)PI	TN1042
04-130	(0,1)DI0	TN1377 or TN1524
04-138	(0,1)DI1	TN1377 or TN1524
04-144	(0,1)TSI/SP	TN1086 or TN1086B
04-156	(0,1)DLI	TN1077B
04-168	(0,1)DSC	TN833
01-156R	(0,1)OPTRCVB	982CG
03-156R	(0,1)OPTXMTB	982CF
07-156R	(0,1)OPTRCVA	982CG
05-156R	(0,1)OPTXMTA	982CF
02-156R	(0,1)OPTB	982WY or 982TS
06-156R	(0,1)OPTA	982TA or 982TR
07-155R	(0,1)MTSSWA	955B
05-155R	(0,1)MTSSWB	955B

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The voltages used are:

a. +5±0.5 volts and

b. -48 volts +4.5, -6.25 volts.

1.02 Ambient Temperature Limits are:

a. 0° to 70° Centigrade at circuit pack and

b. 0° to 50° Centigrade (office aisle ambient).

1.03 Growth:

With the basic unit equipage, each side of the MCTU2 contains thirty-two PIDBs and twenty-three PICBs. The unit may be expanded by adding another CI to each side, for a total of forty-six PICBs per side.

2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for all component codes in the MCTU2 are shown below.

FDESIG	MEANING	COMPCODE
(0,1)PWRCONV	POWER CONVERTER	414AA
(0,1)UNITTST	UNIT TEST TERMINAL FIELD	- - -
(0,1)CS1	CORE SUPPORT 1	UN516
(0,1)CS2	CORE SUPPORT 2	UN517
(0,1)CORE	CORE	UN515/ UN520
(0,1)MEM1	MEMORY BOARD 1	TN1374/ TN1376
(0,1)MEM2	MEMORY BOARD 2	TN1374/ TN1376
(0,1)MEM3	MEMORY BOARD 3	TN1374/ TN1376
(0,1)MEM4	MEMORY BOARD 4	TN1374/ TN1376
(0,1)MEM5	MEMORY BOARD 5	TN1374/ TN1376
(0,1)MEM6	MEMORY BOARD 6	TN1374/ TN1376
(0,1)APPL1	APPLICATION 1	UN518
(0,1)CI0	CONTROL INTERFACE 0	UN71B
(0,1)CI1	CONTROL INTERFACE 1	UN71B
(0,1)PI	PACKET INTERFACE	TN1042
(0,1)PIGRTH	PI GROWTH TERMINAL FIELD	- - -
(0,1)DI0	DATA INTERFACE 0	TN1377 or TN1524
(0,1)DI1	DATA INTERFACE 1	TN1377 or TN1524
(0,1)TSI/SP	TIME SLOT INTERCHANGER/SP	TN1086

FDESIG	MEANING	COMPCODE
(0,1)DLI	DUAL LINK INTERFACE	TN1077B
(0,1)DSC	DIGITAL SERVICE CIRCUIT	TN833
(0,1)DSCGRTH	DSC GROWTH TERMINAL FIELD	- - -
(0,1)OPTRCVB	SM/RSM FIBER OPTIC RCV B	982CG
(0,1)OPTXMTB	SM/RSM FIBER OPTIC XMIT B	982CF
(0,1)OPTRCVA	SM/RSM FIBER OPTIC RCV A	982CG
(0,1)OPTXMTA	SM/RSM FIBER OPTIC XMIT A	982CF
(0,1)OPTB	TRM FIBER OPTIC XMIT/RCV B	982WY
(0,1)OPTA	TRM FIBER OPTIC XMIT/RCV A	982TA
(0,1)AFIBOPT	FIBER OPTIC TRANSCEIVER	982TR
(0,1)BFIBOPT	FIBER OPTIC TRANSCEIVER	982TS
(0,1)MTSSWA	MESSAGE TIME SLOT SWITCH A	955B
(0,1)MTSSWB	MESSAGE TIME SLOT SWITCH B	955B
TF	TERMINAL FIELD	- - -
LUG	POWER/GROUND LUG	- - -

3. FUNCTIONS

3.01 The function of this unit is described in Section II of this Circuit Description.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on an application schematic, the connecting information thereon is to be followed.

4.02 The main connecting circuits are:

a. Time Multiplexed Switch Unit - SD-5D043-01,

b. Time Multiplexed Switch Unit 2 - SD-5D061-01,

c. Six-Fan Unit - SD-5D081-01,

d. Fuse/Filter Unit - SD-5D053-01, and

e. Multi Module RSM MMRSM Alarm and Status Unit - ED-5D586-10.

4.03 The peripheral units are:

a. Line Unit - SD-5D051-01,

b. Line Unit 2 - SD-5D032-01,

c. Line Unit 3 - SD-5D180-01,

d. Trunk Unit - SD-5D300-01,

e. Digital Carrier Line Unit - SD-5D203-01, SD-5D202-01,

f. Integrated Services Line Unit - SD-5D091-01,

g. Packet Switch Unit - SD-5D074-01,

h. Digital Line and Trunk Unit - SD-5D201-01,

i. Digital Line and Trunk Unit Export - SD-5X204-01,

j. Metallic Service Unit - SD-5D033-01,

k. Modular Metallic Service Unit - SD-5D015-01,

l. Digital Service Unit - SD-5D035-01,

m. Digital Service Unit 2 - SD-5D092-01,

n. Digital Service Unit Export - SD-5X201-01,

o. Remote Clock Unit - SD-5D075-01,

p. Facilities Interface Unit - SD-5D401-01,

q. Transmission Rate Converter Unit - SD-5D086-01,

r. Switching Transmission Facilities Unit - SD-5D167-01,

s. Directly Connected Test Unit - SD-2P077-01, and

t. Echo Canceler #5 Signaling Unit - SD-5X213-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 For manufacturing testing requirements, refer to SPECIFICATION (X-80222) Manufacturing Test Requirements For Module Controller And Time Slot Interchange Unit, Model 2 (J5D003LA).

6. REFERENCES

6.01 Supplementary information is contained in the following documents:

a. Switching Module Control Cabinet, Model 2 - CD-5D160-01,

b. CPSM-414AA,

c. CPSM-UN71B,

d. CPSM-UN515,

e. CPSM-UN516,

f. CPSM-UN517,

g. CPSM-UN518,

h. CPSM-UN520,

i. CPSM-TN833,

j. CPSM-TN889,

k. CPSM-TN1042,

l. CPSM-TN1077B,

m. CPSM-TN1086,

n. CPSM-TN1088,

o. CPSM-TN1374,

p. CPSM-TN1376,

q. CPSM-TN1377, and

r. CPSM-TN1524.

7. ACRONYMS

ADR	Alternate data RAM
ALM	Alarm
AM	Administrative module
APPL1	SMP application 1 circuit pack
ASW	All seems well
AUTISS	Automatic time slot switching
BTSR	Bootstrapper
CAD	Cabling and distribution
CI	Control interface
CLM	Communication link monitor
CORE	SMP core circuit pack
CP	Central processor
CPI	Central processor intervention
CS1	SMP core support 1 circuit pack
CS2	SMP core support 2 circuit pack
DI	Data interface
DLI	Dual link interface
DMA	Direct memory access
DRAM	Dynamic random access memory
DSC	Digital service circuit
DSP	Digital signal processor
DUS	Demon utility system
EIA	Electronics industry Association
EPROM	Erasable, programmable, read-only memory
ESR	Error source register
FIFO	First in, first out
FIU	Facility interface unit
FFU	Fuse/filter unit
I/O	Input/output
ISDN	Integrated services digital network
LDSU	Local digital service unit
LED	Light emitting diode
LI	Link interface

LLR	Last look RAM
LRR	Last report RAM
LP	Logical processor
MEM	SMP memory
MCTU2	Module controller time slot interchange unit, model 2
MPF	Mate power fail
MSGS	Message switch
MTS	Message time slot
MPERR	Mate parity error
MUPEN	Mate update enable
NCT	Network control and timing
NDRC	NCT to D3 rate converter
OOS	Out of service
ORM	Optically remote switching module
PB	Packet bus
PCM	Pulse code modulation
PH	Protocol handler
PICB	Peripheral interface control bus
PIDB	Peripheral interface data bus
PLL	Phase lock loop
PP	Port processor
PPM	Parts per million
PI	Packet interface
PSU	Packet switch unit
PWRCTRL	Power control
RAM	Random access memory
RCV	Receive
ROM	Read-only memory
ROS	Request for out of service
RQIP	Request in progress
RSM	Remote switching module
SDI	Serial data interface
SDLC	Synchronous data link controller
SM	Switching module
SMITS	Switching module integrated test system
SMP	Switching module processor
SP	Signal processor
SUIB	Sub-unit interface bus
TMS	Time multiplexed switch
TRCU	Transmission rate converter unit
TRM	Two-mile optically remote switching module
TSI	Time slot interchanger
UCI	Unified control interface
VCXO	Voltage controlled crystal oscillator
XMIT	Transmit

AT&T BELL LABORATORIES

DEPT 55422-DPD-JCB