5ESS® SWITCHING EQUIPMENT TIME MULTIPLEXED SWITCH UNIT MODEL 3 CIRCUIT

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1. GENERAL DESCRIPTION

This section provides a high-level view of the time multiplexed switch unit model 3 (TMSU3).

1.1 PURPOSE OF CIRCUIT

The TMSU3 provides the physical paths which carry data and control messages between the switching modules (SMs) and the administrative module (AM). Major functions of the TMSU3 are to:

(1) Provide a fixed control path between the AM and its associated SMs.

(2) Provide switched data paths between the SMs which are connected to the time multiplexed switch (TMS).

(3) Provide for clock distribution to the SMs by transmitting data timed from a clock which is derived from a switch.

(4) If equipped with quad link (QLPS), provide for inter-SM 2000 communication on variable size ports.

1.2 GENERAL DESCRIPTION OF OPERATION

The TMSU3 is connected to SMs (both SM 2000 and non-SM 2000) through the network control timing (NCT) links which terminate on the foundation link interface (FLI) board or the quad link interface (QLI or QLI2) boards. The FLI and QLI boards terminate NCT links, while QLI2 boards terminated NCT2 links). For clarity, the FLI, QLI and QLI2 circuit packs will be referred to in this document as link interface (LI) boards.

Data from the SMs is buffered by the LIs before being sent to the shelf utility board (SUB) where it is multiplexed up to a 64 Mbit rate and placed on the emitter coupled logic bus (E-Bus). The E-Bus distributes clock and data signals to and from all switch units in the TMS.

Data received from the E-Bus is switched through the fabric board multiplexers and routed back to the appropriate LI board. The LI checks the data for errors and sends it out to a receiving SM through the NCT links.

2. DETAILED DESCRIPTION

The TMSU3 is wired to accept the following circuit packs:

CIRCUIT PACK	DESIGNATION	QTY
SN516B	CONTROL & DISPLAY	1
495CA	-2 VOLT POWER	1
410AA	-5 VOLT POWER	2
TN883	FOUNDATION LINK INTERFACE	1/0
TN888	QUAD LINK INTERFACE	7/8
UN182	SHELF UTILITY BOARD	1
KBN5	CRFABRIC	1
TN1681	QUAD LINK INTERFACE 2	7/8
TN1682	QUAD LINK PACKAGE SWITCH	0/1/2/3/4

The TMSU3 is divided into five circuit elements with the control paths described in Element A. Element B details the clock distribution. Data distribution is explained in Element C and power distribution in Element D. Element E describes the QLPS.

2.1 ELEMENT A: CONTROL

COMMUNICATIONS

The TMS controller resides in the CMCU and interacts with each TMSU3 through the SUB (UN182). Communications with the switch unit are accomplished through the use of the control interface chip (CIC) which converts the parallel address and data buses from the processor, to serial address and data streams. These serial streams are distributed through the E-Bus to the SUB located in each TMSU3. The SUB is responsible for distributing the serial address and data to the switch unit. Serial data returning from the switch unit flows in exactly the opposite direction with the SUB collecting the serial streams from each circuit pack before sending data back to the controller. A multiplexer on the SUB selects which serial stream from all the various circuit packs is to be sent back to the controller. Control for the SUB multiplexer originates at the TMS controller and is derived from the address that the controller wishes to read.

ERROR REPORTING

Error reporting of TMSU3 is accomplished asynchronously through a pyramid error reporting architecture. Errors are reported to the controller in the form of an error summary lead from each circuit pack. The SUB serves as the collection center for these summary errors and produces a *switch unit error summary* used to interrupt the TMS controller and invoke its error handling routines. When an error is detected, the TMS firmware will search through the error reporting hierarchy in hopes of finding the source of the interrupt.

FABRIC CONTROL

Control for the TMS fabric multiplexers is not provided directly by the TMS controller, but rather by the KBN5 circuit pack. The TMS controller sends connection information to the KBN5 board, which in turn configures the fabric multiplexers located on the LI circuit packs on a per time-slot basis.

SHELF SELECT

Since a fully grown TMS contains 12 TMSU3s, a shelf select bus is used to identify the address range of each shelf. The bus is tied to all of the circuit packs on the shelf that perform address decoding and allows for the high-level decoding to be dependent on the state of the leads in the shelf select bus. A programming paddle-board located behind equipment location (EQL) 173 determines the state of the shelf select bus and thus determines the shelf identification. With the high-level address decoding performed by the shelf, not by the circuit pack, TMS circuit packs can be moved between shelves while only maintaining their "base" addresses.

2.2 ELEMENT B: CLOCK

All clocks used in the TMSU3 originate from the E-Bus. The clocks themselves are designated as either "receive" or "transmit", depending upon whether they are being used to clock data onto or from the E-Bus.

Receive clocks are used by the LIs to send received data from the SMs to the SUB and onto the E-Bus. As with the case of serial address and data, the LIs acquire their receive clocks from the SUB board, which serves as a distribution point. A secondary function of the receive clock is to clock the incoming serial address and data streams from the TMS controller. It is for this reason that the KBN5 board is also supplied with versions of the receive clock. The transmit clock and sync pulses are used to recover data from the E-Bus and send it through the fabric and LIs toward the designated SM. The KBN5 fabric board receives a transmit clock directly from the E-Bus. The KBN5 fabric board relays the transmit clock and sync to the LIs.

2.3 ELEMENT C: DATA

Data is also divided into groups of receive and transmit, depending upon whether the data is moving towards or from the E-Bus.

Data from the SMs is received at the LI circuit packs from the NCT/NCT2 links. A link interface receiver (LIR) function (which resides in a custom device) buffers the incoming data before it is sent across the backplane to the SUB. The SUB contains a 2:1 data multiplexer *(not to be confused with the previously mentioned control multiplexer)* which combines LIR data streams before distribution on the E-Bus.

The E-Bus distributes the data *(as well as clock and sync)* throughout the TMS so that all switch units have access to the received data. Once the TMS fabric has received the data from the E-Bus, it is then deemed *transmit* data.

Transmit data is routed through the fabric board multiplexers and is sent to an LI. Data switched through fabric chip 0 on the fabric board is destined for LI 0 - LI 3. Likewise, data switched through fabric chip 1 is destined for LI 4 - LI 7. The data is then checked for errors by the QLT function (in a custom device), before being sent to the corresponding SM.

2.4 ELEMENT D: POWER

The emitter-coupled logic (ECL) used in the TMSU3 necessitates the -5 volt and -2 volt power be available throughout the shelf. Also, due to the large power draw by each circuit pack *(approximately 40 watts)*, two -5 volt supplies are needed. Power distribution is implemented using two power groups that allow a minimal equipage of the switch unit to require only one -5 volt supply. Power Group A operates up to four LIs *(equivalent to 14 SMs)* before requiring the second 410AA power supply.

-2 volts is available from a single 495CA supply capable of driving the entire shelf.

2.5 ELEMENT E: QLPS

The quad link packet switch (QLPS) is a special case of data transport. Functionally, it provides a message pipe for SM 2000 to SM 2000 communication. Together with quad link gateway processor (QGP) it also provides for SM 2000 to AM, and SM 2000 to classic SM communication. The QLPS has the same link interface to the TMSU3 as do the LI boards, and can reside in any QLI/QLI2 slot. In addition, it has four QGP ports which are cabled to the communication module control unit (CMCU) to the appropriate QGPs. QLPS is an optional feature, and there can be 0, 1, 2, 3, or 4 boards in a unit depending on the switch configuration.

Inter-SM 2000 data comes into the TMS through NCT2 links connected to QLI2s. This data leaves QLI2 and is routed through the fabric to a QLPS. The QLPS transfers this transmit data to a receive clock and then routes it according to the destination field in the data frame. The frame leaves the QLPS and is routed once again through the fabric to the QLI2 which connects to the destination SM 2000. SM 2000 to AM or non-SM 2000 communication goes from the SM 2000 to the QLPS as describe above and is then routed to one of the four QGP ports on the QLPS. The QGP then sends the packet to the AM/SM through the message switch. See the message switch control unit (MSCU) circuit description (CD).

3. ADDENDUM

Up to this point, the TMSU3 has been described on a functional basis.

4. REFERENCE DATA

4.1 WORKING LIMITS

None.

4.2 FUNCTIONAL DESIGNATIONS

AM	Administrative Module
CMCU	Communication Module Control Unit
CPF	Circuit Pack Function
CPS	Circuit Pack Schematic
E-Bus	Emitter Coupled Logic Bus
NCT	Network Control Timing
TMS	Time Multiplexed Switch
TMSU3	Time Multiplexed Switch Unit Model 3
SM	Switching Module

4.3 CONNECTING CIRCUITS

The circuits connected directly in the TMSU3 are as follows:

E-Bus
- Shelf Utility Board
- CRFabric Board

TSIU
- Quad Link Interface Boards
- Foundation Link Interface Boards

CMCU
- Foundation Link Interface
- Shelf Utility Board
- Control and Display Pack

5. ACRONYMS

CD	Circuit Description
CIC	Control Interface Chip
ECL	Emitter-Coupled Logic
EQL	Equipment Location
FLI	Foundation Line Interface
LI	Link Interface
LIR	Link Interface Receiver
MSCU	Message Switch Control Unit
QGP	Quad Link Gateway Processor
QLI	Quad Link Interface
QLPS	Quad Link Packet Switch
SUB	Shelf Utility Board

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