5ESS® SWITCHING EQUIPMENT INTEGRATED SERVICES LINE UNIT 2 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. ABSTRACT

1.01 The information in these notes are considered AT&T - Proprietary and to be used pursuant to Company Instructions. The Integrated Services Line Unit 2 (ISLU2) is a peripheral unit on the 5ESS exchange that provides up to 1024 subscriber lines and may be mixed between analog and Integrated Services Digital Network (ISDN) lines. The unit provides low traffic capacity when fully equipped with 1024 lines (particularly with ISDN lines). Actual equipage should be based on customer traffic engineering requirements. The Remote-ISLU2 (RISLU2) is used to remote Plain Old Telephone Service (POTS) and ISDN lines via 1.544 Mb/s or 2.048 Mb/s digital transmission facilities. The ISLU2 uses Fastech N-sized (8.5 by 13 inch) circuit packs with eight lines on each pack. This allows room for additional line circuit functionality and reduces the cost of complex components or PWB layouts. Additional line circuit functionality includes on-board Periodic Pulse Metering (PPM) and Network Termination 1(NT1) remote powering. PPM is used to control pay telephones or home charging meters in many countries. ISLU2 analog (Z) line packs support reverse battery PPM and 12 kHz or 16 kHz tone PPM in the various countries that require them. The Fifty Hertz Periodic Pulse Metering Unit (FPPMU) works with the 12 kHz or 16 kHz tone PPM line packs to provide 50 Hz PPM to countries that require it. The NT1 remote powering functionality allows the digital (U) line pack to remotely power the NT1 at the customer premise. This is desired internationally because the NT1 is considered part of the exchange and is maintained by the telecommunication company.

2. COMPARING (R)ISLU2 to (R)ISLU

2.01 The (R)ISLU2 hardware architecture is based in large part on the hardware architecture of the existing (R)ISLU. ISLU2 differs from ISLU in the following key areas:

(a) ISLU2 can support a maximum of 1024 lines, twice as many as ISLU. The line circuits are partitioned into sixteen line groups. Each line group can be equipped with up to sixty-four lines, as compared to the thirty-two lines per line group maximum for ISLU.

(b) In ISLU2, all line group circuitry is implemented on N-sized circuit packs that are equipped in shelves, eliminating the drawer hardware and smaller KCB and KCD packs used in ISLU. In the present design, eight line circuits are implemented on each pack. Line Group Control (LGC) and Line Group Power (LGP) functionality is distributed across the associated line packs. There are no separate LGC and LGP packs.

(c) ISLU2 has redesigned Common Data (CD) circuit packs supporting a modified Line Interface Data Bus (LIDB) architecture, sixty-four lines per line group, and distributed LGC function.

(d) New Common Control Processor (CCP) and Common Control Interface (CCI) circuit packs are used in ISLU2. The ISLU2 CCP will have a more powerful microprocessor and more RAM than the CCP for ISLU. The ISLU2 CCI supports the Common Control (CC) processor bus structure. It also has an additional Control Sequencer (CS) device that will be used in implementing control capabilities for handling up to sixty-four lines per line group.

(e) A Metallic Access Network (MAN) circuit pack is used in the ISLU2. The metallic access structure implemented using the MAN pack supports the following enhanced capabilities:

- A sparing architecture that provides less degradation in ringing and metallic testing capabilities when sparing is active, as compared to ISLU;

- Cleaner metallic test access paths containing no active components and the ability to insert or remove additional capacitance;

- Metallic access that supports testing at Digital Subscriber Line (DSL) transmission signal frequencies;

- The ability to metallically isolate line packs from access buses for improved fault sectionalization.

(f) An Enhanced High Level Service Circuit (EHLSC) circuit pack is also used in ISLU2. The EHLSC includes capabilities for generating and measuring relatively low level signals in the 0-20 kHz band. These capabilities support the testing of 12 kHz and 16 kHz PPM circuitry on Z-packs and signals diagnostic access to a Fifty Hz PPM Unit (FPPMU).

The EHLSC also supports earth-backed ringing capability.

(g) ISLU2 uses a wider shelf that is capable of supporting thirty-two Fastech circuit packs on 3/4 inch centers.

(h) The U-DSL line pack (U-pack) developed for ISLU2 international applications will support NT1 remote powering and U interface activation/deactivation.

(i) Analog line packs (Z-packs) with on-board 12 kHz and 16 kHz PPM circuitry are developed for ISLU2 international applications.

(j) 50 Hz PPM capability is also provided by a unit external to ISLU2. This unit, designated the FPPMU, converts 12 kHz or 16 kHz signals on the analog interface from ISLU2 to 50 Hz PPM signals on the analog interface to the customer. The FPPMU functions autonomously and is not controlled by a Peripheral Interface Control Bus (PICB) to the SMP. The FPPMU per-line circuitry is diagnosable as part of the Z line circuit diagnostics, with diagnostic access triggered by signals from the EHLSC. The FPPMU common circuitry has Built In Self Test (BIST) capability.

In addition to the differences just cited, RISLU2 includes several capabilities for enhancing remoted operation. These enhancements include:

(a) Support for CCITT-compatible thirty-channel transmission facilities;

(b) The ability to remote the Modular Metallic Service Unit (MMSU) with the RISLU2 to provide improved metallic loop testing and alarming capabilities;

(c) Auto power restart capability, which provides for the automatic restoration of power to all RISLU2 circuitry following a power failure, without requiring craft intervention.

3. ISLU2 ARCHITECTURAL OVERVIEW

3.01 A simplified block diagram of the ISLU2 physical configuration is shown in Figure 1. The ISLU2 can be configured as either a three-shelf, four-shelf, or five-shelf unit. As a three-shelf unit, ISLU2 consists of a common shelf and either one line shelf and a plenum, or two line shelves. As a four-shelf unit, ISLU2 consists of a common shelf and three line shelves. As a five-shelf unit, ISLU2 consists of a common shelf and four line shelves.

The ISLU2 common shelf contains Common Control Processor (CCP), Common Control Interface (CCI), and Common Data (CD) circuit packs which control the flow of data and control information between the line circuits and the rest of the SM. There are two CCP/CCI pairs which form duplex Common Control (CC) service groups which operate in active/standby mode. There are two CD service groups, with two CD packs in each service group. The CD service groups may be operated in either active/active or active/standby modes.

The ISLU2 common shelf may also be equipped with zero through four Metallic Access Network (MAN) circuit packs, zero through two Ringing Generator (RG) packs, and zero through six Enhanced HLSC (EHLSC) packs. These circuit packs support metallic access to line circuits and subscriber lines for testing, ringing, and/or sparing. Different types of RG packs exist to serve the specific ringing and/or testing requirements for different markets. The number of MAN, RG, and EHLSC packs equipped in a unit are

engineered according to the different types of lines, number of each type equipped, and the amount of traffic anticipated.

In ISLU2, the line circuits are partitioned into sixteen line groups, with up to sixty-four lines in each group. From an exchange technician perspective, each line circuit in the unit is identified by a unique line group/line pack/line circuit designation. This designation is determined by the specific ISLU2 shelf and slot in which the line pack is plugged, and the relative position of the line circuit on the line pack. All of the line circuits equipped on a line pack are always the same type: U, T, or Z. Since lines are equipped eight lines per pack, hardware growth/conversion must be done on an eight line basis. Note also that although the line group control architecture will support up to sixty-four lines of any type, care must be taken when equipping ISDN line cards to ensure that a line group is not overloaded in terms of traffic capacity.

4. CONTROL AND DATA FLOW

4.01 A simplified block diagram of the ISLU2 control and data architecture is given in Figure 2. A diagram showing how the ISLU2 interfaces with the rest of the Switch Module (SM) is given in Figure 3.

Control information is passed between the CC and the Switching Module Processor (SMP) over Peripheral Interface Control Buses (PICBs) using a mailbox scheme. The PICBs carry control information transmitted in message bursts at a rate of 2.048 Mb/s.

Control information is passed between the CC and each peripheral circuit in the common shelf via Peripheral Control and Data Buses (PCADBs). PCADBs are 2.048 Mb/s buses which carry control information transmitted in message bursts. Each peripheral circuit has duplicated PCADB interfaces, one to each of the two CCs.

Line group control orders and status messages are passed over Control Interface Data Buses (CIDBs) between the CC and the two CD service groups. The CDs interface with Peripheral Interface Data Buses (PIDBs), which carry subscriber data between the ISLU2 and the SM Module Controller/Time Slot Interchanger (MCTSI). The CDs can also support Directly-connected PIDBs (DPIDBs), which carry packet-switched signaling information and subscriber data between the ISLU2 and the Packet Switch Unit (PSU).

Subscriber data carried on the PIDBs and line group control information carried on the CIDBs are combined within the CDs and passed over Line Interface Data Buses (LIDBs) between the CDs and line packs. In ISLU2, the LIDBs terminate at each line pack on the Eight-Line Controller (ELC).

The CIDB, LIDB, GIDB and (D)PIDB buses are all bidirectional 4.096 Mb/s serial time multiplexed buses. These buses are partitioned into thirty-two 16 bit time slots transmitted at an 8 kHz frame rate.

5. DATA HANDLING ARCHITECTURE

5.01 The ISLU2 data handling architecture is generally equivalent to that of ISLU. The only difference is the electrical configuration of the LIDB interface used in ISLU2 as compared to the LIDB interface in ISLU.

Data switching begins at the line circuit, where instructions carried in Control Time Slots (CTS) via the

CIDB/LIDB/GIDB path are used to read and write line circuit registers which specify the time slot assignments for customer data. There is no time slot interchange function within the ISLU2. Customer data assigned to a GIDB time slot at the line circuit will be transported in the corresponding time slot on the LIDB serving that line group. The CD packs in each service group implement a space division switch, connecting the LIDB time slots to corresponding time slots on the PIDBs.

Data can be placed in LIDB time slots to and from either or both CD service groups. As shown in Figure 4, each CD service group terminates a LIDB from each of the sixteen line groups in the unit and up to twelve PIDBs (six per CD pack). The CD space division switch reconfigures between each time slot interval. For a given time slot, any of the twelve PIDBs can connect to any of the sixteen LIDBs. Two or more PIDBs must not connect to the same LIDB during the same time slot.

The CDs can be configured to deal with the tradeoffs between traffic and reliability. For high reliability, one CD service group can be designated active, carrying all line group control and data information, while the other CD service group is in standby. If higher traffic capacity is wanted, both service groups may actively carry data. Control is always active/standby.

There are a total of sixty-four time slots in the LIDBs to each line group, thirty-two time slots from each CD service group. Two time slots in each LIDB carry line group control information only, which means only thirty time slots in the LIDB to each CD are available for data. If the CDs are run active/active, all of the data time slots in each LIDB may be used, for a total of sixty time slots per line group. If the CDs are run active/standby, only the LIDB to the active CD may actively carry data, limiting the number of available data time slots to thirty.

Assuming active/active CD operation, there are a total of 960 LIDB data time slots connecting the line circuits and CDs, and a total of 768 PIDB data time slots (twenty-four PIDBs times thirty-two time slots/PIDB) connecting the CDs to the rest of the SM. For active/standby CD operation, these total capacities are halved; there are 480 LIDB data time slots connecting the line circuits and CDs, and a total of 384 PIDB data time slots connecting the CDs to the rest of the SM.

Note that in RISLU2 applications, the CDs are always run active/standby. The total number of PIDB time slots connecting the CDs to the rest of the SM is further reduced by the relationship for mapping PIDB time slots into time slots carried over the transmission facilities connecting the RISLU2 to the host.

6. LINE GROUP CONTROL HANDLING ARCHITECTURE

6.01 The general structure of the ISLU2 line group control handling architecture is essentially equivalent to that for ISLU, except that the addressing capacity and effective bandwidth of the control bus fabric has been doubled to support up to sixty-four lines per line group and 1024 lines total, twice the maximum supported by ISLU.

In ISLU2, as in ISLU, the CC generates line group control orders and checks status by writing and reading contents of Control Sequencer (CS) Random Access Memory (RAM). The contents of the CS are hardware mapped into the transmit and receive time slots of the CIDBs,

which carry the line group control and status information between the CC and the CD. On the CD, transmit and receive time slots carrying control information are switched between the CIDBs and each of the LIDBs connecting to the line groups.

In ISLU, each CC has one CS device supporting one CIDB to each of the CD service groups. The CIDBs to the two CD service groups carry identical control information and implement a duplex control path. At each CD service group, the thirty-two CIDB time slots are mapped onto specific time slots on specific LIDBs in a fixed relationship. In general, two CIDB time slots are mapped onto two time slots on each of the sixteen LIDBs.

The LIDB time slots that carry control information are called Control Time Slots (CTS). Each CTS has a four-bit line circuit addressing capability and thus can be used to address up to sixteen circuits. The sixteen line circuits controlled by one CTS are often referred to as a control group. In ISLU there are two CTSs on each LIDB and sixteen LIDBs. Thus the line circuit addressing capability of the ISLU is limited to thirty-two lines per line group, 512 lines total.

The line circuit control capacity in ISLU2 is doubled over that of ISLU by providing an additional CS device on the CC and implementing a second CIDB to each CD service group. As in ISLU, the CIDBs to the two CD service groups will carry identical control information and implement a duplex control path. However, the sixty-four time slots on the two CIDBs to each CD service group provide the capability to support up to sixty-four line control groups, providing the ability to address up to 1024 line circuits, twice the number in ISLU.

To support this enhanced control capability, the LIDBs in ISLU2 are partitioned for control purposes such that four CTSs are provided to each line group. The four CTSs support four sixteen-line control groups, for a total of sixty-four lines per line group.

The ISLU2 LIDBs are electrically partitioned such that the four line packs in the lower and upper halves of each line group (line packs 0-3 and 4-7, respectively) are on separate buses. The LIDB connections to the line packs in the shelves below the common shelf are designated "A" LIDBs and denoted LIDB-A. The LIDB connections to the line packs in the shelves above the common shelf are designated "B" LIDBs and denoted LIDB-B. The four line packs served by an A or B LIDB are referred to as a LIDB group.

The CTSs on the A and B LIDBs to each line group are multiplexed on the CD and mapped into CIDB time slots, such that the time slots on one of the CIDBs, designated CIDB-A, are mapped onto CTSs on the LIDB-As to each line group, while the time slots on the other CIDB, designated CIDB-B, are mapped onto CTSs on the LIDB-Bs to each line group. With this multiplexing function, each LIDB group receives two CTSs, providing line circuit addressing capability for up to thirty-two lines, the maximum number of lines that can be equipped on the four packs in the LIDB group.

There is a fixed relationship governing how the thirty-two CIDB-A time slots are mapped onto specific time slots on specific LIDB-As and the thirty-two CIDB-B time slots are mapped onto specific time slots on specific LIDB-Bs. This relationship is equivalent to the mapping relationship

governing how CIDB time slots are mapped onto LIDBs in ISLU. The specific ISLU2 CIDB to LIDB CTS mapping relationships are summarized in the table below.

In general, the two CTSs on each LIDB (A or B) will be located in time slots n and n+16, where n is the number of the line group served by that LIDB. The CTSs are mapped into the same time slots on the A and B LIDBs serving the same line group. Thus LIDB-0A and LIDB-0B to line group 0, will have control information in time slots 0 and 16; LIDB-1A and LIDB-1B to line group 1 will have control information in time slots 1 and 17; and so on, up to LIDB-15A and LIDB-15B to line group 15, which will have control information in time slots 15 and 31;

The two CTSs in each of the A and B LIDBs control different groups of line circuits within the LIDB groups. The CTS on the lower time slot on each LIDB-A (i.e., time slot 0-15) controls the line circuits on line packs 0 and 1. The CTS on the higher LIDB-A time slot on each LIDB-A (i.e., time slot 16-31) controls the line circuits on line packs 2 and 3. Similarly, the CTS on the lower time slot on each LIDB-B controls the line circuits on line packs 4 and 5, and the CTS on the higher LIDB-B time slot controls the line circuits on line packs 6 and 7.

Note that with this control arrangement, since the two CTSs to each LIDB group within a line group are on the same two time slots, thirty time slots on each LIDB are available for data, as described in the previous section. Note also that the LIDBs are not partitioned for data; the data time slots are not functionally partitioned across the A and B LIDBs, but rather are shared across both LIDB groups in the line group. Partitioning the LIDBs for control is implemented using additional, relatively inexpensive, circuit components and taking advantage of functionality already present in the design of the CD service group. Partitioning the LIDBs for data purposes would require extensive redesign of custom integrated circuitry used on the CD packs.

TABLE 1. ISLU2 CIDB to LIDB Control Time Slot Mapping

CIDB-A Time Slot	LIDB-A to LG	LIDB-A Time Slot	Line Packs	CIDB-A Time Slot	LIDB-A to LG	LIDB-A Time Slot	Line Packs
0	0	0		16	0	16	
1	1	1		17	1	17	
2	2	2		18	2	18	
3	3	3		19	3	19	
4	4	4		20	4	20	
5	5	5		21	5	21	
6	6	6		22	6	22	
7	7	7	0 & 1	23	7	23	2 & 3
8	8	8		24	8	24	
9	9	9		25	9	25	
10	10	10		26	10	26	
11	11	11		27	11	27	
12	12	12		28	12	28	
13	13	13		29	13	29	
14	14	14		30	14	30	
15	15	15		31	15	31	

TABLE 1. ISLU2 CIDB to LIDB Control Time Slot Mapping (Continued)

CIDB-B Time Slot	LIDB-B to LG	LIDB-B Time Slot	Line Packs	CIDB-B Time Slot	LIDB-B to LG	LIDB-B Time Slot	Line Packs
0	0	0		16	0	16	
1	1	1		17	1	17	
2	2	2		18	2	18	
3	3	3		19	3	19	
4	4	4		20	4	20	
5	5	5		21	5	21	
6	6	6		22	6	22	
7	7	7	4 & 5	23	7	23	6 & 7
8	8	8		24	8	24	
9	9	9		25	9	25	
10	10	10		26	10	26	
11	11	11		27	11	27	
12	12	12		28	12	28	
13	13	13		29	13	29	
14	14	14		30	14	30	
15	15	15		31	15	31	

Figure 5 shows an example of the path for control and status messages passed between the CC and the line circuits in line group 0. Two LIDBs, one from each CD service group, interface with each line group. The CTSs in the two LIDBs to each line group implement a duplex control path and carry identical control information if both are enabled. At any time, the line group circuitry in each LIDB group listens to the two CTSs in only one LIDB. Upon reaching the line circuitry, CTS contents are decoded and generate hardware reads or writes of control and status registers.

7. LINE GROUP ARCHITECTURE

7.01 Each ISLU2 line group may be equipped with up to sixty-four line circuits. The line circuits are implemented on N-sized circuit packs. In the present design, each line card contains eight line circuits, and associated power and control circuitry. All of the line circuits on a line pack are of the same type: U, T, or Z. Line packs of different or similar type may be equipped in a line group in any combination and in any position sequence (with the exception of tip/ring cabling differences).

As noted previously, each line circuit in the unit can be identified by a unique line group/line pack/line circuit designation that is determined by the specific ISLU2 shelf and slot in which the line pack is plugged and the relative position of the line circuit on the pack.

In ISLU, the LIDBs use differential drivers and receivers to implement a point-to-point connection between the CD and LGC circuit pack. In ISLU2, the LIDBs use single-ended transmission and implement a point-to-multipoint (bused) connection between the CD and line packs. As discussed in the previous section, the ISLU2 LIDB is electrically partitioned such that the four line packs in the lower and upper line group halves are on separate buses. These buses are connected to the common shelf by separate cable assemblies.

For ISLU2, the line group control functions that were performed by the LGC circuit pack in ISLU have either been eliminated or partitioned along eight-line circuit boundaries and are implemented on each line pack by the ELC. Examples of functions implemented by the ELC include the control of resets to each of the line circuits on the pack and the accumulation of directed scan information. In general, each line pack within a line group functions independently; there are no control interactions or dependencies between packs. The only exception to this rule has to do with the ability to perform a LIDB loopback for diagnostic purposes.

The ELC interfaces with each line circuit on the line card via the GIDB. The GIDB is a pair of data buses that is always duplex for control. The CTSs received over the selected LIDB are transported in the corresponding time slots in two buses between the ELC and the line circuits. At any time, each line circuit listens to one CTS in one of the buses. Control information is always returned over the corresponding CTS in both buses. The GIDB bus that a line circuit listens to for control can be specified by writing to registers on each line circuit. A line circuit will also switch the bus that it listens to or control information each time it is reset.

Although eight-line circuits are physically implemented on each ISLU2 line pack, line circuit control is essentially no different than it is for ISLU. Each line circuit is controlled

on an individual basis via a dedicated set of control and status registers. The actual line circuit implementation may have certain control functions for more than one line implemented within shared ICs or other circuit elements on the line card. Since lines are equipped eight line circuits per pack, hardware growth must be done on an eight-line basis. The ISLU2 line circuit control capabilities will make it possible to assign, remove, restore, and diagnose line circuits on a per-line basis.

8. METALLIC ARCHITECTURE

8.01 The ISLU2 metallic architecture supports metallic access to the tip/ring interface of line circuits and subscriber lines for testing, diagnostics, ringing, and/or sparing. The ISLU2 metallic architecture is also very similar to that of ISLU. Significant differences include:

(a) With sixty-four lines per line group, the maximum number of lines sharing a Line Group Bus (LGBUS) for ringing and test access is doubled, as compared to the maximum with ISLU.

(b) The ISLU2 has a new sparing architecture that provides less degradation in ringing, diagnostics, and metallic testing capabilities when sparing is active.

(c) ISLU2 supports cleaner metallic test paths containing no active components and the ability to insert or remove additional capacitance. These enhancements improve the quality of measurements obtained on analog lines and provide test paths capable of passing Digital Subscriber Line (DSL) transmission signals and test signals of comparable amplitude and frequency.

The ISLU2 metallic access and service capabilities are supported by the MAN, EHLSC, and RG packs equipped in the common shelf.

9. METALLIC ACCESS CAPABILITIES

9.01 Each MAN pack is essentially a relay switching matrix. Four MAN packs together with additional relay circuits on the line packs, EHLSC packs, and RG packs implement the complete ISLU2 metallic access structure. The primary functions supported by the metallic access structure include:

(a) Ability to set up a metallic connection between a line circuit or subscriber line and an EHLSC,

(b) Ability to set up a metallic connection between a subscriber line and a RG,

(c) Ability to set up a metallic connection between a line circuit or subscriber line and a Metallic Test Bus (MTB) connected to the ISLU2 common shelf backplane that provides access for external metallic test systems,

(d) Ability to metallically disconnect a subscriber line from a faulty line circuit and connect it to a spare line circuit.

10. METALLIC SERVICE CAPABILITIES

10.01 Metallic services are supported by the Enhanced HLSC (EHLSC) and RG packs in ISLU2.

The EHLSC is a general purpose test and ringing circuit that can be metallically connected to the tip/ring interface of a line circuit and/or

subscriber loop. It is used to perform per-call tests on analog lines, NT mismatch testing on U-DSLs, and line circuit and metallic network diagnostics. In some applications, it is also used to provide additional ringing capacity and special purpose ringing cadences.

The EHLSC supports PPM and also provides special or overflow ringing in countries that use earth-backed ringing.

The EHLSC supports all of the capabilities of the HLSC. The EHLSC also provides earth-backed ringing capability and capabilities for generating and measuring low-level 0-20 kHz signals. The small signal capabilities will be used to support the testing of 12 kHz and 16 kHz PPM circuitry on Z-packs. They will also be used to control diagnostic access and source PPM test signals to the Fifty Hz PPM Unit (FPPMU).

The type and number of EHLSC packs equipped in a unit will be engineered according to the different types of lines and number of each type equipped, and the amount of traffic anticipated. No EHLSC packs will be required in units equipped with only T line circuits, since T-packs have no metallic access.

Two EHLSC packs will typically be equipped in units with U circuits but not Z line circuits. Two to six EHLSC packs will be equipped in units with Z circuits.

The RG provides bulk ringing capability for Z lines. To ring a line, a metallic path is set up from the tip/ring line interface to the RG pack, which generates the AC ringing voltage. The RG can simultaneously ring multiple lines, although at any instant ringing voltage may be applied to only one line in each group of lines sharing a common Line Group Bus (LGBUS). The RG will typically be used to provide standard ringing to normal single party lines. The EHLSCs will be used to provide certain special purpose ringing functions, including non-standard frequency ringing, ring-lead ringing, and reverse battery ringing. The RG will be used for all other non-standard types of ringing.

ISLU2 will use the RG packs developed previously for ISLU. There are two versions of the RG, one providing 20 Hz bulk ringing and the other providing 25 Hz bulk ringing.

Two RG packs will be equipped in each ILSU2 unit containing Z line circuits. Both RGs equipped in a unit must be the same type. RGs are not needed in units equipped with only T or U line circuits.

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