# 5ESS®SWITCHING SYSTEMS
# SWITCH MODULE PROCESSOR
# MODEL 4 (SMPU4)
# CIRCUIT

*D. Description of Changes*

D.1

This information is to be appended to CD section II-3.

PACKET INTERFACE MODEL 2 - UN395

The PI2 is essentially an enhanced version of the PI with improved performance and the ability to support multiple PSU/PSU2 complexes. the PSU2 was developed for improved packet throughput for existing PSU features (ISDN), and for a new Wireless feature referred to as Code Division Multiplexed Access (CDMA). The PI2 circuit pack (UN395) is architectonically the same as the PI and provides the basic PI function, buffering the signaling packets between the PSU/PSU2 and the SMP40.

The current PI supports one 10Mbps PSU complex. The PI2 can support up to two PSU complexes at a 10Mbps packet bus rate (PSU) or at a 100MBps packet bus rate (PSU2).

The PI2 provides buffering of sugnaling packets between the PSU complexes (PSU or PSU2) via the packet bus (PB), and from the SMP40 via the SUIB. The 68040 core based design resident on the PI2 administers the transmission/receiving of signaling packets to/from the PSUs via PBMAC devices, and arbitrates the release of receiving packets to the SMP4 via a 1M byte FIFO Dual port static RAM.

D.2

This information is to be appended to CD section III-4.

PACKET SWITCH UNIT (PSU/PSU2) INTERFACE

The PB is a duplexed bus connecting the PI/PI2 to the PSU or PSU2 complex. The PI supports only the 10Mbps PB, while the PI2 supports both 10Mbps and 100Mbps PBs. The following paragraphs describe the 10Mbps and 100Mbps packet bus interface.

For the 10Mbps interface six differentially balanced signals are used:

a. Clear to send

b. Transmit/receive data

c. Request to send

d. Receive clock

e. Transmit clock

f. Carrier sense.

For 10Mbps communication, the PSU provides the receive clock which is looped on the PI/PI2 back to the PSU (transmit clock). If the PI/PI2 is trasmitting a signaling packet to the PSU, the PI/PI2 will issue a request to send. The PSU responds by sending carrier sense and clear to send and the PI/PI2 transmits the signaling packet. If the PSU is transmitting signaling packets to the PI/PI2, the PSU sends carrier sense and receive data are sent to the PI/PI2.

For the 100Mbps interface eight differentially balanced signals are used:

a. Clear to send

b. Two - Transmit data

c. Two - Receive data

d. Request to send

e. Receive clock

f. Transmit clock

for 100Mbps communication, the PSU2 provides the receive clock which is looped on the PI2 back to the PSU2 (transmit clock). If the PI2 is transmitting a signaling packet to the PSU2, the PI2 will issue a request to send. The PSU2 responds by sending clear to send and the PI2 transmits the signaling packet. If the PSU2 is transmitting signaling packets to the PI2, the PSU2 sends receive data to the PI2.

D.3

This information is to be appended to CD section I-2.

AWS2000 ADMINISTRATIVE WORKSTATION

The SM2000-AWS provides for a very small office configuration of the 5ESS® Switch consisting of a single SM2000 as the Switch Module, and an Administrative Work Station (AWS) as the Administrative Module providing the disk storage, human interface, and tape writing functions. The SM2000-AWS provides the low-cost workstation configuration with the increased line and trunk capacity provided by the SM2000.

D.4

This information is to be added as CD section III-10.

AWS2000 EXTERNAL INTERFACE

The Ethernet interface within the AWS2000 will be provided by a Message Handler/Ethernet Interface Board (MHEIB). This pack is installed in any one of the three availible MH slots. There are two paddle-boards added on the SMPU4 backplane to provide external interface to the MHEIB in the AWS2000 Configuration. The first paddle-board is the 982YP board that provides Ethernet termination. This board installs on the MH pinfield where the MHEIB is installed. The second paddle-board is the 982YN board that provides a conversion function between the RS232 interface to the Workstation and the CPI interface

to the SM. A new terminal field on the AM3 backplanes will accommodate the 982YN paddle-board. For non-AWS configurations, a jumper paddle-board (982 ET - circuit option ZC) is used to terminate this backplane bus.

The element identifiers NF, NG, NH, NJ, PF, PG, PH, PJ in CAD 1 illustrate the new AWS interfaces. The element identifier 20 in CAD 2 illistrates the new CPI cross-connect cable for AWS.

D.5

This information is to be appended to CD section I-2.

EXTENDED CONTROL DATA UNIT (XCDU)

A new peripheral unit supported in SM2000 R2, XCDU, provides additional PICB and PIDB ports to support any number of additional peripheral on an SM2000, up to the TSI limit. This unit is interfaced to both the SMPU4 and the TSIU4, effectively extending the control and data buses to many more cabinets/lineups in a SM2000.

D.6

This information is to be appended to CD sections III-6 and IV-9.

EXTENDED CONTROL DATA UNIT (XCDU) INTERFACE

Three signal wires were added to the SMPU4-AM3 backplanes (side 0 & 1) for future use with the EXtended Control Data Unit (XCDU).

The three signals ([00,11])ACTIVE, [0,1]RACTIVE, [0,1]FSUMIS), from various packs of the SMP40 unit, were brought to the Spare Slot (eql 88) location of the SMPU4. The APCX (UN555) pack will be located in the Spare Slot and is only required for XCDU interface.

D.7

This information is to be added as CD section III-11.

XCDU EXTERNAL INTERFACES

The Application Controller Expansion (APCX) provides an interface between the SMPU4 Remote Side (RS) bus and the XCDCOM in the XCDU. Note that APCX does not provide the same functionality as the APC pack in SMPU4. Physically, the APCX fits in SMPU4 spare slot at equipment location 088. The APCX interfaces the RS bus to eight eXtended Control and Data Control Link (XCDCL) buses. The XCDCL bus is similsr to the STCL bus between the APC and the SCDCOM; however, the XCDCL transmits different SMP address leads that the STCL. A maximum of eight XCDUs can be connected to the APCX each via their own XCDCL. The XCDCL links are duplexed and max. length is 35 feet. This imposes a limit on the physical location of the XCDU relative to SMPU4. Because of backplane pinout limitations in the spare slot where APCX is located, XCDCL's 4-7 require a "translator board" (9822DR) to be plugged onto the wiring side of the backplane. XCDCL cables 4-7 are plugged inot the translator board. The function of the translator board is to arrange the XCDCL signals in an orderly fashion so they may be cabled easily between the APCX and the XCDU (using the same cable pinout as ports 0-3). XCDCL's 0-3 do not require a translator board and plug directly onto the backplane.

CIRCUIT DESCRIPTION

CD-5D195-01
ISSUE 1
APPENDIX 2B
DWG ISSUE 3B
DISTN CODE BT13

AT&T BELL LABORATORIES

DEPT NA5350300-mgs

CD-5D195-01
ISSUE 1
APPENDIX 1M
DWG ISSUE 2M
DISTN CODE BT13

# 5ESS® SWITCHING SYSTEMS
# SWITCH MODULE PROCESSOR
# MODEL 4 (SMPU4)
# CIRCUIT

## CHANGES

### *D. Description of Changes*

There are no changes to the circuit description (CD) for Issue 2M of the schematic drawing (SD), SD5D195-01.

AT&T BELL LABORATORIES

DEPT NA5350300-MS-FNG

CD-5D195-01
ISSUE 1
DWG ISSUE 1
DISTN CODE BT13

# 5ESS® SWITCHING SYSTEMS
# SWITCHING MODULE PROCESSOR
# MODEL 4 (SMPU4)
# CIRCUIT

TABLE OF CONTENTS PAGE

## *SECTION I - GENERAL DESCRIPTION*

### *1. PURPOSE OF CIRCUIT*

This document is a circuit description of the Switch Module Processor Unit, Model 4 (SMPU4). The hardware of the SMPU4 is a major evolutionary step in the Switch Module Processor architecture, and is intended to provide a processing platform that will meet both International and North American switching needs into the late 1990s. Improved performance was achieved by designing the processor complex around a Motorola 68040 microprocessor split bus architecture and by moving messaging functions to a second processor.

### *2. GENERAL DESCRIPTION OF OPERATION*

The 5ESS Switch is a digital time division switch with a time-space-time architecture. The Time Multiplexed Switch (TMS) provides a centralized space division switching function and connects to various Switching Modules (SMs) that perform time division switching and interface to transmission facilities.

The SMPU4, Time Slot Interchange Unit (TSIU), Digital Service Unit (DSU), mid-cabinet fan unit and Fuse/Filter Unit (FFU) are common to all SMs. Various peripheral units are equipped in the SM as needed.

#### 2.1 Switch Module Processor Unit, Model 4 - Overview

The SMPU4 is the primary intelligence of the SM. It controls the links, Time Slot Interchange (TSI), and peripherals. Figure 1 depicts the Switching Module Processor 40 (SMP40) Processor Architecture. The SMPU4 is a duplex processing complex based on the thirty-two-bit Motorola 68040 microprocessor. The duplex system consists of two identical

microprocessor systems, side 0 and side 1, interconnected by a system update bus that allows each processor (CORE40) full access to its mate's memory and peripherals. The sixty-four-bit (thirty-two bit multiplexed address and data plus thirty-two additional data bits) wide Local System (LS) bus connects each processor to its local memory (MEM32) and to the Bus Service Node (BSN), which provides interfaces to the sixty-four-bit wide update bus and the thirty-two bit multiplexed address and data Remote System (RS) bus.

The RS bus connects the processor to the Message Handler (MH) and APplications Controller (APC) circuit packs, which allows the LS bus to be optimized for the MC68040 processor's burst access to memory. The main features of this are a bus cycle shorter than required for accessing Input/Output (I/O) and a burst cycle where the processor can read or write 128 bits (sixteen bytes) in a single bus cycle. The RS bus is designed for a thirty-two bit transfer (or smaller) and does not support the burst capability.

The system update bus connects the two sides of the processor. When the update bus is enabled, all writes in the active processor also occur in the mate processor, keeping the mate processor's memory and registers up to date. The update bus supports burst writes but not burst reads.

The BSN provides a centralized bus arbitration for the LS, RS, and system update buses. Some modes may be disabled by the BSN; for example, there is a register bit which blocks the RS bus from gaining control of any of the other buses.

The CORE40 is the lowest priority and receives a bus grant only if no other source requests the bus [RS-Direct Memory Access (DMA) or update bus accesses].

Processor control of existing peripheral units such as Gated Diode Crosspoint (GDX) line units, Digital Line and Trunk Units (DLTUs), Digital Carrier Line Units (DCLUs), and Integrated Services Line Units (ISLUs) occur through serial control buses called Peripheral Interface Control Buses (PICBs), which are 2 MHz serial buses with fixed length control messages that consist of address and data fields and are generated by the Control Interface (CI) packs. Processor control of the Packet Switching Unit (PSU) occurs through the Packet Interface (PI) circuit-pack. The CIs and PIs are part of the SMPU4 and provide cross-coupled interfaces to the peripheral units. The processor communicates with the CIs and the PI on the same side over the Sub-Unit Interface Bus (SUIB). On each side, the APC circuit-pack provides the bus interface between the RS bus and the SUIB.

The Switch Module 2000 (SM-2000™) TSI is accessed through the Serial Time slot interchange Control Link (STCL) on the APC for processor control of the TSI. The TSI occupies 2-Mbyte direct-mapped address space in the SMPU4's address spectrum, and is part of the same failure group as

the SMPU4. The STCL is not cross-coupled.

The MHs are used by the SM processor to communicate with the Administrative Module (AM) and other SMs. There will be one to three MH circuit packs per side. The messages use High-level Data Link Control (HDLC) formatted frames transferred into time slots that are switched through the TSI. Each MH is provided a 256-time-slot link from the APC. The MH time slots are mapped by the APC into the 768 data time slots called the Messaging, Central processor intervention, and Pump (MCP) link, which is part of the 1024-time-slot link from the TSI.

Physically, the MCP link is a bi-directional serial link consisting of two data leads in each direction. Each data lead carries alternate bits of the serial bit stream and runs at 32.768 Mbits/sec over coaxial cables using differential pseudo Emitter Coupled Logic (ECL) levels. The APC provides the interface between the MH links and the MCP link, breaking up the time slots from the TSI to the MHs, and combining the time slots from the MHs to the TSI. The MHs for Release 1 of the SM-2000 will be capable of handling up to thirty-two time slots from their 256-time slot links. MH0 (zero) is always equipped in the system.

The MCP link is also used for pump of the SM memory. Thirty-two of the 256 time slots that go to the third MH circuit-pack (MH2) are reserved for pump. The Bootstrapper function within the APC extracts the pump data and places it in processor memory using DMA.

Error-checking circuitry and diagnostic aids are used extensively to facilitate maintenance of the SMPU4. All busses in the SMPU4 are protected by parity, with provision to force parity inversions to verify the operation of the error detection circuits. The MCP link has Cyclic Redundancy Checking (CRC).

The SMPU4 is a duplex unit equipped with the CORE40, the memory subsystem (MEM32), BSN, and all RS Bus circuit packs (MHs and APC circuit packs). The terms "processor" or "simplex" refer to a single side of the SMPU4 (CORE40, MEM32s, BSN, and RS Bus packs).

Comparisons to the Switching Module Processor (SMP) 20 and earlier SMP architectures are included.

## 2.2 SMPU4 Address Space

The address space of the SMPU4 contains regions for each circuit pack's I/O registers, along with large blocks allocated for various memory resources, test interfaces, and future expansion. All address allocations are within blocks of at least 16 MBytes, which allows the possibility of using the transparent translation resources of the MC68040's Memory Management Unit (MMU). (See the section on MMU.) The addressable memory range of 4096 MBytes is broken into four regions of 1024 MBytes each, which have similar memory maps and are decoded to

provide normal forced local only, forced mate only, forced both, and normal access.

The CORE40 will provide 1 Megabyte of Read Only Memory (ROM), which starts at address 0, since it is required on power up. In the remainder of this 16 Megabyte region are the allocations for pseudo-ROM static Random Access Memory (RAM), DEMON Utility System (DUS), and Switch Module Integrated Test System (SMITS) memory. Only the ROM will be equipped in the SMPU4; all the others will be on external test hardware such as the DUS/SMITS board.

A 1024-Mbyte region is allocated to the main memory subsystem.

16 Mbytes are allocated for boot ROM, pseudo-ROM static RAM, DUS ROM, and I/O.

A 736-Mbyte region is allocated for the SMPU4's memory boards.

A 16-Mbyte region is dedicated to LS Bus I/O, including the CORE40 I/O, MEM32 I/O, and BSN I/O.

A 16-Mbyte region is allocated for the RS I/O space, which includes the MH I/O, the APC I/O, and all sub-unit addressing [CIs, PI, and TSI/Signal Processor (SP) via the APC].

A 112-Mbyte region is allocated for the Special Memory Region (SMR), which is only used for the MH buffer RAM and the MH local memory regions. Up to three MH packs per side may be equipped in an SMPU4. Each MH will contain 1 Mbyte of buffer RAM and 1 Mbyte of local memory. To accommodate future growth, 16 Mbytes of memory space is allocated for each MH for shared memory, and 16 Mbytes is allocated for local memory.

128 Mbytes are unequipped.

### 2.3 Power-On Reset Generation

There are situations in which it is desirable to generate a power-on reset to the microprocessor but not to the rest of the SMPU4 hardware. The mechanisms provided for this are as follows:

1. If the Sanity Timer expires eight times in a row with no attempt by software to maintain it, the hardware will generate the power-on reset to the microprocessor. The Central Processor Intervention (CPI) sanity timer inhibit message blocks this protection mechanism.
2. The SM software may write the "Force Power-Up in Mate Controller" strobe, which will have the same effect on the mate processor.
3. CPI reset will cause a processor reset. In previous versions of the SMP, the CPI reset generated a level seven Non-Maskable Interrupt (NMI).
4. SMITS can initiate a reset in a test environment.

### 2.4 Read-Modify-Write Cycles

The SMPU4 allows the use of the instructions for read-modify-write cycles, which are available through execution of the Test And Set (TAS), Customer Account Services (CAS), and Customer Account Services Release 2 (CAS2)

instructions, along with certain page descriptor updates, during translation table searches for the MMU. These will be atomic operations which DMA, interrupts, and mate accesses can not interrupt. They will not be supported for access to the MHs.

## 2.5 Duplex Operation Modes

The SMP has always provided for increased availability by having fully-duplicated processors, which have operated in an active/standby configuration. The SMPU4 is designed so that it will support either an active/standby configuration or a master/slave configuration. To accommodate these two modes of operation, backplane straps will be installed which will force the SMPU4 to operate in the active/standby mode, so that the choice between the two modes will not controlled by software.

Active/standby and master/slave modes of operation require different treatment of level 7 interrupts in the hardware. Since the selection of the mode of operation is made via a backplane strap, a given unit will operate only in the specified mode.

### 2.5.1 Active/Standby Bus Operation

The SMPU4 is designed to run primarily in the active/standby mode, in which one processor side is active [A Flip-Flop (A-FF) set and RUNNING], and the other side is standby (as indicated by its microprocessor having executed a STOP instruction and its memory being up to date). When the update bus is enabled in the active/standby mode, all write operations in the active processor are performed simultaneously in the mate standby processor. This allows switching from side to side, and under no-fault conditions, switching to the mate side is accomplished without introducing errors.

### 2.5.2 Master/Slave Support

An alternate mode of operation is master/slave operation, in which both sides of the SMPU4 are executing code. One processor is designated master, the other, slave. Periodically, the master processor queries the slave to determine if it is software-synchronized. The SMP20 can run master/slave. however, certain capabilities will be enhanced in SMPU4 to better support master/slave operation.

To operate as master/slave, two processors need to meet the following criterion:

a. The master must have the ability to stop the slave execution and then allow the slave to resume from the point of stopping (PAUSED).

b. The master must have the ability to stop and restart the slave at a pre-defined point (STOPPED).

c. An efficient message capability must exist between the master and slave processors. In master/slave operation, the update bus is not normally enabled.

The separation of the stop mate and pause mate capability will deterministically place the mate processor into a known configuration from which its future actions can be predicted.

## 2.6 Other Hardware Features

An addition to the SMP architecture is the ability to utilize the update bus when both processors are executing code, which delivers update requests in much the same way DMA cycles are delivered to the microprocessor. When a processor is not in update mode, the arbitration for the bus allocation is biased towards the update bus to reduce bus latency. When in the update mode, the bus is biased towards the microprocessor.

The CORE40, MEM32, BSN, and MH boards each have an eight-bit read-only configuration register [or IDentification (ID) Register], which allows quick identification of any features implemented on the boards.

Each board (except the PI and CI) also has a 1024 eight-bit location Inventory Register that contains ASCII-based inventory control information such as serial numbers, Common Language Equipment Identifier (CLEI) code, series number, etc. The eight-bit locations are long word (thirty-two bit) aligned and occupy 4 Kbytes of addressable space.

# *SECTION II - DETAILED DESCRIPTION*

The SMPU4 has four subfunctions:

a. Switch Module Processor (SMP),

b. Control Interface (CI),

c. Packet Interface (PI), and

d. PoWeR ConTRoL (PWRCTRL).

The sections that follow deal with the four SMPU4 subfunctions in details.

### *1. SWITCHING MODULE PROCESSOR*

The SMPU4 provides the operating environment for software and interfaces to the TSI sub-units, and may be in one of five states:

- The first state, OFF, is when the processor has no power (5 Volts) applied or when a power fault is present in the SM.
- The second state, RUNNING and not ACTIVE, is when:
  - a processor is executing code in STANDBY mode, the term "STANDBY" signifying a non-active processor whose memory is identical to the active processor, and
  - the update bus is enabled from the active to the standby side.
- The third state, RUNNING and ACTIVE, is when a processor is executing code in the ACTIVE mode, the term "ACTIVE" signifying a processor that is RUNNING and has its A-FF set. While RUNNING, the mate is unable to gain access to the running processor's buses.
- The forth state, STOPPED, is when the microprocessor has executed a STOP instruction,

which puts the microprocessor in a DMA hold condition, granting the mate access to all internal buses via the update bus. The processing will resume once an appropriate level interrupt has been received, no cycles are pending, and the appropriate interrupt has been acknowledged.

- The fifth state, PAUSED, is when execution of code has been temporarily suspended by mate software. The term "mate" always refers to the other side. (Side 0's mate is side 1, and side 1's mate is side 0.) Only non-active processors may be PAUSED.

Under normal (no faults) operating conditions, the active processor keeps all data areas in the standby controller up to date, so that the standby processor can, at any time, be made active. Should a fault occur in the active processor, the standby processor will be made active and the active processor put into Out Of Service (OOS) mode.

Two types of program memory are provided in the SMP: flash memory and Dynamic Random Access Memory (DRAM). 1Mbyte of non-volatile memory is provided on the CORE40 for power-up initialization and fault recovery. The SMPU4 uses up to four TN1685 memory boards, 32 Mbytes each, which allows a maximum of 128 Mbytes of DRAM to be equipped. The MEM32-TN1685 provides Error Detection and Correction (EDC) circuitry over its DRAM that detects and corrects all single bit errors prior to delivery of data to the backplane. (The CORE40 and BSN will see corrected data.) All double bit errors will be detected but not corrected.

In the SMP20, system memory write protection was provided on-board by each memory pack. In the SMPU4, system memory write protection is provided by the BSN pack over 4 Kbyte pages (no write protection on the memory board) and by the MMU resident in the MC68040 microprocessor.

The interrupt structure for the SMPU4 is similar to the structure of the SMP20. Refer to the CORE40 Interrupt Structure for a detailed description.

Each processor possesses a sanity timer, reset under software control. Failure to reset the timer, or resetting the timer too often causes an NMI to be applied to the SMPU4. The active processor resets the timer in the standby processor. A timeout of the sanity timer in the standby processor results in the standby processor leaving the standby state and, under software control, entering the OOS state. The minimum interval requirement is disabled in the off-line side.

A CPI path from the Administrative Module (AM) to each SMPU4 can be used as a hard-wired path to force an SM into a known state. The SMPU4 has a minimum of control over the path of the CPI message and no control over the designated action taking place. The six possible CPI actions are:

1. force SMPU4 side 0 active, side 1 OOS,
2. force SMPU4 side 1 active, side 0 OOS,
3. clear the force active set by one of the above CPI functions,
4. force processor(s) reset,
5. disable the sanity timers in both processors, or
6. enable the sanity timers in both processors.

A Mate Power Fail (MPF) detection capability is provided to prevent the active processor from corrupting the mate's memory when the active processor sustains a power failure. This circuitry prevents a processor that has lost power from writing the mate, and forces the mate active.

The SMPU4 function is performed by the following five SMPU4 circuit packs:

1. the processor Core (CORE40) contained on the UN540 circuit pack,
2. the processor Memory (MEM32) contained on one to four TN1685 circuit packs,
3. the processor BSN contained on the KBN8 circuit pack,
4. the processor MH contained on one to three UN538 circuit packs, and
5. the processor APC contained on the UN539 circuit pack.

### 1.1 Microprocessor Core (CORE40) - UN540

The CORE40 circuit pack contains the Motorola MC68040 microprocessor, operating at 33.33 MHz, which provides an integral MMU, two internal 4 Kbyte cache memory systems, and an integral Floating Point Unit (FPU) along with the highly pipelined Integer Execution Unit. The MMU is the primary mechanism for validating each bus cycle initiated by the microprocessor. The MMU page descriptors provide the write protect and "cachable" status either for 4 Kbyte or 8 Kbyte pages (for either all-4-Kbyte or all-8-Kbyte pages. There is no intermixing.)

#### 1.1.1 Internal Cache Memories

The two 4 Kbyte caches (one for instructions, the other for data) internal to the MC68040 will be the only cache memory provided in the system. The data cache can operate in one of two modes, as selected by the MMU page descriptor on a per page basis:

1. Copy-Back mode, which only writes data to main memory when the cache entry will be updated with a new tag and
2. Write-Through mode, which maintains coherency between the cache and main memory by performing all writes to the cache and main memory simultaneously.

Special attention must be taken by software when utilizing the copy-back mode to ensure mate memory coherency.

### 1.1.2 Memory Management Unit

The Integral MMU provides logical to physical address translation and is the primary mechanism for write protection for microprocessor initiated cycles. Pages may be 4 or 8 Kbytes, and each page may be specified as write-protected and non-cachable, non-cachable serialized, cachable write-through, or cachable copy-back. Page descriptors are stored in RAM. The MC68040 accesses the appropriate page descriptor by using the value in the Supervisor Root Pointer (SRP) or User Root Pointer (URP), depending on whether it is in Supervisor or User mode, and performs a tablewalk. To reduce the number of tablewalks, two sixty-four entry four-way set-associative address translation caches are internally provided to the MC68040 for storage of most recently accessed pages' descriptors.

Page descriptors must be maintained for all equipped addresses in the system, as an access fault (bus error) will result if an attempt is made to access a page that has no descriptor. In addition to the page descriptors, the MC68040 provides four Transparent Translation Registers (TTRs), two for text accesses and two for data accesses, which may be used to provide protection and cache modes for blocks (minimum 16-Mbyte resolution) of transparently translated (no logical to physical translation) addresses.

In SMPU4, the MMU provides access to the mate processor. The thirty-two-bit address spectrum of the MC68040 is broken down into four separate spaces, as indicated by address bits A30 and A31.

When using the Normal Space encoding, the operation will follow the standard update bus protocol. If the update bus is enabled, then all writes will occur in the mate processor as well as in the local processor. The MMU will translate these four spaces into the same addresses, except that A30 and A31 will be set to zero and the User Page Attributes (UPAs) UPA0 and UPA1 will be set to the values of A30 and A31, respectively. The backplane will then receive the values of UPA0 instead of A30, and UPA1 instead of A31. This insures coherency and protection between mate memory, local memory, and the internal caches of the MC68040.

Coherency of the MC68040 internal caches can be insured only if the Forced Mate and Forced Local and Mate address spaces are designated as non-cachable. The caches of the MC68040 are physical caches. Therefore, a conflict exists with the translation of multiple logical addresses into common physical addresses in different processor sides. To resolve this conflict, one of the logical addresses (for performance reasons, the mate space) must be marked as non-cachable.

The mate memory spectrum may be accessed, with the MMU disabled, by the same addressing scheme. Hardware cache coherency will not be maintained if forced local

operations (A31=0 and A30=1) are utilized.

Disabling of the MMU while the caches are enabled will select the default cache mode of write-through, and serialization of operations will not be enforced when address translation is disabled. (This is independent of the caches being on or off.) Serialization can be forced by placing a No OPeration (NOP) instruction between the accesses that should be serialized.

For example, a write of the PRE-A Flip-Flop (PREAFF) followed by a read strobe of the A Flip-Flop CLocK (AFFCLK) can be performed out of sequence if the MMU (specifying I/O to be serialized) is disabled. Placing a NOP instruction between the write and read will insure proper sequence.

If accesses to I/O space are not serialized, many errors may occur due to incorrect sequencing, such as writes to registers being attempted before the I/O timer is unlocked or after it has been locked.

### 1.1.3 EPROM & Pseudo-ROM

The CORE40 contains 1 Mbyte of flash memory to replace the 128 Kbytes of Erasable Programable Read Only Memory (EPROM) present in the SMP20 and earlier versions. The flash memory in the system can not be altered until specific hardware is added in the test utility slot (specifically for updating the flash memory). The pseudo-ROM feature used in the test environment with SMITS will be provided for the entire EPROM spectrum. Static RAM for the pseudo-ROM will be located on the SMITS board.

### 1.1.4 System Bus Control

The System Bus Control will interface the microprocessor with the LS Bus and will support byte (8 bit), word (16 bit), long word (32 bit) and Quad Long Word (QLW) (128 bit) operations.

### 1.1.5 Interrupt Structure

The interrupt structure for SMPU4 will be similar to the structure of SMP20. The SMPU4 utilizes six of the seven available interrupt levels. A new Interrupt Enable Register (IER) on the CORE40 will allow each level of interrupt (with the exception of level 7) to be enabled or disabled independently, providing a single location to mask each level of interrupt independently.

Level 7: These interrupts will be sourced by any unmasked bit set in the Reset Source Register: Sanity Timer, CPI, from mate reset, SMITS/DUS, and summary errors from the hardware and software Error Source Registers (ESRs).

Level 6: These interrupts are allocated to the Address/Data/Operational pattern matchers on the BSN circuit pack.

Level 5: These interrupts are the fast pump mechanism on the APC.

Level 4: These interrupts are the operational CPI.

Level 3: These interrupts are the programmable interrupt controllers for peripheral maintenance interrupts.

Level 2: These interrupts are the programmable interrupt controller for operational interrupts.

Level 1: Level 1 is not assigned and is available, if required, for future applications.

### 1.1.6 Test Utility Bus (TUB)

The Test Utility Bus (TUB) interface resides on the CORE40 and provides the connection to the SMITS/DUS circuit pack in a test environment. This is a new thirty-two-bit interface (replacing the existing eight-bit interface), which required the development of a new SMITS/DUS board (UN364) for use with the SMPU4.

Refer to the "Internal Interfaces" section for a detailed description.

### 1.1.7 CORE40 I/O Structure

The I/O structure of the CORE40 contains registers and strobe points that provide the necessary support for interrupt maintenance and duplex control.

#### 1.1.7.1 Reset Source Register

The Reset Source Register summarizes the seven NMI sources to the microprocessor. It operates in conjunction with the Reset Source Mask Register to generate an NMI if any of the specific conditions are met.

#### 1.1.7.2 Hardware, Software, and Summary Error Source Registers

The hardware, software, and summary Error Source Registers (ESRs) function identically. The Summary ESR reports to the Hardware ESR, and the Hardware and Software ESRs report directly to the Reset Source Register. Each bit in each of the three ESRs can be set by externally detected sources (if specified) or by software. Each bit also has an associated mask bit in the appropriate mask register. If a mask bit is set, the error bit may be set, but the error will not propagate beyond the register. If a mask bit is not set and an error bit is set (by hardware or software), the error will be propagated to the next level register.

#### 1.1.7.3 Interrupt Enable Register

This is a new register for SMPU4. The Interrupt Enable Register provides a single location to mask each level of interrupt independently. Previous SMPU4s had various interrupt mask bits scattered throughout the system (generally associated with the circuitry responsible for generation of the interrupt). SMPU4 consolidates these mask bits into a single register. A "1" in each bit position will allow the specific level of interrupt to be presented to the microprocessor.

#### 1.1.7.4 Read Interrupt Status Register

This is a new register for SMPU4. The Read Interrupt Status Register gives software the ability to determine if a specific level of interrupt is pending prior to enabling that level.

#### 1.1.7.5 Controller Status Registers

There are five registers which report processor status. The Controller Status 1, Controller Status 2, and Active Status Register are carry-overs from previous SMPs. The Auxiliary Status Register and Test Utility Status Register are new additions for SMPU4.

The Controller Status 1 Register is divided into two parts. The high four bits are read-only bits that reflect processor status, and the low four bits are read/writable bits that contain the reset count.

The Controller Status 2 Register primarily provides information about the last exception zero. All of the bits in this register latch on specific events and hold that information until the register is written. The low six bits give information about why the microprocessor was given an external reset (exception zero). They are as follows:

- reset From the Test Utility,
- reset from CPI Gate Array,
- reset from Mate GENESIS Strobe,
- reset From Double Bus Error (HALTED),
- reset from Sanity Timer Timing out 8 times with no maintenance, and
- reset from Hardware Reset prior to Sanity Timer Minimum.

Two additional conditions are latched in Controller Status 2. Any change in the mate processor's execution state (ACTIVE, RUNNING, STOPPED) will set the Mate State Change Bit. Read Data Parity Errors from the TUB are also logged in this register.

The Active Status register provides information about both processor sides of an SMPU4, and reflects the mate's execution status and if any forces are currently active.

The Test Utility Status Register is a new register that consolidates the status from the TUB.

The Auxiliary Status Register has been added to provide additional miscellaneous status for Out-Of-Service, Diagnosing This Controller, Diagnosing Mate Controller, I/O Timer 1 Running, I/O Timer 2 Running, and Test Utility Equipped.

#### 1.1.7.6 Configuration Register

The configuration register is an eight-bit read-only register that currently has no bits defined. The register reads zero for this first core circuit pack, indicating a 33.33 MHz MC68040 based SMPU4 with no external cache. Future versions of the processor pack will define additional bits, as necessary, to distinguish between various

COREXX board capabilities.

#### 1.1.7.7 Special Function Maintenance Register (SFMR)

The Special Function Maintenance Register (SFMR) can invert parity for each byte of address and data on a per-cycle basis, can ignore bad parity on a per-cycle basis and can initiate self-test in the dynamic memory system.

Previous SMPs guaranteed non-interruptibility for the Special Function operation occurring on the next data cycle. Increasing levels of parallelism caused the inclusion of two NOP instructions prior to the writing of the Special Function Registers. The parallelism of the MC68040 is such that non-interruptibility cannot be guaranteed. Therefore, the functionality of the register is changed.

### 1.1.8 I/O Timer

The I/O timer provides a measure of control over accesses to I/O locations that have the capability to change the state of the processor. Due to the large internal caches of the MC68040, the I/O timer in SMPU4 will run for fifty-six I/O cycles (not including memory accesses or DMA accesses), or 117 us, which ever comes first. The I/O timer blocks level 2 interrupts when unlocked.

### 1.1.9 Scan And Distribute

The scan and distribute point terminations from the SMPU4 Control and Display function have been relocated to the CORE40 circuit pack. The scan and distribute function has been collapsed from three registers to two registers, and the Dual Link Interface (DLI) scan and distribute function has been eliminated, as the DLI scan and distribute points are no longer applicable. The SMPU4 will use the SN516B board for control and display functions (this functionality had been integrated into the SMP20).

### 1.1.10 Conditional Suspend Timer

This is a new thirty-two-bit timer, which runs at a 15.36 us rate. It is anticipated to implement a conditional suspend function in the operating system of the SMPU4 where, if the calling code has executed for longer than a specified interval, the function will perform a suspend and give up control of the processor.

## 1.2 Memory (MEM32) - TN1685

There are four dedicated unit slots for the main memory subsystem, physically located between the CORE40 and the BSN circuit packs. Initially, the MEM32 (32 Mbyte) memory board will provide main memory. The SMPU4 architecture supports memory mixing like the SMP20, except that future memory boards are limited to multiples of 16 Mbytes. Due to the bus architecture of the SMPU4, the MEM32 circuit pack is not compatible with Module Controller and Time slot interchange Unit 2 (MCTU2) or any previous SMP releases.

The memory subsystem resides on the LS Bus and is capable of transferring 128 bits, a QLW, in a single transaction. A thirty-two-bit multiplexed address/data bus and a thirty-two-bit data bus (used only for burst transfers) allow sixty-four bits of data to be transferred simultaneously. Therefore, a burst operation consists of two sixty-four-bit data transfers.

Each MEM32 circuit pack occupies 64 Kbyte of I/O space. The I/O offset is determined by the unit slot position in which the board is equipped.

The MEM32 pack does not provide any write protection hardware. Processor initiated cycles utilize the MMU for write protection. DMA cycles and update bus cycles will utilize the DMA write protection facility provided by the BSN pack.

### 1.2.1 Dynamic RAM Error Detection and Correction (EDC)

Current design practice in the 5ESS® Switch has placed an Error Detection and Correction (EDC) circuit on most Dynamic Random Access Memory (DRAM) systems. The memory access protocol between the CORE40 and the MEM32 is such that the CORE40 will always receive corrected data from the memory system. The MEM32 provides EDC circuitry over its DRAM that detects and corrects all single bit errors prior to delivery of data to the backplane. (The CORE40 and BSN will see corrected data.) All double bit errors and some triple bit errors will be detected but will not be corrected. The only performance penalty imposed by this mode of operation occurs when correctable errors are encountered in the RAM.

### 1.2.2 Dynamic RAM Self-Test

A memory self-test will verify the ability of each memory location to store a zero and a one, and will verify addressability of each memory location. It will not verify proper operation of the EDC circuitry nor any of the system interface logic or I/O control logic. An initialization pass (initialize all memory locations to 0 and store good Hamming) will be available via the control register and will be executed automatically by hardware on power-up resets.

### 1.2.3 Memory Error Source and Mask Registers

Each MEM32 circuit pack has an MEMory Error Source Register (MEM_ESR) for latching and reporting memory pack related errors. For reporting errors, each MEM32 pack provides a single error lead that feeds the Summary Error Source Register on the CORE40 circuit pack. Each bit in the MEM_ESR is maskable by the corresponding bit in the MEMory Mask Error Source Register (MEM_MESR).

### 1.2.4 Correctable Count and Threshold Registers

Each detected correctable bit error will increment the value in the MEMory Correctable Bit Count (MEM_CBC) register. When the

value in this register exceeds the value specified in the MEMory Correctable Bit Threshold (MEM_CBT) register, a correctable bit error will be set in the MEM_ESR. Upon receipt of a hardware reset signal or power-up reset, the MEM_CBC and MEM_CBT are cleared to zero. The value specified in the MEM_CBT is the threshold value for reporting correctable bit errors as NMIs to the microprocessor. For example, writing the MEM_CBT to zero means that detection of the first correctable bit error will be reported to the MEM_ESR. Writing the MEM_CBT register to a value of 0xFE implies that the detection of the 255th correctable bit error will set a correctable bit error in the MEM_ESR. Writing the MEM_CBT to the value 0xFF is special in that a correctable error will never be set in the MEM_ESR by the detection of correctable bit errors (equivalent to masking the correctable bit error via the MEM_MESR). If the value written to the MEM_CBT register is 0xFF then the count value in this register will wrap around to 0x0 upon receipt of the 256th error (counter is modulo 256).

### 1.2.5 Memory Base and Size Registers

The memory subsystem supports memory mixing. Each memory pack receives an eight-bit base address to which it adds its size. It then passes that value to the next memory pack slot position to become the base for the next memory pack. The first memory pack receives its base from the CORE40 pack. Both the base and the size of each memory board may be read via registers on each memory board.

### 1.2.6 Memory Control and Status Registers

The MEM32 circuit pack contains control and status registers to conduct and supervise operations performed by the pack. The MEMory ConTRoL (MEM_CTRL) register specifies the pack operating modes, and the MEMory STATus (MEM_STAT) registers (MEM_STAT1 and MEM_STAT2) contain miscellaneous read-only maintenance status.

### 1.2.7 Memory EDC Diagnostic Latches

There are four thirty-two-bit EDC circuits on the MEM32 pack. Each thirty-two-bit EDC is dedicated to and provides error detection and correction for one word in a line of memory. Each EDC device contains an internal diagnostic latch for verifying proper operation. Through a coordinated sequence, each diagnostic latch register is available to diagnose the ability of the device to detect and correct single-bit errors over the thirty-two-bits of data it protects.

### 1.2.8 Memory ID Register

MEMory IDentification (MEM_ID) is an eight-bit register that provides pack-specific information. For the initial release of the MEM32 pack, this register will read 0x0, indicating that this memory pack uses 4 Mbit DRAM technology and is burst capable.

## 1.3 Bus Service Node (BSN) - KBN8

The Bus Service Node (BSN) provides the interface between the LS, RS, and system update busses, which determines which bus: LS, RS, or system update, currently "owns" this processor side. The BSN is the master for all busses on a given SMPU4 side and is responsible for granting the busses to all circuit packs (CORE40, APC, mate BSN) that wish to perform transactions.

The BSN provides much of the core support functionality that is found in earlier SMPU models, in addition to some new features.

### 1.3.1 Bus Interfaces and Arbitration

The BSN provides interconnection between the LS bus, the RS bus, and the system update bus of the SMPU4. An arbiter on the BSN provides a single point from which the CORE40, mate processor, and RS bus packs request ownership of the busses. (Presently, the only RS bus pack which will be capable of being a bus master is the APC.) The arbiter assigns access priority based on the update mode status, the mate enable function, the bus(es) being requested, etc. The arbiter grants ownership of each bus on a per-cycle basis, allowing both processors full access to their mate's memory. Whenever both processors request the same resource, the arbiter determines which processor must "relinquish-and-retry," if necessary.

### 1.3.2 Timers

Two programmable timers are used to provide two distinct system functions: a billing counter and a 10 ms operational interrupt. Their implementation in the SMPU4 provides the same functionality as the SMP20. Each timer device contains three independent sixteen-bit counters, which can be programmed to operate in any of six modes.

#### 1.3.2.1 10 ms Timer

One of the timer devices contains the 10 ms timer, miscellaneous timer, and 10 ms interval timer. Counter 0 of the device is dedicated to the 10 ms timer and is clocked at 1.125 MHz (the same as SMP1 and SMP20). The output of this is connected as an operational interrupt in Programmable Interrupt Controller (PIC) A.

Counter 1 is clocked by a 1.125 MHz clock. Its output is connected as an operational interrupt in PIC-A. This counter is available as a miscellaneous timer.

Counter 2 is clocked by the output of the 10 ms timer (counter 0) and counts the number of 10 ms intervals which have occurred.

#### 1.3.2.2 Billing Counter

The second timer is used for the billing counter. This counter actually consists of counter 1 and 0 of the device cascaded to form a thirty-two-bit counter. Counter 1 is the least significant sixteen bits and

counter 0 is the most significant sixteen bits. The billing counter is clocked by the 8 KHz CPI clock provided to the BSN from the APC.

Counter 2 [MISCellaneous 2 (MISC2)] of the billing counter can operate in the following modes:

1. it can operate identically to the SMP20 implementation with an input clock rate of 281 KHz, or
2. it can be used to count the number of instructions executed by MC68040.

When using option 2, each count of the MISC2 counter indicates 128 instructions.

#### 1.3.2.3 Load Count Strobe Points

The counters of the timers will not load the programmed values until a clock edge occurs. The special strobe points are provided to generate a single clock to the 10 ms interval timer and billing counter, respectively.

### 1.3.3 Programmable Interrupt Controllers

The BSN provides three Programmable Interrupt Controllers (PICs) to handle operational and maintenance interrupts. The implementation is the same as SMP20, except for the differences mentioned below.

PIC-A provides operational interrupts at level 2 to the CORE40, changed from level 4 in the SMP20. The operational interrupts are: the 10 ms interrupt, operational interrupts from each RS Bus pack (MH0, MH1, MH2, APC, and SPARE), and the miscellaneous counters' interrupts.

PIC-B and PIC-C provide a reporting mechanism for up to sixteen maintenance interrupts. The functionality is the same as the SMP20, but the interrupt sources have changed in the SMPU4, due to architectural differences. These PICs generate a level 3 interrupt to the CORE40.

The maintenance interrupts are: the RS Bus packs (MH0, MH1, MH2 and APC), an interrupt caused by clearing the A-FF, the subunits (TSI/SP, CIs, and PI), the spare RS Bus slot, the CPI error, and mate error inputs.

### 1.3.4 Central Processor Intervention (CPI)

CPI provides the AM with a "hard-wired" path to the SM, over which specific configurations can be forced within the SMP. The CPI link is formed by sampling one bit out of each Control Time-Slot (CTS) to form an 8 Kbyte/sec path from the Dual Message Interface (DMI) to the SMPU4. The bit is stripped out of the CTS of the TSI link on the APC, and passed to the BSN for decoding.

All CPI operational messages (except for Force Reset) generate a level 4 interrupt to the CORE40. Diagnostic messages do not. Force reset generates an exception 0 (reset) to the microprocessor. The CPI messages also contain a seven-bit data

field, which can be used to send additional information with the message.

The CPI device is accessed by SMPU4 software via five I/O locations. Four are read-only eight-bit registers, and one is a write-only strobe point. The four registers reflect the state of the CPI device outputs (which directly control the hardware state of the SMPU4), the last message type sent, error indication bits, and the CPI data field. If an error is detected (such as message CRC failures), the CPI device generates a maintenance interrupt to PIC-B.

### 1.3.5 Write Protection

The SMPU4 utilizes the MMU of the MC68040 for providing write protection and stack protection on processor-originated cycles. The MMU does not provide write protection for bus cycles originated by the system update bus or RS Bus (DMA). Consequently, a write protection mechanism is provided by the BSN, which protects system memory from errant write cycles. This protection includes all cycles: CORE40 originated cycles, RS bus cycles (DMA), and system update bus cycles.

Three BSN registers control write protection: Bus Service Node Set Write Protect (BSN_SWP), Check Write Protect (BSN_CKWP) and the Bus Service Node Miscellaneous Control And Status (BSN_MCAS). The BSN_SWP register is used to set or clear write protection over a 4 Kbyte block of memory.

In order to check the write-protect status of a particular block, the BSN_CKWP register is used.

A master write protection disable bit is available in the BSN_MCAS register. Write protection can also be disabled for testing via a backplane pin. The status of the backplane disable lead is reflected in the BSN_MCAS register.

### 1.3.6 Shadow Registers

The shadow registers capture the state of the SMPU4s' address and data busses, and their control signal status, when a level 7 interrupt occurs.

### 1.3.7 Matcher Registers

The matcher registers are a new capability for the SMPU4, which provide a function within the BSN similar to a logic analyzer trigger. It is anticipated that these registers will be used (with appropriate SW) for debugging system problems, both in the system labs and in operational environments. Matcher registers are provided for the address bus, data bus, and control signals, using the same layout as the shadow registers.

These registers can be programmed with a value to which each bus cycle is compared. If the values in all three registers match and the function is enabled, a level 6 interrupt pulse is generated to the CORE40. The matcher function will continue to generate level 6 pulses for subsequent matches until the function is disabled.

### 1.3.8 A Flip-Flop and A Flip-Flop Clock

Hardware ensures that only one processor may have its A-FF set when RUNNING. Hardware will also set (Force Active) the A-FF under the following conditions:

1. If the mate processor is powered down, the A-FF is forced to the active state.
2. Upon receipt of a CPI Force Active message, the A-FF is set.
3. For Remote Switch Modules (RSMs), the Craft Intervention Key in the alarm status panel will simulate a CPI Force Active.

### 1.3.9 Bus Control Register (BCR) and Shadow BCR

The Bus Control Register (BCR) provides control over the operations allowed on the SMPU4 busses and information regarding its respective processor side.

### 1.3.10 BSN Error Source Register

The BSN contains an error source register which collects address and data parity errors for each of the three busses terminating on it. A bit is present for BSN-detected multiple response, along with a bit which indicates that a bus arbitration error has occurred. This arbitration error occurs if:

1. this side is RUNNING with its update bus off,
2. the mate is RUNNING with its update bus off,
3. the Mate Enable bit is active on both sides, and
4. the mate does not respond to a mate only cycle request in 128us.

The summary of these errors is reported to the CORE40 Hardware ESR.

### 1.3.11 RS Bus Parity Control

The BSN provides the ability to invert the sense of the RS Data and Address bus parity checkers on a byte-by-byte basis. This capability is provided via the Bus Service Node PARity Maintenance (BSN_PARM) register. This register cannot be written in a processor which is ACTIVE, as a ready time-out will occur. This is an eight-bit register, each bit corresponding to one of the four data bytes and four address bytes of the RS Bus. Setting the appropriate bit will force the BSN to check for even parity on address and/or odd parity on data for the specified byte of the RS Bus. This register is cleared by the Hardware Reset strobe and held clear if this side is ACTIVE.

### 1.3.12 Diagnostic Synchronization Strobe

A read/write strobe point is provided which toggles the logic level of backplane pin 653. This pin can be used by software to provide external test equipment with a synchronization point.

### 1.3.13 Remote Switching Module Registers and Strobes

The Bus Service Node Remote Switching Module Status (BSN_RSMS) register centralizes RSM configuration indicators (backplane straps) and reflects the RSM stand-alone and sanity lamp status. The RSM sanity timer (not related to the SMPU4 sanity timer) must be administered by system software every fifty-nine seconds, or the RSM sanity lamp [located on the Switching Module Control (SMC) cabinet bezel on RSMs] will change from green to red.

### 1.3.14 Configuration Register

The configuration register is an eight-bit read-only register. Currently, only of its one bits, which indicates that this is a BSN for release 1 of SM-2000, has been defined. Future versions of the BSN may define additional bits as necessary to distinguish between various BSN and SMPU4 capabilities.

## 1.4 Message Handler (MH) - UN538

The MH terminates multiple message links in the SMPU4. It is a fully-duplexed part of the SMPU4 failure group, with a corresponding MH in the mate SMPU4. A single MH can terminate thirty-two of the 256 time slots available to each MH board slot from the APC. A maximum of three MHs may be equipped on a given SMPU4 side. (The minimum required is one.) The thirty-two available time slots on an MH can be treated as thirty-two individual sixty-four-Kbit channels, or concatenated together to form higher bandwidth channels.

HDLC-formatted frames may be transferred over a given channel with a resident processor available on the MH for performing protocol processing. The dedicated C-links for the SMPU4 are fixed and occupy four time slots of the first MH slot (MH0) in the SMPU4. Ten additional time slots on an MH may be programmed for C-links. The major components of the MH are:

1. two 1-Mbyte memory subsystems: Local Random Access Memory (LRAM) and Buffer Random Access Memory (BRAM),
2. Local Processor (LP),
3. SPYDER-T Synchronous Protocol Data Formatter,
4. Bit Register Interrupt Controller Programmable Interval Times (BRICPIT) custom device,
5. mate MH update bus interface,
6. APC interface,
7. SMPU4 interface, and
8. General Purpose Integrated Test System (GPITS) interface.

The MH is essentially a two-bus architecture. The LP resides on the Local bus (L-bus) together with its local memory (LRAM), the BRICPIT device, MH update bus interface, and GPITS interface. Isolating the LP and its memory system on the L-bus maximizes LP performance.

HDLC frames are formatted by the SPYDER-T device and stored in the BRAM for transfer to and from the SMPU4. These functions reside on the Buffer bus (B-bus), with the interface used by the SMPU4 for accessing buffered frames.

### 1.4.1 Memory

The MH provides a total of 2 Mbytes of Static Random Access Memory (SRAM), partitioned into two 1-Mbyte regions. One region of 1-Mbyte SRAM, the LRAM, interfaces to the L-bus and is dedicated primarily to LP usage. The second 1-Mbyte region of memory, BRAM, is used by the SMPU4 and SPYDER-T for storage of transmit and receive frames.

The LRAM is accessible to the LP, SMP, mate LP, and mate SMP. Since the LRAM is intended to be dedicated to LP usage during normal operation, there should be no contention on the L-bus when the LP accesses it. This ensures that fast access times can be achieved, thus maximizing LP performance. The hardware does not allow access of the LRAM by the SPYDER-T device.

The second 1-Mbyte region of memory is used for storage of transmit and receive frames, and for the SMPU4/MH software interface. It is accessible to the LP, SMP, mate LP, mate SMP, and SPYDER-T device. Non-LP initiated accesses to the BRAM do not impact LP real time.

Both 1-Mbyte regions are organized as 256K x 32-bit long words, with a stored parity bit over each byte. Parity is checked for any SMPU4, LP, or SPYDER-T read operation and generated and stored on any write by the LP, SMPU4, or SPYDER-T. Parity for SMPU4 accesses is generated and checked by the SMPU4. The MH stores the parity received on writes and passes the stored parity to the SMPU4 for checking on reads.

Byte, word, and long word operations are supported. The RAM regions are not initialized by hardware after a power cycle.

No ROM is provided on the MH. It is assumed that the MH LP will be held in reset until the LRAM has been pumped by the SMPU4. At that time, the LP can be released.

#### 1.4.1.1 Memory Spectrum

Three fundamental regions are defined for the MH: LRAM, BRAM, and I/O. Each is mapped into the LP and SMP memory spectrum and aligned to a 16-Mbyte boundary (though the 16-Mbyte boundary is different for the SMP and LP).

Each of these regions in the mate MH are fully accessible to the LP.

#### 1.4.1.2 I/O Structure

The LP MMU is the only form of write protect provided for LP-initiated accesses to I/O. No other form of I/O protection (I/O timer, for instance) is provided for LP-initiated I/O cycles, except for the BRICPIT reset strobe.

### 1.4.2 LP Description

For the LP, the MH uses the Motorola 68040 microprocessor, operating at 16.67 MHz, which provides an integral MMU, two 4-Kbyte cache memory systems, an integral FPU, and a highly-pipelined Integer Execution Unit. It is anticipated that all features except for the FPU will be utilized in the MH application. Bursting is inhibited by hardware, forcing the MC68040 to automatically generate four distinct long word transfers for sixteen-byte operations (for instance, filling or pushing an internal cache line). Byte, word, long word, and sixteen-byte transfers are supported.

Parity will be checked on all LP-initiated reads of LRAM or BRAM, with an error latched in the Event Source Bit Register (ESBR), if an error is detected. Parity is generated and stored for LP-initiated writes to LRAM, BRAM, and over the MH update bus.

#### 1.4.2.1 Internal Caches

Two 4-Kbyte caches are provided in the MC68040: one cache dedicated to the instruction stream and one to the data stream. The caches are four-way set-associative, with a line size of sixteen bytes, and operate on physical addresses. The cache can operate in one of four modes, as selected by the MMU page descriptor, on a per-page basis:

1. cachable, copyback;
2. cachable, writethrough;
3. cache-inhibited, serialized; and
4. cache inhibited, not serialized.

No form of external cache disable control is provided on the MH.

#### 1.4.2.2 MMU

The integral MMU provides logical-to-physical address translation, is the mechanism for write protection over LP-initiated write cycles, and is used for detection of LP accesses to unequipped memory regions. A page size of 4-Kbyte or 8-Kbyte may be selected. Each page may be write protected and specified as non-cachable, non-cachable serialized, write through cachable, or copyback cachable.

### 1.4.3 Interrupts

Various events which can occur on the MH generate an interrupt to the LP, and a subset of these events also generates an interrupt to the SMPU4. All interrupt event sources are latched in the BRICPIT for software evaluation by the LP or SMPU4. All interrupts to the LP use the MC68040 autovector operation to provide the exception vector number and terminate the interrupt acknowledge cycle. The event categories which result in an interrupt to the LP are:

1. GPITS,
2. loss of MH update bus,
3. hardware detected errors,
4. SPYDER-T interrupt,

5. SMPU4 to LP interrupt, and

6. BRICPIT timers.

Hardware error checking is provided over each interface and over various internal MH operations. All errors are detected and latched in the BRICPIT to generate an interrupt to the LP. These interrupts may be masked by the LP or the SMPU4. Errors which indicate a potential loss of LP sanity, incorrect LP operation, or SMPU4 interface errors generate an error interrupt to the SMPU4 in addition to the LP interrupt. If the error interrupt is enabled in the SMPU4, the resulting SMPU4 interrupt will cause the MH update bus to be removed (if it's currently enabled), generating a subsequent interrupt to the LP. Disabling of the MH update bus prevents a potentially insane LP from corrupting the mate's memory.

Errors which are reported by hardware to the SMPU4 are summarized into a single error interrupt signal, latched in the SMPU4, which generates a level 7 interrupt to the SMPU4. This interrupt can be masked at multiple points in the SMPU4 interrupt hierarchy.

The SMPU4 can generate an interrupt to the LP using a bit in the Reset/Set Bit Register (RSBR). This may be used by the SMPU4 to notify the LP of high priority tasks for which it wants immediate attention.

### 1.4.4 SPYDER-T

The SPYDER-T device performs the HDLC formatting functions for the thirty-two channels terminating on the MH, and provides zero-bit insertion and deletion, and CRC generation and checking during the transmission and reception of frames. All interactions between the SPYDER-T device and the LP occur through the shared memory structure in the BRAM, the interrupt lead (2860INT) from the SPYDER-T to the LP, and the ReSeT (RST) and SPYDER-T Attention (SA) leads from the LP to the SPYDER-T.

Even parity is checked and generated on a per-time-slot basis for the thirty-two time slots that are used by the MH.

When the SPYDER-T device reads the BRAM, parity is checked and any errors are sent to the ESBR. On writes, parity will be generated and stored in the BRAM.

### 1.4.5 BRICPIT

The BRICPIT device performs a number of functions on the MH. It contains:

1. six programmable timers, with associated interrupts available,

2. an RSBR with individual bit operation capabilities,

3. an ESBR for latching various events,

4. an Interrupt Source Request Register (ISRR) with associated Interrupt Mask Bit Register (IMBR) for generating interrupts from events latched in the ESBR, and

5. various configuration and maintenance registers for

initialization and diagnostic testing of the device.

The device is clocked at 16.67 MHz providing internal timers with a 60 ns resolution.

Of the six internal timers, two are dedicated for the sanity timer and ready (watchdog) timer. The remaining four are available for software use. Timeouts from all six terminate in the ESBR, allowing interrupt generation to the LP, if unmasked in the IMBR. In addition, a ready timer timeout results in an error interrupt to the SMPU4, if allowed by the RSBR. A sanity timer error does not result in an error interrupt to the SMPU4.

### 1.4.6 MH Update Bus

When running duplex, a dedicated update bus is provided, between each active side MH and its associated MH in the mate SMPU4, for maintenance of the standby MH memory image. This minimizes the amount of data which needs to be copied from the active MH to the standby MH prior to an SMPU4 switch.

Refer to the "Internal Interfaces" section for detailed description.

### 1.4.7 Parity

The majority of cycles which occur on the MH use data which is protected by parity. There is one parity bit for each byte of address and each byte of data. Even parity (parity such that all bits plus the parity bit result in an even number of "1's") is used over the data, and odd parity is used over address. Data parity is generated and checked for MH I/O regions, and is stored with the data for MH RAM regions.

Address and data parity is utilized for all transactions which occur over an external bus (update and SMPU4 system bus transactions). Address parity is checked for all SMPU4-initiated cycles on the remote system bus (RS bus - SMPU4 interface), with data parity also checked for all SMPU4-initiated writes to the MH. Detection of an address or data parity error is latched in the ESBR, with an error interrupt reported to the SMPU4 (if unmasked in the RSBR).

Write operations are always blocked by hardware if an error is detected, independent of the error interrupt mask. Data parity is provided for all SMPU4 reads of the MH. SMPU4 reads of RAM regions return the stored parity to be checked by the SMPU4. Data parity is generated for all SMPU4 reads of MH I/O. Write data parity can be inverted by the SMPU4 for diagnostic testing using the SMPU4 special function maintenance register. If the "ignore bad parity" signal from the SMPU4 special function maintenance register is also asserted during the cycle with bad parity, the write operation will be allowed to complete (the error is still latched in the ESBR), and the bad parity will be stored if the write is to a RAM region.

Data parity is generated and stored for all LP-initiated writes to RAM regions and checked

for all LP reads of RAM regions. LP operations which initiate an update bus cycle generate address parity over the update bus. Data parity is generated for all update write cycles and checked for all update read cycles. Update-bus-initiated cycles occurring in the mate MH perform an address parity check for all operations and a data parity check for write operations. If an error is detected, write operations are blocked. The received data parity is stored for update-bus-initiated writes to RAM regions. Stored parity is checked and passed for update-bus-initiated reads (a mate-only read cycle initiated by the mate processor) of the RAM regions. Data parity is generated for update bus initiated reads of MH I/O regions.

Parity is generated and stored for SPYDER-T writes to BRAM. Parity is checked, with an error latched in the ESBR, for SPYDER-T reads of BRAM. No mechanism is provided to invert parity for SPYDER-T-initiated writes. The LP may plant parity errors in LRAM and then initialize the SPYDER-T device to read the corrupted BRAM locations for verification of proper parity error detection during a SPYDER-T read.

### 1.4.8 MH's APC Interface

The MH's APC interface is a bi-directional serial interface, consisting of 256 eight-bit time slots for use as messaging channels. The three 256-time-slot links from the MHs are merged at the APC into the TSI link between the SMPU4 and TSI.

Refer to the "Internal Interfaces" section for further details.

### 1.4.9 SMPU4 Interface

The system bus that the MH interfaces to is the RS bus, which is a multiplexed thirty-two-bit address/thirty-two-bit data bus. A parity bit is provided for each byte of the address/data. The RS bus uses odd parity for address and even parity for data.

Address parity is checked on all SMPU4-initiated bus cycles. The MH hardware claims ownership of a cycle, using the board response code bus, and checks for multiple-response code violations (indicating RS bus contention) for all addresses decoding to it. Multiple-response errors are latched in the ESBR, with an associated SMPU4 error interrupt generated (if unmasked in the RSBR). Data parity is checked on all SMPU4 writes to the MH. Writes are blocked if MH hardware detects an error (address parity, data parity, or multiple response).

Refer to the "Internal Interfaces" section for further details.

### 1.4.10 GPITS Interface

The MH has an interface to the General Purpose Integrated Test System (GPITS), which is a tool used for early debugging of the MH's circuitry. GPITS interfaces to the MH L-bus. An eight-bit

data interface with associated address is provided for accessing external GPITS hardware.

## 1.5 Applications Controller (APC) - UN539

The APC contains most of the application-specific interfaces between the processor unit and other SM hardware. The major functional blocks of the APC are:

1. the TSI Link Interface, used to interface the MCP Link to the three MH links, and to extract the CPI and pump time slots,
2. the BooTStrappeR (BTSR) interface (implemented using the same Bootstrapper/Dual Link (BDL) interface custom device used on the UN518 circuit-pack, the BDL data interface block, and the DMA logic), used to provide fast pump of the SM memory after the power-up and initialization sequences,
3. the Sub-Unit Bus Interface, used to interface the SUIB, and to control the SUIB cycles,
4. the Serial TSI Control Link (STCL) Interface, used to interface the STCL, and to control the STCL cycles, and
5. the System Bus Interface, used to interface the system bus to the internal registers, SUIB, and STCL interfaces, and to control the system bus during DMA write cycles generated by the APC.

Other miscellaneous functions implemented by the APC include the APC Error Register; the Hardware Delay Register, used to provide small, fixed hardware delays independent of processor speed on I/O cycles; the Inventory Information Storage function, used to store circuit-pack information; and the Message Handler Reset function, used to provide reset pulses to the Message Handlers.

### 1.5.1 TSI Link Interface

The TSI Link to the APC is the MCP link. In release 1, the messaging consists of CTS and Quad Link Packet Switch (QLPS) time slots. After release 1 it is anticipated that there will be a need for other message interfaces, which will be handled by the MHs. There may be from one to three MH circuit-packs per side. Each MH is provided with a 256-time-slot link from the APC. The MH time slots are mapped by the APC to the 768 data time slots of the TSI Link. The APC provides the interface between the MH links and the MCP link, breaking up the time slots from the TSI to the MHs, and combining the time slots from the MHs to the TSI. The MHs for Release 1 of the SM-2000 will be capable of handling up to thirty-two time slots only from their 256-time slot links. Future releases of the MHs may be capable of using all 256 time slots.

Refer to the "External Interfaces" section for further details.

### 1.5.2 Bootstrapper (BTSR) Function

The APC bootstrapper will provide a fast pump capability for the SMPU4, which will be provided by the BDL device, a BDL Device Interface circuit, and a DMA controller. The BDL device is the same device that is used for fast pump in the SMP20. Since the signaling is now subsampled and TSI Link time slots are eight bits long, a BDL Device Interface will construct the sixteen-bit pump time slots that the BDL device expects by bit-stuffing the eight bits of signaling and parity bit. The assembly and DMA transfer of thirty-two-bit words of pump data is performed after the BDL device detects the start of a pump block. Incoming pump data is First In, First Out (FIFO) buffered, and FIFO overflow indication is provided.

For SM-2000 Release-1, the DMA controller will be implemented discretely on the APC, in which case the DMA controller registers will change from the previous Application Controller. In particular, the DMA Mask register will not be implemented since DMA can be disabled on the BSN and on the APC.

The bootstrapper can be configured to pump either the local or the mate processor or both. The Bootstrap control register in the BDL device determines the mode of operation. There are three operational modes: interrupt mode, DMA mode, and resync mode. The maintenance modes are the same. However, in the maintenance modes, an internal data source is generating the pump data.

The three test modes, interrupt, DMA, and resync, all utilize the internal data source to generate an alternating data pattern through the data assembler.

#### 1.5.2.1 Bootstrapper BDL Device

The BDL device (also used in SMP20) contains the bootstrapper data assembler, Bootstrap Control register, Bootstrap Diagnostic Strobe Point, BDL FIFO, and DMA map register.

There is a bootstrapper FIFO of thirty-two bits wide by sixty-four words internal to the BDL device. Only thirty-two bit accesses are allowed to the FIFO. At the maximum pump rate of 192 Kbytes/s, this provides 1.33 ms of header and data buffering. A level 5 interrupt is generated, if unmasked at all appropriate levels, after four words have been loaded into the FIFO, leaving 1.25 ms of additional data buffering remaining for the SMPU4 to complete header processing and programming of the pump DMA controller. The FIFO is accessed via the APC internal thirty-two bit data bus.

The bootstrapper data assembler extracts six data bits per sixteen-bit time slot for pump, reassembles them into thirty-two-bit words, and loads the assembled word into the BDL FIFO.

The registers are addressed, using the address decoding of the BDL device, during processor accesses, and are written or read over the high word of the APC internal data bus. The Bootstrap Control register is an eight-bit

register which:

1. controls the modes of operation,
2. indicates which processor is to be pumped (as in "this side" or "mate side"),
3. indicates the FIFO status (empty or overflow), and
4. provides a diagnostic bit which can be written by software and is cleared by the 8KHz sync pulse.

There are 5 DMA map registers internal to the BDL device provided for five DMA channels. However, only one channel will be used on the APC, and only one map register will be selected for pump DMA. Two other BDL registers are the Bootstrapper Diagnostic Strobe Point, used to force the data assembler to lose sync, and the FIFO thirty-two-bit read/write register.

#### 1.5.2.2 Bootstrapper BDL Device Interface

To be compatible with the sixteen-bit time slot format that the BDL device expects, the BDL Device Interface will construct sixteen-bit time slots from the eight-bit pump time slots received from the TSI Link Interface functional block. It will append eight bits to each of the eight-bit time slots. The fifth bit it appends to each time slot will be the bit extracted from the Active Pump Time Slot (APTS) register, used to indicate which pump time slots are active.

#### 1.5.2.3 Bootstrapper DMA Controller

The bootstrapper DMA controller is implemented discretely on the APC. It contains one channel for DMA, to be used in conjunction with the DMA functionality contained in the BDL device. It also contains two sixteen-bit registers: the DMA controller address register and the DMA controller word count register.

The DMA controller can assume one of three states: idle, DMA, or I/O. During the idle state, all control signals are initialized to the correct values for no DMA or I/O accesses of the DMA controller registers. Based on two inputs, a DMA select signal from the APC address decoder, or a Pump DMA request from the BDL, the DMA controller will change states to the I/O state or the DMA state.

DMA I/O accesses are considered to be I/O accesses to: the DMA address register, the DMA word count register, the bootstrapper reset strobe point, and the bootstrapper diagnostic scan point. The I/O state will override the DMA state in case there are any I/O operations to the APC DMA controller in progress when the BDL detects a long word in the FIFO and issues a pump DMA request.

Once in DMA mode, the DMA controller will issue an RS bus request and wait for the RS bus grant, upon which the acknowledge is issued to the BDL, and the DMA cycle is begun. When the DMA cycle concludes, the DMA controller goes back to the idle state to wait for another pump

DMA request from the BDL or a DMA select signal for an I/O access of the DMA controller. However, if no RS grant is issued, because DMA is not enabled in the BCR, the controller will switch states to the I/O mode and begin the I/O cycle once the controller is in DMA mode awaiting an RS bus grant and a subsequent I/O access is made to the DMA controller.

At the completion of the I/O cycle, the controller will switch back to the idle state, where the pump DMA request from the BDL will still be asserted, and the DMA controller will enter the DMA state again.

### 1.5.3 The Sub-Unit Interface Bus

The Sub Unit Interface Bus (SUIB) is used to access the subunits that are housed within the same unit: the CI and the PI. The APC provides the interface between the system bus and the SUIB and controls the SUIB read and write cycles. The signals, format, and timing of this bus are unchanged from the SMP20.

An RS bus ready time-out error occurs and the RS bus cycle is forced to terminate, causing the APC to terminate the cycle, when:

1. there is a ready time-out error in the system because an APC is not in place or because an APC does not generate a ready back to the RS bus,
2. the APC does not generate a ready back to the RS bus because a sub-unit fails to release the wait lead to the APC during SUIB cycles, or
3. the APC does not generate a ready back to the RS bus because there is no acknowledge from the TSI during STCL cycles.

Refer to the "Internal Interfaces" section for further details.

### 1.5.4 Serial TSI Control Link (STCL) Interface

The Serial Time slot interface Control Link (STCL) Interface provides the processor control interface to the TSI. This new interface was developed for processor control of the TSI, as the SUIB has an address range of only 128 bytes (addressable as sixty-four words), and the new TSI for the SM-2000 requires up to two Mbytes of addressing (addressable as 512K longwords). The TSI is part of the same failure group as the SMPU4, hence the STCL bus is not cross-coupled to the TSI.

Refer to the "External Interfaces" section for further details.

### 1.5.5 System Bus Interface

The system bus that the APC interfaces to is the RS bus, which is a multiplexed thirty-two-bit address/thirty-two-bit data bus. A parity bit is provided for each byte of the address/data. The RS bus uses odd parity for address and even parity for data.

Refer to the "Internal Interfaces" section for further details.

### 1.5.6 Miscellaneous Functions

#### 1.5.6.1 APC Error Register

The APC contains an ESR, which latches and reports errors detected by the APC board.

#### 1.5.6.2 The Hardware Delay Register

The hardware delay register provides software with a means of implementing small, programmable delays that are independent of the processor execution speed. A value between 0 and 31 may be written into this byte wide register. The duration of the write cycle on the RS bus (that writes this value into the register) will be extended such that the cycle will be at least as long as the value that is written, in microseconds. It is anticipated that this register will be used to implement the gapping required between CI operations. Where delays of greater than 32us are required, multiple writes must be performed.

#### 1.5.6.3 Message Handler Resets

Three message handler reset signals are generated by the APC, one to each message handler, and can be asserted or de-asserted by writing to a register on the APC. This register is cleared to an all "0"s state if the backplane power-up reset signal is active, so that the message handlers will be held in the reset state during power-up.

### *2. CONTROL INTERFACE - UN71B*

The Control Interface (CI) function consists of one/four circuit pack(s) per SMPU4 side and provides an interface (PICB) between the SMPU4 and various peripheral units for control information. Up to twenty-three PICBs are available with each CI. One to four CIs may be equipped in the SMPU4 side, providing a maximum of ninety-two PICBs. Each PICB contains five twisted-wire pairs that carry clock, output data, input data, SMPU4 select information, and peripheral unit service requests.

The CI to SMPU4 interface is through the SUIB, which is a parallel, sixteen-bit, bidirectional data bus with a six-bit address bus. The CI contains several registers that are accessible by the SMPU4 through this bus. The CI performs four functions for the SMPU4:

a. permits the SMPU4 to write sixteen bits of information to a peripheral unit register (maximum of 256 destination registers),

b. permits the SMPU4 to read sixteen bits of information from a peripheral unit register (maximum of 256 source registers),

c. receives, latches, and reports service requests from peripheral units, and

d. detects and reports CI operational errors.

The CI reads and writes peripheral registers through an exchange of serial messages over

the PICB. A distribute operation writes sixteen bits of data into a peripheral unit destination register, and a scan operation reads sixteen bits of data from a peripheral unit source register.

The SMPU4 will initiate all scan and distribute operations, in which the peripheral unit will send a reply message back to the CI. In the reply message, there is a three-bit All Seems Well (ASW) code, which is used to report errors detected by the peripheral unit. If errors are detected during a scan or distribute order by either the CI or a peripheral unit, the error will be reported by latching a bit in the error source register. The interrupt lead to the SMPU4 will become active if an error occurs. The ability to inhibit this interrupt on a per-PICB basis is provided.

In addition to performing scan and distribute orders, the CI reports peripheral unit service requests by latching an active state on the PICB interrupt lead into the interrupt source registers. (Remote interrupt) inhibit registers are provided such that these service requests may be handled by interrupts or by polling.

### *3. PACKET INTERFACE - TN1042*

The Packet Interface (PI) function consists of one circuit pack per SMPU4 side and provides an interface between the SMPU4 and the PSU, which implements Integrated Services Digital Network (ISDN) capabilities on the 5ESS Switch. The PI and PSU provide a centralized high-bandwidth interface to support packetized data and signaling messages. By centralizing packet processing in the PSU, efficient signaling, maintenance, and administrative interfaces are maintained, and the distributed architecture of the 5ESS Switch is enhanced.

The main function of the PI is to buffer signaling packets between the PSU Protocol Handlers (PHs) via the Packet Bus (PB), and to and from the SMPU4 via the SUIB. Resident on the PI is circuitry that interfaces to the SUIB and a Port Processor (PP), which transmits and receives packets between the SMPU4 and PHs. The PP design is common to the PI and PH. The signaling packets are FIFO-buffered in a 1-Mbyte dual port memory of the PP circuitry. The PP controls Port A of the dual port memory and transfers the signaling packets across the PB. Port B of the dual port memory transfers signaling packets to and from the SMPU4 over the SUIB.

### *4. POWER CONTROL*

There is a PoWeR ConTRoL (PWRCTRL) function on each SMPU4 side, which provides a +5 volt controlled power supply for the SMPU4, CI, PI, and TSIU functions. Two power supplies are used per SMPU4 side, each powering different portions of the SMPU4 unit. One power supply (EQL 04-018) supplies power to the CORE40 circuit pack, the four MEM32 circuit packs, the BSN circuit pack, and the spare slot. The other power supply (EQL 04-

178) is used to power the three MH circuit packs, the APC circuit pack, the PI circuit pack, and the CI circuit pack. The PWRCTRL function is contained on the 410AA Power Converters, and the Control & Display circuitry contained on SN516B.

### 4.1 Power Converter - 410AA

The converter provides a means of converting nominal -48 volt input to a well-regulated and isolated +5 volt output for applications in the SMPU4 circuitry. The power units are pulse width controlled for regulation, self-oscillating, and operate at a fixed frequency. The unit is also self-protected by several types of alarms. The 410AAs provides +5 volts at 300 watts to the SMPU4, CI, and PI functions in the SMPU4.

### 4.2 Control And Display - SN516B

The SN516B provides the following control and display functions:

a. The human interface allows an operator to power on, power off, request a unit either in service or out of service, and manually override momentarily.

b. The alarm display allows the operator to read the status of the power circuits by observing a Light-Emitting Diode (LED) display that indicates the following:

OFF – is a red LED, which when lit, indicates that power is off.

ALM – is a red LED, which when lit, indicates a power fault on the unit fuse or converter alarms. Note that in the alarm state, all power may not be off in the unit. Once an operator powers down the unit for repairs, the OFF LED will light and the ALarM (ALM) LED will extinguish.

OOS – is a yellow LED, controlled by the system, which is lit whenever the unit is OOS.

RQIP – ReQuest In Progress (RQIP) is a green LED, controlled by the system, which lights whenever a request to restore or remove a unit has been received by the system.

ROS – is a green LED, which lights whenever the Request Out of Service (ROS)/ReSeT (RST) switch is in the ROS position.

c. The converter control interface allows the human interface and software interface to control the power converter.

d. The software interface is in the form of scan points to report alarms and signal distributor points to light status LEDs (OOS, RQIP), as all 5ESS Switch units will require some interface between their power and the system software.

e. Auto-Power Off, which prevents powering up to the

whole failure group if a fault is detected.

f. Auto Power Recovery, which is an option for the International market, particularly where AC power is unreliable or battery power is unavailable. If -48 Volts drops below the 410AA power supply threshold of -39V, power is turned off on the SM. Power returns when the voltage reaches a -43V. It is enabled with a jumper strap on the backplane of the C/D circuit pack in the SMPU4.

## *SECTION III - EXTERNAL INTERFACES*

In SD-5D195-01, the external interfaces consist of cables connecting SMPU4 functions to other 5ESS Switch equipment and are referenced as Computer-Aided Drawing (CAD) 1 with individual element identifiers.

### *1. MCP LINK*

The TSI Link interface of the APC will assemble/disassemble the TSI Link into three 16-Mbit/s MH links, four 8-Kbit/s CPI links, and a 2.048-Mbit/s (thirty-two-time-slot) pump link. The functional name for this particular TSI Link to the APC is the MCP Link.

The MCP link is a bidirectional serial link, consisting of two differential data leads in each direction, one differential clock, and one sync signal in each direction. The MCP link is physically connected to the SMPU4's APC and the TSI.

The APC will extract an eight-bit CRC value, received on the MCP Link in the second framing/maintenance byte of the second block (block1) in every frame. This CRC will have been calculated over the previous frame, hence it will be compared to an eight-bit CRC generated by the APC over the previously-received frame. Detection of a CRC error will set the receive bad CRC bit in the APC ESR on the APC. When bad CRC is detected from the TSI, MH data is passed along, with good parity, to the MH, and a bad CRC error bit is set in the APC ESR. Pump data and CPI bits are passed, as when bad CRC is detected on the MCP Link, and a bad CRC error bit is set in the APC ESR.

In the direction back to the TSI on the MCP Link, the APC will generate a CRC byte over the outgoing frame and insert this into the following frame. The APC ID will also be inserted into appropriate overhead bytes in the frame with good odd parity, since only overhead bytes are checked for good parity at the TSI.

The element identifiers AG and FG of CAD 1 illustrate the interconnections between the APC and the TSIU for the MCP link.

#### 1.1 Messaging

A portion of the MCP link (four of the 256 time slots going to MH0) are the CTS messaging time slots used for communication with the AM and other SMs through the MeSsaGe Switch (MSGS) in the Communications Module (CM). CTS

positions on the TSI Link are fixed and occupy the Pulse Code Modulation (PCM) time slot of the first four blocks per frame. All eight bits of the CTS byte will be sent to MH0, where the bits that are unused by the MH will be discarded. In the APC receive direction, the APC will receive the CTS from MH0 where the unused bits in the CTS have been driven to a logical 1 by MH0. Hence, the APC will not treat this time slot differently from any other time slot that it receives from MH0.

### 1.2 CPI

Central Processor Intervention (CPI) bits that are part of the CTS time slots are extracted by the APC circuit pack and sent to a CPI gate array on the BSN pack.

### 1.3 Pump

The MCP link is also used for pump of the SM memory. Thirty-two of the time slots, that are part of the 256 time slots that go to the MH circuit pack, are reserved for pump.

## *2. STCL INTERFACE*

The Serial Time slot interchange Control Link (STCL) provides control access to the TSI from the SMPU4. This link, electrically very similar in nature to the MCP link, consists of two data leads, clock, and sync in each direction. In addition, there is an interrupt signal from the TSI to the SMPU4, and a SMPU4-Active signal from the SMPU4 to the TSI. All signals are differential. The link consists of the following signals:

a. two differential serial data signals at 32MHz in each direction - a total of eight leads,

b. one differential 32MHz clock signal in each direction,

c. one differential sync signal in each direction,

d. one differential interrupt signal from the TSI to the APC, and

e. one differential SMPU4-Active signal from the APC to the TSI.

All operations are longword (thirty-two-bit) operations, and are aligned to longword boundaries. Byte (eight-bit) and word (sixteen-bit) accesses will cause a "no response" error in the system. Non-longword-aligned thirty-two-bit accesses will also cause "no response" errors in the system, since the microprocessor will break these into multiple sixteen-bit/eight-bit accesses.

The serial data from the APC consists of a direction bit, the upper nineteen bits of the twenty-one-bit address, thirty-two-bit write data (if it is a write cycle), and a parity bit that provides even parity over the whole data stream. The direction bit is "0" for a write and "1" for a read. A sync pulse is also transmitted by the APC at the beginning of transmission. In the case of a write cycle, the TSI returns only an acknowledge sync pulse. In the case of a read cycle, along with the sync

pulse, the TSI returns thirty-two-bit serial data, and a parity bit over the data that provides even parity.

Address parity and write data parity error from the RS Bus are checked prior to the initiation of an STCL cycle. If an address parity error or write data parity error is detected on the RS Bus, the corresponding bit is set in the APC ESR, and the cycle is invalidated. (It is completed, but no writes will be performed, and any read data will be invalid.) If the error is not masked, then the error signal is asserted.

During an STCL cycle, a parity bit is transmitted at the end of the serial data stream from the APC to the TSI. This parity is checked by the TSI. During STCL read cycles, the TSI generates parity over the serial data stream to the APC. The APC checks the incoming parity, and if an error is detected, a bit is set in the APC ESR which will cause the assertion of the APCERR signal unless the error is masked. Also, in this case, the data parity bits over all four bytes of data placed on the RS bus will be inverted from the normal even parity.

During an STCL cycle, if the TSI fails to return an acknowledge sync, the APC does not provide acknowledge on the RS Bus. This causes a ready timeout error in the SMPU4, and the RS cycle is forced to terminate, which in turn will cause the APC to terminate the STCL cycle.

If the TSI clock is lost on the STCL link [such as if the Time Slot Interchangeer-COMmon (TSI-COM) circuit pack is missing], TSI accesses will cause a "ready timeout error" in the system.

The element identifiers AH and FH of CAD 1 illustrate the interconnections between the APC and the TSIU for the STCL interface.

### *3. PERIPHERAL INTERFACE CONTROL BUS (PICB)*

A PICB consists of five balanced, differential driven, RS422-compatible, twisted pairs. The clock pair carries a 2.048MHz gated clock signal to the peripheral units. The data out pair carries serial information to the peripheral units from the CI, and the data in pair carries serial data from the peripheral units to the CI. The select pair carries signaling information which is used to select the active side CI, and the interrupt pair transmits service requests from the peripheral units to the CI.

Although the cable length of the PICB may vary, it has a maximum limit of twenty-eight feet. Data is to be gated in and out of the peripheral unit on the negative edge of the clock. To avoid a timeout error, the reply must be received by the CI within 21.5us from the first clock pulse.

The elements identifiers of PICB interfaces in CAD 1 are:

AJ, AK, AL, AM, AN, AP, AR, AS, AT, AU, AW, AY, BA, BB, BC, BD, BE, BF, BG, BH, BJ, BK, BL, BM, BN, BP, BR, BS, BT, BU, BW, BY, CA, CB, CC, CD, CE, CF, CG, CH,

CJ, CK, CL, CM, CN, CP, CR, CS,
CT, CU, CW, CY, DA, DB, DC, DD,
DE, DF, DG, DH, DJ, DK, DL, DM,
DN, DP, DR, DS, DT, DU, DW, DY,
EA, EB, EC, ED, EE, EF, EG, EH,
EJ, EK, EL, EM, EN, EP, ER, ES,
ET, EU, EW, EY, FJ, FK, FL, FM,
FN, FP, FR, FS, FT, FU, FW, FY,
GA, GB, GC, GD, GE, GF, GG, GH,
GJ, GK, GL, GM, GN, GP, GR, GS,
GT, GU, GW, GY, HA, HB, HC, HD,
HE, HF, HG, HH, HJ, HK, HL, HM,
HN, HP, HR, HS, HT, HU, HW, HY,
JA, JB, JC, JD, JE, JF, JG, JH,
JJ, JK, JL, JM, JN, JP, JR, JS,
JT, JU, JW, JY, KA, KB, KC, KD,
KE, KF, KG, KH, KJ, KK, KL, KM,
KN, KP, KR, KS, KT, KU, KW, KY

### *4. PACKET SWITCH UNIT INTERFACE*

The PB is a duplexed bus connecting the PI to the PSU, and consists of the following six differentially-balanced signals:

a. Clear To Send,

b. Transmit/Receive Data,

c. Request To Send,

d. Receive Clock,

e. Transmit Clock, and

f. Carrier Sense.

The PB operates at 10 Mbits/s and allows the PSU to communicate with the PI. The receive clock is continuously sent from the PSU. If the PI is sending a packet to the PSU, the PI will issue a request to send. The PSU responds by sending carrier sense and clear to send. If the PSU is transmitting to the PI, the PI responds by sending carrier sense. The element identifiers of the PSU interface in CAD 1 are: LA, LB, MA, and MB.

### *5. CRAFT INTERVENTION INTERFACE*

There are no plans for SMPU4-Release 1 of the SM-2000 to support an RSM environment, though the hardware exists in the SMPU4 to support this feature for any future releases.

The element identifiers AD, AE, FD, and FE of CAD 1 illustrate the interconnections between the SMPU4 and the RSM status.

### *6. FUTURE FEATURE INTERFACE*

An undefined future feature interface exists on the SMPU4. There is a register on the BSN that is monitored by software. The element identifiers in CAD 1 are AC and FC.

### *7. FAN UNIT SCAN AND DISTRIBUTE INTERFACE*

A fan failure is reported to the SMPU4 through a scan point from the mid-cabinet fan unit to the CORE40 circuit pack. When a fan fails, a scan lead becomes active and is used to light a red alarm LED on the mid-cabinet fan unit and a yellow alarm LED on the cabinet bezel.

The SMPU4 monitors this scan point and will take appropriate recovery actions if the scan point becomes active. A fan alarm can be retired by SMPU4 software, using a distribute point, or manually, by using a push button located on the rear of the mid-cabinet fan unit.

The Fan Unit Scan and Distribution Interface is unchanged from the previous SMP20.

The mid-cabinet fan unit scan and distribute interface appears in element identifiers AA and FA of CAD 1.

### *8. SMPU4 CONTROLLER FUSE ALARM INTERFACE*

The controller fuse alarm interface consists of signals between C/D, Power Converter, and the FFU. The interface is used to monitor blown fuses. When an SMPU4 controller indicator fuse (10A, or 15A for auto-power recovery) is blown, the fuse connects -48 volts to the signal used to light a red alarm LED on the FFU at that blown fuse location, at the cabinet bezel, and on the SN516B-C/D circuit pack. The mate SMPU4 monitors the scan points, and takes appropriate recovery actions if they become active. The SMPU4 also monitors fuse alarms from peripheral units through a Z scan point, and will take appropriate recovery actions if it becomes active.

The element identifiers in CAD 1 for controller fuse alarms are AB and FB.

### *9. UNIT POWER INTERFACE*

The unit power interface is used to control the power to the SMPU4 and the TSIU through the remote start signals, illustrated by the element identifiers AF and FF in CAD 1.

All power for the SMPU4 is connected to the FFU by means of -48 volt feed and -48V return (ground potential). Power feed and return lugs appear in CAD 1, elements XX and YY.

## *SECTION IV - INTERNAL INTERFACES*

In SD-5D195-01, internal interfaces consist of backplane wiring and/or cables between the two backplanes of the SMPU4. All cross-coupled interfaces (signals between side 0 and 1) are indicated in CAD 2.

### *1. LOCAL SYSTEM BUS INTERFACE*

The System Bus Interface connects the LS Bus to the microprocessor and the I/O Structure. The following is a list of the LS Bus signals and a brief description of their functionality.

| | |
|---|---|
| LSD [00:31]: | Local System Data (LSD) bits 00-31 - these bits are used for QLW accesses only. |
| LSDP [H,MH,ML,L]: | Local System Data Parity (LSDP) - Low, Middle Low, Middle High and High parity bits for the LSD bus. Low corresponds to LSD[00:07], Middle Low to LSD[08:15], Middle High to LSD[16:23], and High to LSD[24:31]. |
| LSAD [00:31]: | Local System Address/Data (LSAD) bits 00-31, multiplexed address |

and data bus.

LSADP [L,ML,MH,H]: Local System Address/Data Parity (LSADP) - Low Middle Low, Middle High and High parity bits for the LSAD. Low corresponds to LSAD[00:07], Middle Low to LSAD[08:15], Middle High to LSAD[16:23], High to LSAD[24:31].

LSRDRQ: Local System ReaD ReQuest (LSRDRQ) - "0" indicates a request on the bus for a read operation.

LSWRTRQ: Local System WRiTe ReQuest (LSWRTRQ) - "0" indicates a request on the bus for a write operation. LSWRTRQ and LSRDRQ are mutually exclusive signals.

LSIZ [0:1]: Local system SIZe (LSIZE) - indicates the size of the transaction-byte, word, long word or quad long word.

LSAL: Local System Address Latch (LSAL) - indicates that the address information from the LSAD bus is valid and should be latched.

LSDS: Local System Data Strobe (LSDS) - indicates that it is safe to drive data onto the multiplexed address/data bus for read cycles or that write data is valid on the bus for write cycles.

MSRSP [0:1]: Memory System size ReSPonse (MSRSP) - MSRSP0 is driven by the memory board to indicate burst capability on the current bus cycle. MSRSP1 is driven by the memory board to indicate that is cannot perform the burst cycle request and that the CORE40 circuit pack must perform a fake burst transfer.

LSACK: Local System ACKnowledge (LSACK) - driven by the destination to indicate that the data has been absorbed on writes or the data is valid on reads.

UPWAIT: UPdate WAIT (UPWAIT)- driven by the BSN pack to indicate that the Update Bus is busy and cannot accept the current update requested cycle.

A parity bit is provided for each byte of the address/data. The LS bus uses odd parity for address and even parity for data. Address parity on the LS bus is checked on every LS bus cycle, and data parity on the LS bus is checked on every LS bus write cycle.

*2. REMOTE SYSTEM BUS INTERFACE*

The RS bus connects the processor to the MHs and the APC circuit packs. The following is a list of the RS Bus signals and a brief description of their functionality.

RSAD [00:31]: Remote System Address/Data (RSAD) bits 00-31, multiplexed address and data bus.

RSADP [L,ML,MH,H]: Remote System Address/Data Parity (RSADP) - Low Middle Low, Middle High and High parity bits for the LSAD. Low corresponds to LSAD[00:07], Middle Low to LSAD[08:15], Middle High to LSAD[16:23], High to LSAD[24:31].

RSRDRQ: Remote System ReaD ReQuest (RSRDRQ) - "0" indicates a request on the bus for a read operation.

RSWRTRQ: Remote System WRiTe ReQuest (RSWRTRQ) - "0" indicates a request on the bus for a write operation. RSWRTRQ and RSRDRQ are mutually exclusive signals.

RSIZ [0:1]: Remote system SIZe (RSIZ) - indicates the size of the transaction-byte, word, long word or quad long word.

RSAL: Remote System Address Latch (RSAL) - indicates that the address information from the RSAD bus is valid and should be latched.

RSDS: Remote System Data Strobe (RSDS) - indicates that it is safe to drive data onto the multiplexed address/data bus for read cycles or that write data is valid on the bus for write cycles.

RSACK: Remote System ACKnowledge (RSACK) - driven by the destination to indicate that the data has been absorbed on writes or the data is valid on reads.

RSDS: Remote System Data

Strobe (RSDS) to indicate data bus may now be driven with read data or is being driven with write data

The RS bus is a multiplexed thirty-two-bit address/thirty-two-bit data bus. The RS bus uses an acknowledge signal (generated by any pack that is accessed) to terminate the bus cycle. If the acknowledge does not occur within a prefixed time period, a ready timeout error is generated in the system.

A parity bit is provided for each byte of the address/data. The RS bus uses odd parity for address and even parity for data. Address parity on the RS bus is checked on every RS bus cycle, and data parity on the RS bus is checked on every RS bus write cycle to the APC.

*3. UPDATE BUS*

The SMPU4 update bus connects the two sides of the processor. When the update bus is enabled, all writes in the active processor also occur in the mate processor, keeping the mate processor's memory and registers up to date.

The system update bus of the SMPU4 consists of the following signals:

UPAD[00:31]: UPdate Address/Data (UPAD) bus - a 32 bit wide bus (UPAD 0 - 31) with a parity bit per byte (UADPL, UADPML, UADPMH and UADPH). This bus is multiplexed to provide address and the low 32 bits of data on update bus transfers.

UPD[00:31]: UPdate Data (UPD) bus - a 32 bit wide bus (UPD 0 - 31) with a parity bit per byte: UPDate Parity High (UPDPH), UPDate Parity Low (UPDPL), UPDate Parity Medium High (UPDPMH), and UPDate Parity Medium Low (UPDPML). This bus is only used during update bus burst writes to transfer the high thirty-two bits of data. This bus is not used on thirty-two-bit (or smaller) update bus reads or writes.

UPRDRQ: UPdate ReaD ReQuest (UPRDRQ) - this active low signal indicates an update bus read cycle is in progress.

UPWTRQ: UPdate WriTe ReQuest (UPWTRQ) - this active low signal indicates an update bus write cycle is in progress.

USACK: UPdate System

ACKnowledge - this active low signal indicates an update bus cycle has completed.

UPGO: UPdate second data GO (UPGO) - this active low signal indicates the second double long word is available on the UAD and UD bus during an update burst write.

UPQLW: UPdate Quad Long Word (UPQLW) - this active low signal indicates the current update bus cycle is a burst (QLW) cycle.

FMWXLE: From Mate WX Latch Enable (FMWXLE) - the rising edge of this signal is used to latch address information on the multiplexed UAD bus during all update bus cycles.

UPSIZ(0,1): UPdate SIZe (UPSIZ) - these two signals indicate the size of the current update bus transaction (byte, word, long, or QLW).

The interconnections appear in CAD 2.

*4. MH UPDATE BUS*

When running duplex, a dedicated update bus is provided, between each MH and associated mate MH, for maintenance of the standby MH memory image. This minimizes the amount of data that needs to be copied from the active MH to the standby MH prior to a SMPU4 switch. The interconnections appear in CAD 2.

The MH update bus consists of the following signals:

[0:2]UAD [00:31]: Bi-directional, multiplexed thirty-two bits address/thirty-two bits data plus four parity bits:

1. [0:2]UPMH - Update Parity Middle High, [0:2]UPH - Update Parity High, [0:2]UPL - Update Parity Low, and [0:2]UPML - Update Parity Middle Low

[0:2]USIZ0 (0,1): Update SIZe (USIZ) - Two bits of transfer size indication (bidirectional)

[0:2]URW0: Update Read-Write (URW) - Transfer direction (RW) signal (bi-directional)

[0:2] (T,F)ALE: Transfer (To-Mate, From-Mate) Address Latch Enable (ALE) (uni-directional)

| | |
|---|---|
| [0:2] (T,F)DLE: | Transfer (To-Mate, From-Mate) Data Latch Enable (DLE) (uni-directional) |
| [0:2] (T,F)REQ: | Transfer (To-Mate, From-Mate) REQuest (REQ) (uni-directional) |
| [0:2] (T,F)ACK: | Transfer (To-Mate, From-Mate) ACKnowledge (ACK) (uni-directional) |

Only the LP can initiate cycles over the MH update bus. Three types of cycles can be performed: mate-only write, mate-only read, and duplex write. Mate-only read/writes are explicit operations to the mate, and cause data to only be written or read in the mate. Duplex writes are write operations which occur in both the active and mate side.

Only the active side MH (SMPU4 "A" flip-flop set and executing code) may initiate cycles over the MH update bus. Any attempt by a non-active side LP to initiate an update bus cycle will result in a mate ready timeout error on the side which attempted to initiate the cycle.

Parity protection is provided over address and data for all MH update bus operations. Address parity is generated on the active side for read and write cycles, and is checked in the mate MH. Data parity is also generated for all LP-initiated write cycles that generate an update bus cycle, and is checked in the mate MH.

### *5. MH'S APC INTERFACE*

The MH's APC interface is a bi-directional serial interface, consisting of 256 eight-bit time slots that are used as messaging channels. The three 256-time slot links from the MHs are merged at the APC into the TSI link between the SMPU4 and TSI.

The APC/MH interface consists of one single-ended 16.384-Mbit/s serial data lead and one single-ended parity lead in each direction, and the MH receives a single-ended 16-MHz clock and a single-ended 8-KHz sync from the APC.

The APC will check for even parity received on the links from the MH. Parity over this link is generated on a per-time-slot basis. Parity errors received on the MH links will set a bit (per MH) in the APC ESR, and will activate a level 7 interrupt to the processor when unmasked at all appropriate levels. The frame going back to the TSI is constructed with the MH time slots and a good CRC generated over the frame, regardless of a parity error that may have been detected on the APC/MH link. End to end detection is provided by a CRC over each message in the appropriate protocol.

The APC will generate parity over the eight-bit time slots sent to each MH on a per-time-slot basis. APC transmit parity to the MHs will normally be even.

### *6. SUB-UNIT INTERFACE BUS*

The Sub-Unit Interface Bus (SUIB) is used to access the subunits

that are housed within the same unit. These are the CI and the PI. The APC provides the interface between the system bus and the SUIB bus, and controls the SUIB read/write cycles.

The SUIB and the cycles run on the SUIB are unchanged from the design of the SMP20, except that longword (thirty-two-bit) accesses to sub-units connected via the SUIB are no longer available, as the 68040 does not do dynamic bus sizing. (In the SMP20, the 68020 processor performed dynamic bus sizing, which automatically split longword accesses to the sub-units into multiple word accesses). Only word (sixteen-bit) accesses are supported. There is no pipelining performed by the SUIB interface. The RS bus read and write cycles complete only after the SUIB cycles complete. The I/O timer must be running to initiate both write and read subunit cycles. Each subunit receives an individual select, wait and interrupt lead (the interrupt leads are not terminated on the APC). The SUIB consists of the following signals:

- six Sub-Unit Address (SUA) bits (SUA01 - SUA06),
- one Sub-Unit Address Parity (SUAP) bit (odd parity),
- sixteen Sub-Unit Data (SUD) bits (SUD00..SUD15),
- two Sub-Unit Data PARity (SUDPAR) bits, one per byte (even parity) [Sub-Unit Data PARity High (SUDPARH), Sub-Unit Data PARity Low (SUDPARL)],
- one Sub-Unit ReaD (SURD) signal,
- one Sub-Unit WRite (SUWR) signal,
- eight Sub-Unit SELect (SUSEL) signals, one per sub-unit (SUSEL0..SUSEL7),
- eight Sub-Unit WaiT (SUWT) signals, one per sub-unit (SU0WT..SU7WT), and
- eight sub-unit interrupt signals, one per sub-unit (not terminated on the APC).

Address parity and write data parity from the RS bus are checked, prior to the initiation of a SUIB cycle, by the RS Bus Interface. If an address parity error or write data parity error is detected on the RS bus, the cycle is invalidated. (It is completed, but no writes will be performed, and any read data will be invalid.)

During a sub-unit cycle, a sub-unit that asserts but fails to release the wait lead will generate a ready timeout error in the system. When this happens, the RS bus cycle is forced to terminate by the processor, which causes the sub-unit cycle to be terminated by the APC.

All sub-unit wait signals are latched in the Sub-Unit Ready register at the end of each sub-unit cycle. This register can be read by software to determine the sub-unit that failed to release the wait lead.

The sub-unit select leads are also monitored to ensure that no more than one lead can be active (to detect stuck-at and similar faults on the leads).

On sub-unit read cycles, the data from the sub-unit is checked for even parity. The parity is computed so that the sum of bits set to a logic one in each byte (including the parity bit) is even. The read data parity received from the SUIB is passed on to the RS bus.

*7. TEST UTILITY BUS (TUB)*

The SMPU4 contains one circuit pack slot that is used for testing and uses the TUB Interface residing on the CORE40. This interface provides the connection to the UN364-DUS/SMITS test circuit pack when the SMPU4 is in a unit test or lab test environment, and is externally powered from an associated paddle board (L567902) on the back of the test slot.

Depending on the type of mode the circuit pack is configured for, the test slot is used for unit test or software testing. The DUS mode is used during unit hardware testing, and the SMITS mode is used during software testing. SMITS permits a user to examine and modify the execution of a program, and accommodates step-by-step execution of target programs, the setting of breakpoints, and the running of error detection programs. Additional test cables are required when using DUS or SMITS in a duplex environment.

The TUB interface consists of a thirty-two-bit multiplexed address and data bus, along with the control signals necessary to perform operations over the TUB. The TUB signals are as follows:

| | |
|---|---|
| TAD[0:32]: | Test Address/Data (TAD) bus - bi-directional Address/Data bus for operations to the DUS/SMITS utility board. |
| TADP [M][LH]: | Test Address/Data Parity (TADP) - bi-directional parity bits for each byte of Address/Data transferred. |
| TSIZ[0:1]: | Test utility bus transfer SIZe (TSIZ) indicator. Byte, Word, and Long Word only. No Burst transfer capability on the TUB. |
| TSAL: | TeSt Address Latch (TSAL) - output that indicates the address should be latched on the TUB. |
| TDS: | Test Data Strobe (TDS) - output that indicates that it is safe to accept/drive data from the multiplexed TAD bus. |
| TSAK: | TeSt AcKnowledge (TSAK) - input that indicates the requested test utility bus access has completed. |
| TRAMEN: | Test Random Access Memory ENable (TRAMEN) - output |

that functions as a RAM select for accessing the RAM that may be accessed as Pseudo-ROM on the DUS/SMITS board.

TIOEN: Test utility Input/Output ENable (TIOEN) - output that functions as a board select for the DUS/SMITS circuit pack.

TMONINV: Test MONitor INVoke (TMONINV) - input that generates a NMI to the MC68040 microprocessor to invoke SMITS or DUS code.

TPWRUP0: Test PoWeR-UP (TPWRUP) - output that indicates that a power-up has occurred.

TWPSPIH: Test Write Protect and Stack Protect InHibit (TWPSPIH) - inputs used to disable all write and stack Protect by disabling the MMU on the CORE40.

TTIMINH: Test TIMer INHibit (TTIMINH) - input used by SMITS to disable all timers in the SMP40. Including the Billing Counter, the Sanity Timer, the 10 Msec. timer, the 10 Msec. Interval counter, the spare miscellaneous timer, and the Conditional Suspend Timer.

TPSROM: Test PSeudo-Read-Only Memory (TPSROM) - input that indicates that Pseudo-ROM is to be invoked.

SMTSEQ: Switching Module integrated Test System EQuipped (SMTSEQ) - input that indicates the presence of a SMITS circuit pack.

SMTSMD: Switching Module integrated Test System MoDe (SMTSMD) - input to indicate the current SMITS Mode of operation, Integrated Test System (ITS), or DUS/CTS.

SMTSACT: Switching Module integrated Test System ACTive (SMTSACT) - input which indicates that a SMITS Session is currently active.

MSTR/SLV: MaSTeR (MSTR)/SLaVe (SLaVe) - indicates the current operating mode is master/slave.

ATRK: Auto TRAck (ATRK) - input indicates the SMITS auto tracking

circuit has tracked to this processor.

SMTSDG: Switching Module integrated Test System DiaGnostic request (SMTSDG) - input indicates that the SMITS software on the SMP should diagnose the TUB from the SMP side.

SMAPP: Switching Module integrated test system APPlication spare bit (SMAPP) - input for future definition.

TRESET: Test RESET (TRESET) - input used to provide a reset to the microprocessor only via TUB.

TRESTRT: Test RESTaRT (TRESTRT) - input used to initiate a power-up sequence in the CORE40 by SMITS.

TACT: Test ACTive indicator (TACT) - output that provides the Active status of module processor. This signal is active only if the processor is executing code and the A-FF is on.

TRDRQ: Test ReaD ReQuest (TRDRQ) - output that initiates a read operation over the TUB.

TWRTRQ: Test WRiTe ReQuest (TWRTRQ) - output that initiates a write operation over the TUB.

TRUN: Test RUN (TRUN) - output that provides the RUNNING status to the Test Utilities.

### *8. GROUND LUGS*

Ground connections between the two backplanes of the SMPU4 appear in CAD 2.

### *9. WIRING FOR GROWTH*

The SMPU4 contains a spare slot in each shelf for an additional circuit pack, if required in future applications. This circuit pack slot contains wiring similar to the MH slots (RS Bus) and is located at 04-088 in the unit.

## *SECTION V - REFERENCE DATA*

### *1. UNIT LAYOUT*

The SMPU4 is considered to be a single-shelf unit containing two versions of backplanes (ED-5D517-30 and ED-5D518-30). It functions as a duplexed entity, with two units required, each with a different backplane code. Side 0 (ED-5D517-30) is contained in the lower shelf, and Side 1 (ED-5D518-30) is contained in the upper shelf. The SMP40 is housed in a two-shelf unit. Figure 2

depicts the physical circuit pack layout of the SMP40. A maximally-equipped simplex unit contains two 410AA (300 Watt) bulk power modules, one SN516B Control and Display pack, one CORE40 pack, four MEM32 packs, one BSN pack, three MH packs, one spare slot, one APC pack, one PI pack, and four CI packs. A test slot is provided in the unit to facilitate circuit and system lab testing. In the field, this slot is unequipped.

Equipment locations and functional designations for all component codes in the SMPU4 are shown in Table 1.

*2. WORKING LIMITS*

Voltages:

a. +5±0.5 volts

b. -48 volts +7.5, -9 volts

Ambient Temperature:

a. 0 to 55 degrees Centigrade (operational).

b. -5 to 55 degrees Centigrade (no damage).

Growth:

The spare slot (04-088) in SMPU4 can be used for future applications, and contains basically the same signals that are used on the MH slots (RS Bus).

*3. FUNCTIONS*

The function of this unit is described in Section II of this Circuit Description.

*4. CONNECTING CIRCUITS*

The connecting circuits listed were valid at the time this was written and may not reflect existing connecting circuits that have been Manufacture Discontinued (MDed) or any new connecting circuits that have been introduced. When this circuit is listed on an application schematic, the connecting information is to be followed.

The main connecting circuits are:

a. Time Slot Interchange Unit - SD5D196-01,

b. Digital Service Group - SD5D197-01,

c. Mid-Cabinet Fan Unit - SD5D168-01, and

d. Fuse/Filter Unit - SD5D190-01.

The Peripheral Units are:

a. Line Unit 3/E3 - SD5D180-01,

b. Integrated Services Line Unit/2 - SD5D091-01,

c. Remote Integrated Services Line Unit/2,

d. Trunk Unit - SD5D300-01,

e. Analog Trunk Unit/E2/AC15,

f. Digital Line/Trunk Unit 2/3/RH - SD5D201-01,

g. PPMU-E/2,

h. FPPMU,

i. Integrated Digital Carrier Unit (TR08/TR303),

TABLE 1. SMPU4 Component Equipment Locations And Functional Designations.

| EQL | FDESIG | MEANING | CIRCUIT PACK CODE |
|---|---|---|---|
| 04-006 | (0,1)UNITTST | UNIT TEST SLOT | - |
| 04-018 | (0,1)PRS | POWER CONVERTER | 410AA |
| 04-028 | (0,1)CD | CONTROL/DISPLAY | SN516B |
| 04-036 | (0,1)C40 | CORE40 | UN540 |
| 04-044 | (0,1)MEM0 | MEMORY BOARD 0 | TN1685 |
| 04-052 | (0,1)MEM1 | MEMORY BOARD 1 | TN1685 |
| 04-060 | (0,1)MEM2 | MEMORY BOARD 2 | TN1685 |
| 04-068 | (0,1)MEM3 | MEMORY BOARD 3 | TN1685 |
| 04-077 | (0,1)BSN | BUS SERVICE NODE | KBN8 |
| 04-088 | (0,1)SS | SPARE SLOT | - |
| 04-096 | (0,1)MH0 | MESSAGE HANDLER 0 | UN538 |
| 04-104 | (0,1)MH1 | MESSAGE HANDLER 1 | UN538 |
| 04-112 | (0,1)MH2 | MESSAGE HANDLER 2 | UN538 |
| 04-122 | (0,1)APC | APPLICATIONS CONTROLLER | UN539 |
| 04-130 | (0,1)PI | PACKET INTERFACE | TN1042 |
| 04-138 | (0,1)CI0 | CONTROL INTERFACE 0 | UN71B |
| 04-146 | (0,1)CI1 | CONTROL INTERFACE 1 | UN71B |
| 04-154 | (0,1)CI2 | CONTROL INTERFACE 2 | UN71B |
| 04-162 | (0,1)CI3 | CONTROL INTERFACE 3 | UN71B |
| - | TF | TERMINAL FIELD | - |
| - | LUG | POWER/GROUND LUG | - |

j. Packet Switch Unit (PH1/2/3) - SD5D074-01,

k. Modular Metallic Service Unit - SD5D015-01,

l. Modular Metallic Service Unit-E/2,

m. Remote Modular Metallic Service Unit,

n. Directly Connected Test Unit - SD2P077-01,

o. Global Digital Service Unit,

p. Echo Canceler number 5 Signaling Unit - SD5X213-01,

q. Transmission Rate Conversion Unit 2, and

r. Remote Switch Module.

## 5. *REFERENCES*

Supplementary information is contained in the following documents:

a. Switching Module Fuse/Filter Unit - CD-5D190-01,

b. Switching Module Fan Unit - CD-5D168-01,

c. Time Slot Interchange Unit - CD-5D196-01,

d. Digital Service Unit - CD-5D197-01,

e. CPSM-410AA,

f. CPSM-SN516B,

g. CPSM-UN540,

h. CPSM-TN1685,

i. CPSM-KBN8,

j. CPSM-UN538,

k. CPSM-UN539,

l. CPSM-TN1042, and

m. CPSM-UN71B.

*6. ACRONYMS*

| | |
|---|---|
| A-FF | A Flip-Flop |
| AFFCLK | A Flip-Flop CLocK |
| ACK | ACKnowledge |
| ALE | Address Latch Enable |
| ALM | ALarM |
| AM | Administrative Module |
| APC | APplications Controller |
| APCERR | APplications Controller ERRor |
| APTS | Active Pump Time Slot |
| ASCII | American Standard Code for Information Interchange |
| ASW | All Seems Well |
| ATRK | Audio TRacK |
| B-bus | Buffer bus |
| BCR | Bus Control Register |
| BDL | Bootstrapper Dual Link |
| BRAM | Buffer Random Access Memory |
| BRICPIT | Bit Register Interrupt Controller Programmable Interval Times |
| BSN | Bus Service Node |
| BSN_CKWP | Bus Service Node CheckWrite Protect |
| BSN_MCAS | Bus Service Node Miscellaneous Control And Status |
| BSN_PARM | T{ Bus Service Node PARity Maintenance |
| BSN_RSMS | Bus Service Node Remote Switching Module Status |
| BSN_SWP | Bus Service Node Set Write Protect |
| BTSR | BooTStrappeR |
| CAD | Computer-Aided Drawing |
| CAS | Customer Account Service |
| CAS2 | Customer Account Service Release 2 |
| CI | Control Interface |
| CLEI | Common Language Equipment Identifier |
| CM | Communication Module |
| CORE40 | CORE circuit pack containing a 68040 processor |
| CPI | Central Processor Intervention |
| CTS | Control Time Slot |
| CRC | Cyclic Redundancy Check |
| DCLU | Digital Carrier Line Unit |
| DLE | Data Latch Enable |
| DLI | Dual Link Interface |
| DLTU | Digital Line and Trunk Unit |
| DMA | Direct Memory Access |
| DMI | Dual Message Interface |
| DRAM | Dynamic Random Access Memory |
| DSU | Digital Service Unit |
| DUS | DEMON Utility System |
| ECL | Emitter Coupled Logic |

| | |
|---|---|
| EDC | Error Detection Correction |
| EPROM | Erasable Programmable Read Only Memory |
| ESBR | Event Source Bit Register |
| ESR | Error Source Register |
| FFU | Fuse/Filter Unit |
| FIFO | First In, First Out |
| FMWXLE | From Mate WX Latch Enable |
| FPU | Floating Point Unit |
| GDX | Gated Diode Crosspoint |
| GPITS | General Purpose Integrated Test System |
| HDLC | High-level Data Link Control |
| I/O | Input/Output |
| ID | IDentification |
| IER | Interrupt Enable Register |
| IMBR | Interrupt Mask Bit Register |
| ISDN | Integrated Services Digital Network |
| ISLU | Integrated Services Line Unit |
| ISRR | Interrupt Source Request Register |
| ITS | Integrated Test System |
| L-bus | Local bus |
| LED | Light-Emitting Diode |
| LP | Local Processor |
| LRAM | Local Random Access Memory |
| LS | Local System |
| LSACK | Local System ACKnowledge |
| LSAD | Local System Address/Data |
| LSADP | Local System Address/Data Parity |
| LSAL | Local System Address Latch |
| LSD | Local System Data |
| LSDP | Local System Data Parity |
| LSDS | Local System Data Strobe |
| LSIZ | Local system SIZe |
| LSRDRQ | Local System ReaD ReQuest |
| LSWRTRQ | Local System WRiTe ReQuest |
| MCP | Messaging, Central processor intervention, and Pump |
| MCTU2 | Module Controller and Time slot interchange Unit 2 |
| MD | Manufacturer Discontinue |
| MEM_CBC | MEMory Correctable Bit Count |
| MEM_CBT | MEMory Correctable Bit Threshold |
| MEM_CTRL | MEMory ConTRoL |
| MEM_ESR | MEMory Error Source Register |
| MEM_ID | MEMory IDentification |
| MEM_MESR | MEMory Mask Error Source Register |
| MEM_STAT | MEMory STATus |
| MEM32 | MEMory circuit pack, 32 megabyte |
| MH | Message Handler |
| MISC2 | MISCellaneous 2 |
| MMU | Memory Management Unit |
| MPF | Mate Power Fail |
| MSGS | MeSaGe Switch |
| MSRSP | Memory System size ReSPonse |
| MSTR | MaSTeR |
| NMI | Non-Maskable Interrupt |
| NOP | No OPeration |
| OOS | Out Of Service |

| | |
|---|---|
| PB | Packet Bus |
| PCM | Pulse Code Modulation |
| PH | Protocol Handler |
| PI | Packet Interface |
| PIC | Programmable Interrupt Controller |
| PICB | Peripheral Interface Control Bus |
| PP | Port Processor |
| PREAFF | PRE-A Flip-Flop |
| PSU | Packet Switch Unit |
| PWRCTRL | PoWeR ConTRoL |
| QLPS | Quad Link Packet Switch |
| QLW | Quad Long Word |
| RAM | Random Access Memory |
| REQ | REQuest |
| ROM | Read Only Memory |
| ROS | Request Out of Service |
| RQIP | ReQuest In Progress |
| RS | Remote System |
| RSACK | Remote System ACKnowledge |
| RSAD | Remote System Address/Data |
| RSADP | Remote System Address/Data Parity |
| RSAL | Remote System Address Latch |
| RSBR | Reset/Set Bit Register |
| RSD | Remote System Data |
| RSDP | Remote System Data Parity |
| RSDS | Remote System Data Strobe |
| RSIZ | Remote system SIZe |
| RSM | Remote Switching Module |
| RSRDRQ | Remote System ReaD ReQuest |
| RST | ReSeT |
| RSWRTRQ | Remote System WRiTe ReQuest |
| SA | SPYDER-T Attention |
| SFMR | Special Function Maintenance Register |
| SLV | SLaVe |
| SM | Switching Module |
| SM-2000 | Switching Module 2000 |
| SMAPP | Switching Module integrated test system APPlication spare bit |
| SMC | Switching Module Control |
| SMITS | Switching Module Integrated Test System |
| SMP | Switching Module Processor |
| SMPU4 | Switching Module Processor Unit, model 4 |
| SMR | Special Memory Region |
| SMTSACT | Switching Module integrated Test System ACTive |
| SMTSDG | Switching Module integrated Test System DiaGnostic request |
| SMTSEQ | Switching Module integrated Test System EQuipped |
| SMTSMD | Switching Module integrated Test System MoDe |
| SP | Signal Processor |
| SRP | Supervisor Root Pointer |
| SRAM | Static Random Access Memory |
| STCL | Serial Time slot interchange Control Link |
| SUA | Sub-Unit Address |
| SUAP | Sub-Unit Address Parity |
| SUD | Sub-Unit Data |
| SUDPAR | Sub-Unit Data PARity |
| SUDPARH | Sub-Unit Data PARity High |
| SUDPARL | Sub-Unit Data PARity Low |
| SUIB | Sub-Unit Interface Bus |
| SURD | SubUnit ReaD |
| SUSEL | Sub-Unit SELect |
| SUWR | SubUnit WRite |

| | |
|---|---|
| SUWT | SubUnit WaiT |
| SW | SoftWare |
| TACT | Test ACTive indicator |
| TAD | Test Address/Data |
| TADP | Test Address/Data Parity |
| TAS | Test And Set |
| TDS | Test Data Strobe |
| TIOEN | Test utility Input/Output ENable |
| TMONINV | Test MONitor INVoke |
| TMS | Time Multiplexed Switch |
| TPSROM | Test PSeudo-Read-Only Memory |
| TPWRUP | Test PoWeR UP |
| TRAMEN | Test Random Access Memory ENable |
| TRESET | Test RESET |
| TRESTRT | Test RESTaRT |
| TRUN | Test RUN |
| TSAK | TeSt AcKnowledge |
| TSAL | TeSt Address Latch |
| TSI | Time Slot Interchange |
| TSI-COM | Time Slot Interchanger-Common |
| TSIU | Time Slot Interchange Unit |
| TSIZ | Test utility bus transfer SIZe |
| TTIMINH | Test TIMer INHibit |
| TTR | Transparent Translation Register |
| TUB | Test Utility Bus |
| TWPSPIH | Test Write Protect and Stack Protect InHibit |
| TWRTRQ | Test WriTe ReQuest |
| UPA | User Page Attributes |
| UPAD | UPdate Address/Data |
| UPD | UPdate Data |
| UPDPH | UPDate Parity High |
| UPDPL | UPDate Parity Low |
| UPDPMH | UPDate Parity Medium High |
| UPDPML | UPDate Parity Medium Low |
| UPGO | UPdate second data GO |
| UPH | Update Parity High |
| UPL | Update Parity Low |
| UPMH | Update Parity Middle High |
| UPML | Update Parity Middle Low |
| UPQLW | UPdate Quad Long Word |
| UPRDRQ | UPdate ReaD ReQuest |
| UPSIZ | UPdate SIZe |
| UPWTRQ | UPdate WriTe ReQuest |
| UPWAIT | UPdate WAIT |
| URP | User Root Pointer |
| URW | Update Read Write |
| USIZ | Update SIZe |

**AT&T BELL LABORATORIES**

DEPT 55535-DAS-CEJ

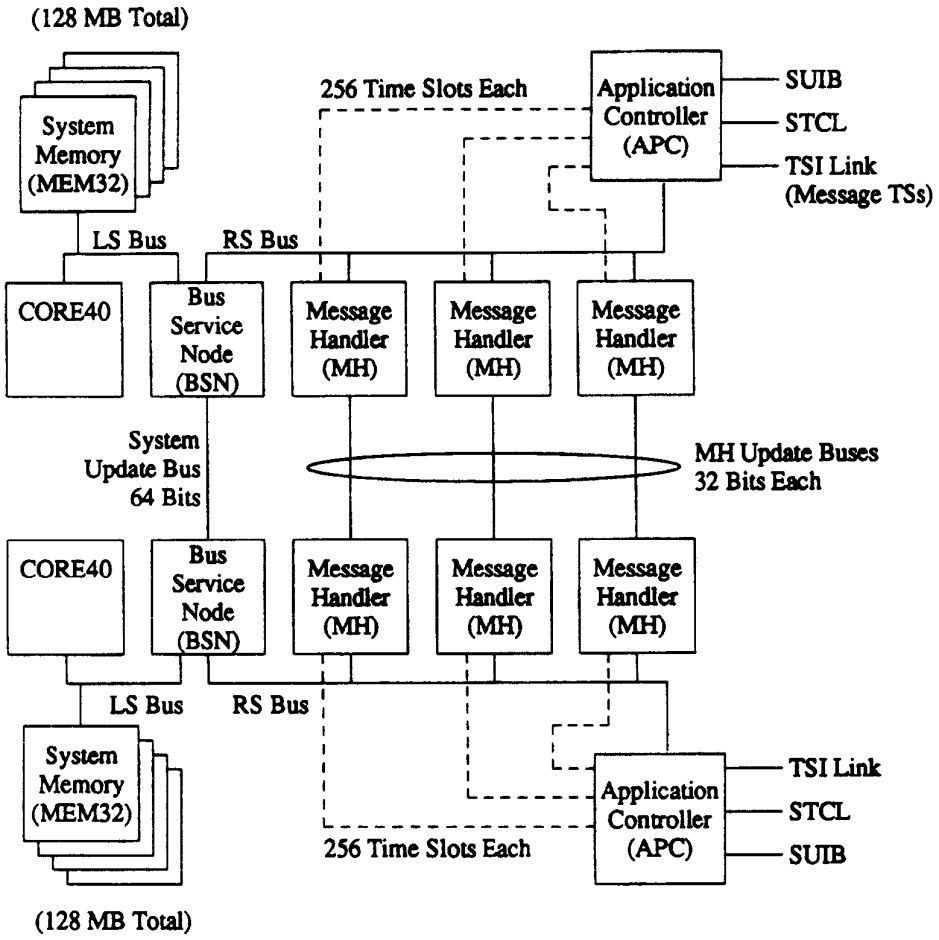
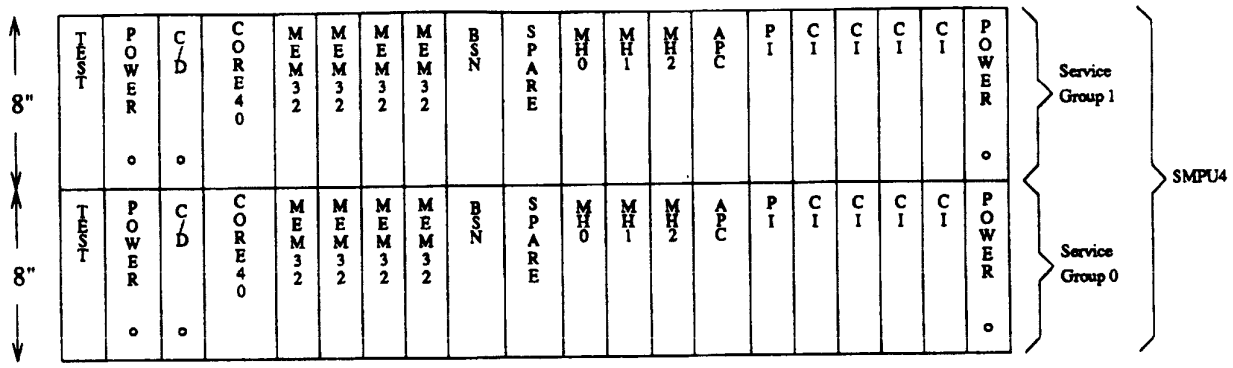



**Figure 1.** SMP40 Architecture Block Diagram.




| | | |
|---|---|---|
| TEST | - UN364 | - Switching Module Integrated Test System (SMITS) |
| POWER | - 410AA | - 300 Watt Power Converter |
| C/D | - SN516 | - Control/Display |
| CORE40 | - UN540 | - Processor Core w/MC68040 |
| MEM32 | - TN1685 | - 32 MByte Memory |
| BSN | - KBN8 | - Bus Service Node |
| MH | - UN538 | - Message Handler |
| APC | - UN539 | - Applications Controller |
| PI | - TN1042 | - Packet Interface |
| CI | - UN71B | - Control Interface |

o Out Of Service Indication

**Figure 2.** SMP40 Unit Layout.