5ESS® SWITCHING SYSTEM
TIME SLOT INTERCHANGE UNIT
MODEL 4 (TSIU4)
CIRCUIT

Description of Changes

1.

The following general rule is to be applied throughout the Circuit Description:
All references to TSICOM UM74 also apply to the revised version UM74B.

2. GENERAL CAPABILITIES

This information is to be appended to Section 1.1.4:

In addition to NLI paddle boards and DX packs, network/peripheral interface is availible via NLI1 paddleboards for CM2C, ENLI paddleboards for EXM2000, and PLI paddleboards for DNU-S.

This information is to be appended to Section 1.1.6:

In addition, provides capability to access an external DS1 or CEPT1 clock source for stand alone operation should network clocking be lost or not applicable.

3. PERIPHERAL INTERFACE

This information is to be appended to Section 1.4:

9. Provides the capability to terminate optical PCT links carrying 768 whole timeslots in duplexed arrangement with the use of PLI paddleboards on duplex TSI links.

This information to be appended to Section 1.5:

7. Provides connections through a duplex TSI link to duplex NLI1 paddleboards. Each NLI1 terminates one NCT link. One NLI1 will be connected to CM2C Side 0 and one to CM2C Side 1.

8. Provides connections through a duplex TSI link to duplex ENLI paddleboards for EXM2000 applications. Each ENLI terminates one electrical NCT link to an associated remote TRCU2 circuit.

4. BLOCK DIAGRAM OVERVIEW

This information is to be appended to Section 2:

Not shown in the figure are additional network/peripheral (NCT/PCT) links utilizing the following paddleboards:

PLI The paddleboard that terminates one PCT link, which carries 768 whole time slots, and converts the data from electrical to optical format.

ENLI The paddleboard that terminates one NCT link for Extended Switching Module applications, carrying 256 whole time slots in electrical format.

5. TSICOM DESCRIPTION

This information is to be appended to Section 2.3:

Not shown in the figure is an additional feature incorporated into the revised TSICOM pack, UM74B.

7. Accept external timing reference from either a DS1 or CEPT1 clock source.

6. MISCELLANEOUS CIRCUIT EQUIPMENT

This information is to be appended to Section 4.2.1:

For VCDX2000 and AWS/SM2000 applications, the CTSNS paddle boards are still equipped, with switches set as if the SM was linked to a CM. The software for these applications does not read the registers at this time.

This information is to be appended to Section 4:

4.6 DX/TSIS Flexible Link Cables

Any TSIS port and any DX port (1-5) can also be connected by means of a DX/TSIS Flexible Link cable. These can be used in combination with the DX/TSIS Jmpr Boards or independently. Side 0 and Side 1 equipage must be identical with either connection method.

4.6.1 Software Interface

There is no software interface for the DX/TSIS Flexible Link cables.

4.7 24/30 Channel Mode Selection Jumper

Used in conjunction with the an external timing source, the 24/30 channel mode jumper enables the T1 or E1 clock mode. 24 channel (T1) is default without the jumper. 30 channel (E1) with jumper installed. Installed on pins 532-533 of the TSICOM (Side 0 and Side 1) if equiped.

4.7.1 Software Interface

The status of the 24/30 channel mode jumper is availible to software via the clock control register CMCR.

7. PERIPHERAL LINK INTERFACE

This information is to be appended to Section 5.1:

5.1.9 Peripheral Link Interface - PLI

The PLI provides for one PCT link connection between the SM and an optical peripheral. Any TSI port, except the first two primary NCT ports, can be used for a PCT link.

INTERFACE SPECIFICATIONS:

Connection Type: Point to Point - PLI to optical paddleboard
Speed: 65.536Mhz continuous
Driver/Receiver Technology: 850nm wave length, LED transmitter, PIN diode receiver.
Cable Type: 62.5 micron multi-mode fiber
Connector Type: AT&T - ST/bayonet
Approximate Distance: 0-2000 ft.
Number of Conductors: 2 (transmit,receive)

5.1.10 ELECTRICAL NETWORK LINK INTERFACE - ENLI

The ENLI is very similar to the NLI design with the exception of electrical rather than optical interface. The ENLI provides for one NCT link between the SM and transmission equipment (TRCU2). The links, A and B, carry 256 PCM time slots, timing references, and CTS data.

INTERFACE SPECIFICATIONS:
Connection Type: Point to Point - ENLI to DS3 (TN1345)
Speed: 32.768Mhz continuous
Driver/Receiver Technology: FAST - TTL
Cable Type: shielded twisted pair
Connector Type: 982BM paddleboard
Approximate Distance: 0-4 ft.
Number of Conductors: 8 (4 pair)

5.1.11 EXTERNAL CLOCK SOURCE INTERFACE

The external clock source feature allows the TSICOM pack to receive a DS1 or CEPT1 transmission carrier timing reference directly should the CM timing reference be lost or not applicable.

INTERFACE SPECIFICATIONS:
Connection Type: Point to Point - BITS, DFI2, or Dig. Cross Connect to TSICOM
Speed: E1 or T1 reference (2.048MHz or 1.544MHz)
Receiver Technology: transister coupled, 7290 Line Interface
Cable Type: shielded twisted pair
Connector Type: 982AB paddleboard
Approximate Distance: 0-450 ft.
Number of Conductors: 4 (2 pair)

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5ESS® SWITCHING SYSTEM
TIME SLOT INTERCHANGE UNIT
MODEL 4 (TSIU4)
CIRCUIT

Description of Changes

There are no changes to the circuit description (CD) for issue 3M of the schematic drawing (SD), SD5D196-01.

AT&T BELL LABORATORIES

DEPT NA5350300-MGS-FNG

5ESS® SWITCHING SYSTEM
TIME SLOT INTERCHANGE UNIT
MODEL 4 (TSIU4)
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1. HIGH LEVEL OVERVIEW

The following sections provide a high level overview of the TSIU4's capabilities.

1.1 GENERAL CAPABILITIES

The TSIU4:

1. Is configured as two service groups, in order to provide a reliable switching network. A failure in one service group does not cause a failure in the other service group. Each TSIU4 service group is a part of one of the switching module processor unit, model 4 (SMPU4) failure groups.
2. Receives an indication of which service group is active from the SMPU4.
3. Provides a growable switching network that, when fully equipped, allows for the interconnection of at least 30,000 time slots. Some of these time slots are reserved to transport messages between the switching module processor unit (SMPU4) and the rest of the switch and other time slots will be used for access to the local digital service function (LDSF). The reserved time slots are not available for carrying subscriber traffic.
4. With the exceptions of the time slots that are dedicated for use with the primary network control and timing, version 2 (NCT2) links and the messaging central processor intervention and pump (MCP) link, any group of time slots can be used as either network or peripheral time slots. Thus, there is flexibility in mixing network link interface (NLI) paddle boards and duplex (DX) circuit packs. All time slots are completely free to be used as either network or peripheral data.
5. Terminates from eight (the minimum number required for the LDSF (DSC3)) to 144 peripheral interface data buses (PIDBs).
6. Provides a stratum 4 clock reference that is synchronized to the timing reference received from the communications module (CM) over one of the primary NCT2 links. The selection of the timing source is under software control.
7. Provides two backplane dip switches that specify the time slot interchange (TSI) link byte numbers used to carry the control time slots (CTSs) from the primary NCT2 links. One dip switch specifies the TSI link byte number for the link carrying even numbered time slots. The other dip switch specifies the TSI link byte number for the link carrying odd numbered time slots.

1.2 SWITCHING NETWORK

The TSIU4:

1. Connects any peripheral time slot to any network time slot in either direction. It also provides the capability for non-blocking peripheral-to-peripheral and network-to-network connections.
2. Provides the capability to either single or double buffer time slots, selectable on a per time slot basis, to allow wideband connections (n x 64 kb/s) while ensuring frame integrity.
3. Provides the capability to fan out an input time slot to any number of output time slots.
4. Provides an alternate data capability to independently source constant pulse coe modulation (PCM) data and/or A-D signaling bits, and/or E-G signaling bits to outgoing time slots selectable on a per time slot basis. A minimum of 32 different constant PCM values are simultaneously available. The constant PCM values are programmed by software. *This ability can be used to source μ-law and A-law idle code.*
5. Provides, on a per time slot basis, programmable attenuation, ranging from 0 to 15.5 dB in 0.5 dB steps, or programmable amplification, ranging from 0 to 15.5 dB in 0.5 dB steps, for outgoing time

slots with μ-law or A-law PCM companding. At the same time it provides the ability to perform translation from μ-law to A-law or A-law to μ-law format at any attenuation or amplification level. The above is available for both peripheral and network time slots.

6. Provides the ability to loop an outgoing time slot back into the TSI on the same time slot number with zero relative time slot skew. This operational loopback switch is controllable on a per time slot basis.

7. Provides the ability to source idle code for any number of time slots as they exit from the TSIU4. This idle code insertion is located after the operational loopback switch, so that a time slot may be looped and optionally stuffed with idle code as it leaves the TSIU4. Idle code may also be optionally stuffed into time slots which are not looped.

1.3 SIGNAL PROCESSOR

The Signal Processor (SP) in the TSIU4:

1. Provides the ability to detect valid state changes for the A-G signaling bits on all time slots, both network and peripheral, that terminate on the Switching Module-2000 (SM-2000). The SP monitors signaling bit state changes for time slots that are looped by the operational loopback switch (S4 in Fig. 5) as they leave the TSIU4, by receiving the data from the actual source (not the looped data).

2. Provides, on a per time slot basis, the ability to select between a fixed bit timing algorithm (two successive 3 ms samples) and a programmable bit timing algorithm to be used to validate signaling bit state changes. The programmable time can be independently set on a per time slot basis to be in the range from 10 ms to 310 ms. Two time values shall be available for each time slot, one to be used for high-to-low transition timing (on-hook) and the other to be used for low-to-high transition timing (off-hook).

3. Provides the ability to turn off the reporting of signaling bit transitions for an entire TSI link by writing a single control register. When this ability to turn off the reporting is activated, it is required to continue to maintain and validate the state of the signaling bits.

4. Provides the ability to ignore state changes of some or all of the signaling bits (any combination), on a per time slot basis.

5. Uses a first-in first-out (FIFO) for storing and reporting signaling bit state changes.

6. Provides the ability for software to read the latest value of the signaling bits received from any time slot.

7. Gives software the ability to read the latest valid state of the signaling bits for any time slot.

8. Provides software with the ability to force the reporting of a signaling bit state change for any time slot. This ability is provided for both of the bit timing algorithms.

9. As a part of its actions in response to a reset, it automatically sets all of the internal control RAMs to the value that causes all signaling bit state changes to be ignored.

1.4 PERIPHERAL INTERFACE

The TSIU4:

1. Provides data, clock, and synchronization for peripherals (such as the analog Line Unit) that connect to the SM-2000 switching fabric through PIDBs. The two TSIU4 service groups generate PIDBs whose clock signals have a phase difference of less than 60 ns, provided the PIDB cables are the same length. The phase difference between the clocks of any two PIDBs generated by the same TSIU4 service group is less than 60 ns, provided the PIDB cables are the same length.

2. Allows a PIDB maximum cable length of 28 feet.
3. Uses a walking parity generation and checking scheme to ensure the integrity of the data transmitted over PIDBs.
4. Provides for the reporting of PIDB parity errors on a per time slot basis from peripherals that use PIDBs.
5. Provides the capability to disable, on a per time slot basis, parity checking on PIDB time slots to accommodate peripheral units that are unequipped or have known faults.
6. Provides software the ability to ignore parity transmitted over a group of PIDBs (PIDBs that terminate on the same TSIU4 circuit pack) by writing a single control register.
7. Provides a 2:1 data fan-in selection switch to allow software the ability to fan-in data from one PIDB time slot to the same time slot number on its adjacent PIDB. The data fan-in switch is controlled on a per time slot basis, independent of the data fan-out switch.
8. Provides the ability for software to fan-out data from one PIDB time slot to the same time slot number on its adjacent PIDB. This data fan-out switch is controlled on a per time slot basis, independently of the data fan-in switch.

1.5 NETWORK INTERFACE

The TSIU4:

1. Provides connections through a duplex TSI link to duplex NLI paddle boards. Each NLI terminates one NCT2 link. One NLI will be connected to CM side 0, and one NLI will be connected to CM side 1.
2. Provides the capability to select, as a default, which of the duplex NLIs to accept data from.
3. Provides the automatic time slot switching (AUTISS) function to autonomously select on a per time slot basis, based on the state of the E signaling bit, which NLI to use as the source for time slot data.
4. Provides the capability to select which of the duplex NLIs to use as the source for the clock. Data can be selected from one NLI while using the clock from the other NLI.
5. Provides the capability to select which of the pair of duplex NLIs that terminate the primary NCT2 links to accept clock synchronization signals from.
6. Provides software with an indication that at least one time slot in each of the last 256 frames has been switched by AUTISS. Software can program which time slots will be used when determining this indication.

1.6 SMPU4 INTERFACE

The TSIU4:

1. Provides, through one simplex TSI link (known as the MCP link), the means to transport, without the need for software control, the four CTSs including the central processor intervention (CPI) bit, between the four primary NCT2 links and the SMPU4. Prior to inserting the CTSs onto the MCP link or a TSI link, the TSIU4 reverses the order of the CTS's PCM bits.
2. Provides the means to transport to and from the APC, any other time slots, up to a maximum number of 764. These slots can be used for pumping the SMPU4 software image and for communication with the rest of the switch.

3. Provides software with read access of PCM sample and signaling bits for any input time slot stored on a slice. The latency between when the time slot number to be read is requested and when the time slot data is valid is less than 10 μs.
4. Provides a clock reference to the SMPU4 which is used as a timing source for call billing.
5. Provides the ability to read the TSI link time slot numbers that are being used to transport CTSs.
6. Provides software with the ability to specify the TSI link byte numbers that will be used to transport CTSs when the CTS dip switches are not equipped.
7. Provides read-modify-write operations on all control RAMs.
8. Provides software with the ability to independently read and write the registers that are contained in the duplex NLI paddle boards. These indirect accesses of the paddle boards are transmitted over the TSI link using the overhead bytes that are assigned for this purpose.
9. Provides a mask register for the error source registers' (ESRs) outputs. Setting the corresponding bit in the error mask register (EMR), prevents a selected error source from generating an interrupt. ESR bits are set when errors occur regardless of the EMR contents. Software has read and write access to the ESR. Reading the ESR does not affect its contents. To clear the ESR, the software must write it to zero. The active value for all ESR bits is 1 (active high),
10. Contains a TSIU4 SP service request register. Each circuit pack that contains an SP is mapped to one bit in this register. When an SP on a circuit pack has at least one report in its FIFO, the corresponding bit in the TSIU4 SP service request register will become active. There also is a TSIU4 SP service request mask register. Finally, there is a TSIU4 SP masked service request register. Each bit in the TSIU4 SP masked service request register will be determined by performing the logical AND operation on the corresponding bits in the SP service request register and the SP service request mask register. The active value for the bits in the SP service request and SP masked service request registers is 1 (active high), i.e., a set bit indicates that the FIFO in the SP contains entries which have not been read.
11. Contains a TSIU4 summary interrupt source register (ISR). Each circuit pack in the unit is assigned one bit in the ISR for maintenance error reports. There also is a bit in this register that becomes active whenever one or more bits are active in the TSIU4 SP masked service request register. There also is a TSIU4 summary interrupt mask register (IMR). The active value for the bits in the ISR is 1 (active high).
12. Activates an output lead whenever one or more unmasked bits are active in the ISR. This is the TSIU4 interrupt signal for the SMPU4.
13. Provides a board level summary ESR on each TSIU4 circuit pack. Each bit in the ESR is assigned to a component on the circuit pack and is used to report errors detected by that component. There also is a board level summary EMR.
14. Provides software with the ability to control and monitor the execution of the device's built in self test (BIST) for each custom device being designed for the TSIU4.

    The BIST is controlled through a register that has protected access. On completion of BIST, a bit is set in a register that is software readable.
15. Provides each TSIU4 circuit pack with the ability to store information that is specific to that circuit pack using a non-volatile device. The TSIU4 provides software with the ability to read the contents of the device, but it cannot write to the device.

16. Provides on each TSIU4 circuit pack a non-volatile register, containing at least three bits, that are used to store the version number of the circuit pack. The initial version number is zero, and is incremented whenever a modification impacting software is made to the circuit pack after its initial deployment.

2. BLOCK DIAGRAM OVERVIEW

The TSIU4 is a growable architecture and is divided into the following circuit packs to provision that growth:

UM74 - TSICOM The TSICOM is responsible for overall unit timing and the generation of the TSI Control (TSICNTL) Bus.

KLU1 - TSIS The TSIS circuit pack is one of the growable elements of the TSIU4. Each TSIS is responsible for: terminating four duplex TSI links (768 time slot each, for a total of 3072 time slots) on its four TSI ports, performing the signal processing function on these four links, participating in the distribution of all of the time slots that terminate on the SM-2000 to all of the TSISs, and selecting the time slots to be sent out over its four duplex TSI links. A fully equipped TSIU4 service group can contain 10 TSIS circuit packs.

UM73 - DXThe DX is the circuit pack that terminates PIDBs and, by subsampling the signaling bits, converts the data from 24 PIDBs into a TSI link. A fully equipped TSIU4 service group can contain six DX circuit packs.

For detailed information on the TSICOM, TSIS, and DX see the appropriate circuit description.

The following components of the SM-2000 switching network terminate and generatenew optical and electrical links based on the TSI link and are described further in their circuit description documents.

NLI The paddle board that terminates one NCT2 link, which carries 512 whole time slots, and one duplex TSI link (a simplex TSI link from each TSIU4 service group) and converts the data from one format to the other.

The interconnections between these circuit packs are shown in Figure 1.

2.1 TSI ARCHITECTURES

The TSIU4 is a large growable switching network that is non-blocking and fully interconnected. It is a one-sided TSI, as shown in Figure 2. Note that while the various peripheral, network, and local digital service function (LDSF) interfaces are shown, the TSI does not treat them differently. All connections to the TSI are through TSI links so anything to be connected to the TSI must support that interface. The TSI is divided into pieces, known as slices. Each slice is responsible for accepting incoming time slot data and generating the output time slot data for the links that are connected to it. Any time slot that arrives on a TSI link can be transmitted during any time slot on any link on any slice. Each slice stores in its data RAMs the time slots that arrive from all of the links on all of the slices . The arriving time slots are stored on each slice in the same location in its respective data RAMs. The slice control RAM circuitry reads the appropriate locations in its data RAMs to generate the time slot data for its output links. Most of the time slots that get stored in the slice's data RAMs will not be used, because the number of input time slots to the whole TSI is usually much greater than the number of output time slots on a single slice. This architecture allows a single input time slot to be transmitted on as many output time slots as desired, providing unlimited data fan-out since every slice contains all of the time slot data received on the TSI links.

2.2 TSIU4 OVERVIEW

The TSIU4 is being implemented using the one-sided TSI architecture described in the previous section. The TSIS circuit packs are responsible for performing the functions of a slice of the TSI.

A drawing of the SM-2000 frame layout, including the TSIU4 unit (the top two shelves), is shown in Figure 3. The TSIU4 will be a two shelf duplex unit that contains a cross-coupled connection of clock and synchronization signals to ensure that the two service groups are in synchronization. The unit is divided into left and right service groups, with service group 0 on the left side when facing the front of the unit. The top shelf will contain 8" high circuit packs. The bottom shelf will be 16" high in order to increase the

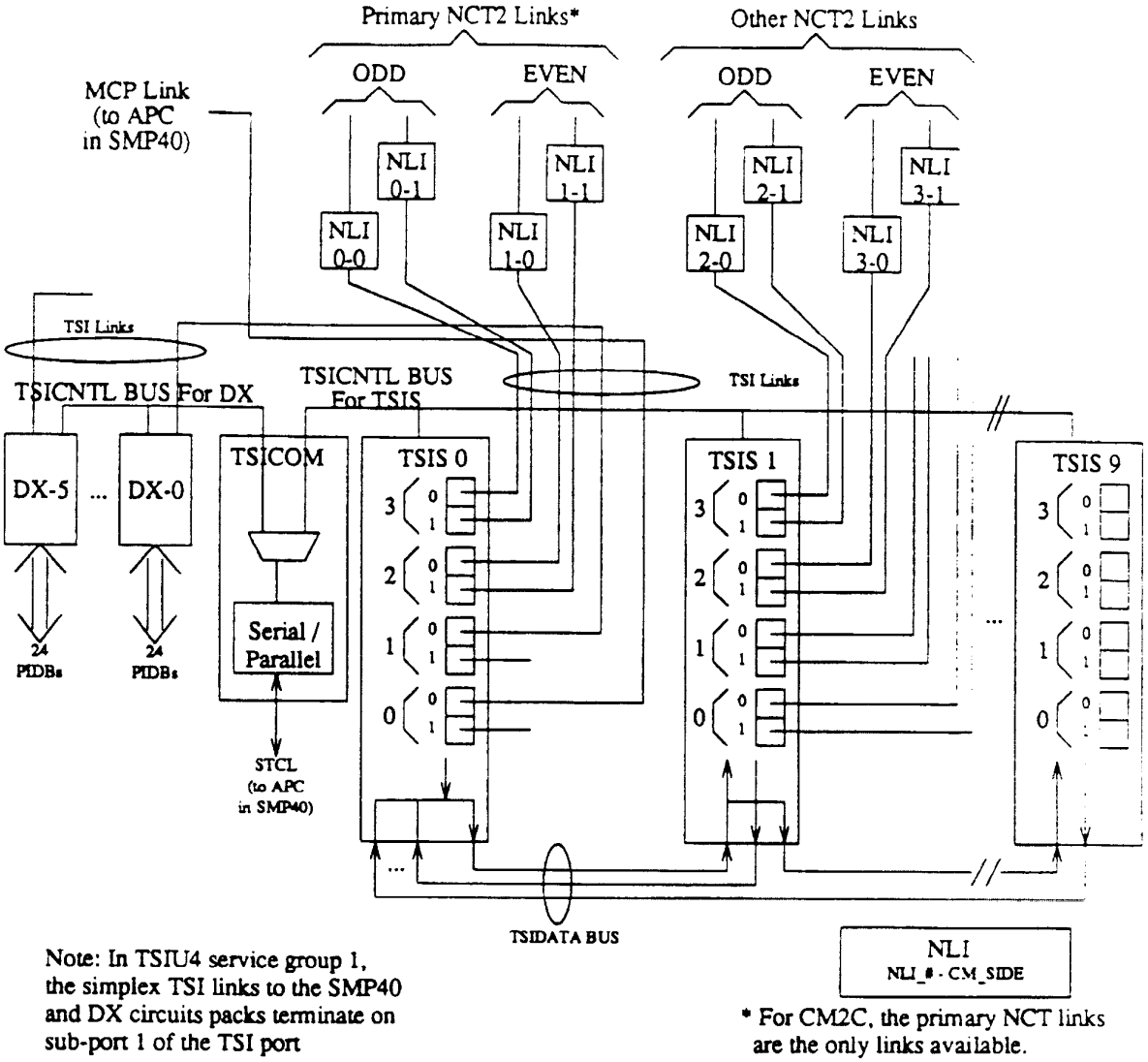


Figure 1. SM-2000 Switching Network

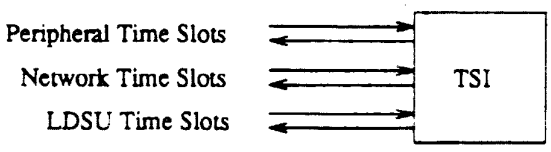


Figure 2. A One-Sided TSI

number of I/O leads available on each TSI slice. Both shelves are 10" deep (the normal unit depth is 13"). Each service group is in the same failure group as one of the SMPU4 shelves.

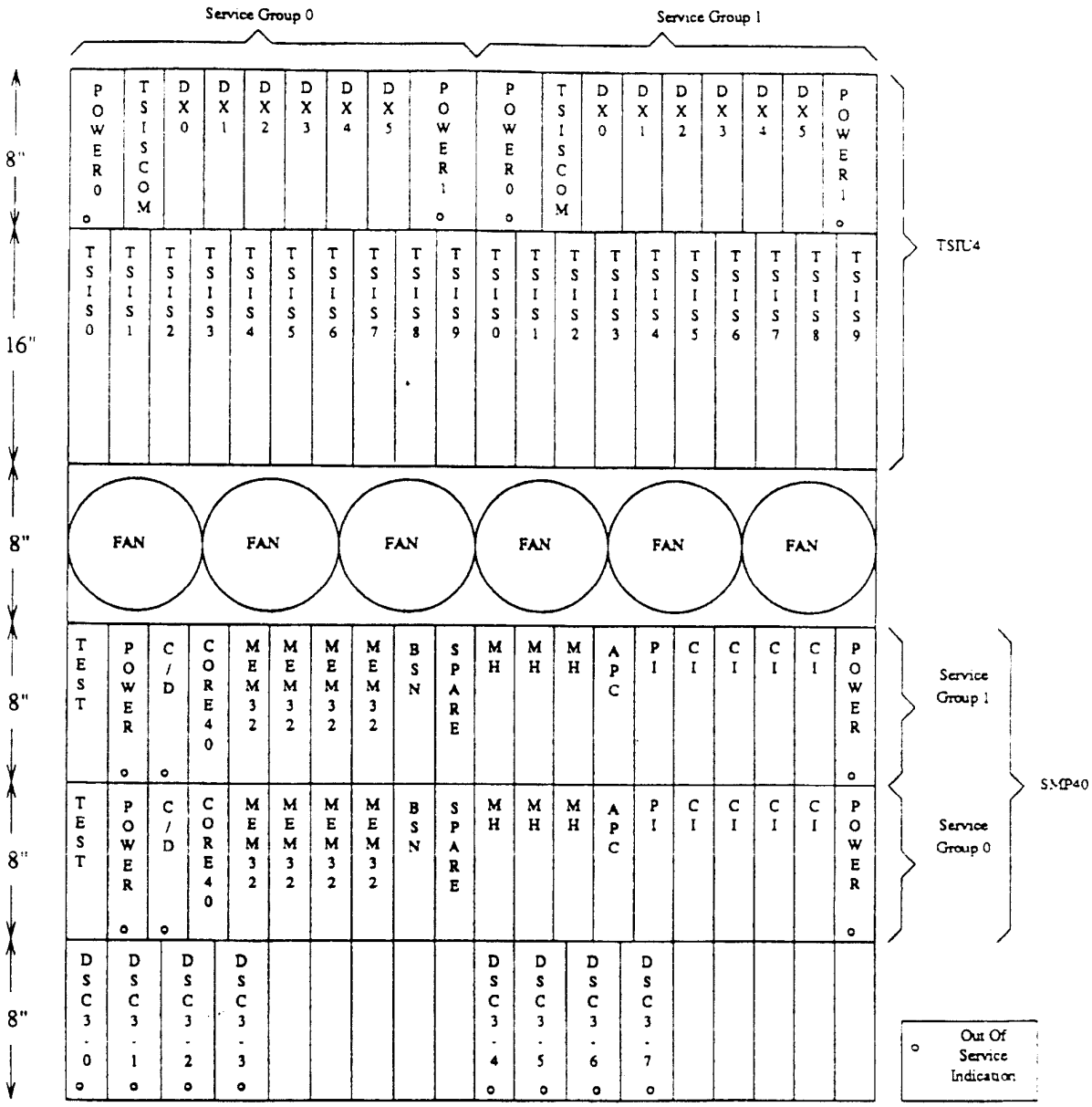


Figure 3. SM-2000 Frame Layout

The TSIU4 triple high backplane measures approximately 23" by 25". It is manufactured "impedance controlled" in order to maintain 100 ohm +/-10% impedance for the numerous high speed connections which use differential balanced pairs. The cross-coupled TSI links of the two TSIU4 service groups is designed in this manner as well as the system clock distribution. Since most of the printed wire runs horizontally across the backplane each signal layer of this 20 layer backplane is sandwiched between power and ground planes to prevent crosstalk between adjacent signal layers.

The power converter on the left hand side of each service group (PWRCNVTR 0) is always equipped, while the one on the right side of each service group (PWRCNVTR 1) is only equipped when the number of TSISs in the shelf is greater than 3 or the number of DXs in the shelf is equal to 6. The second power converter is installed at the same time that TSIS3 and/or DX5 is grown. Due to the TSIU4's data distribution architecture, TSIS circuit packs must be grown in numerical order (from left to right on the shelf). No empty slots are allowed in the middle of the group of TSIS circuit packs. A rear view of the TSIU4 unit is shown in Figures 4a-d.

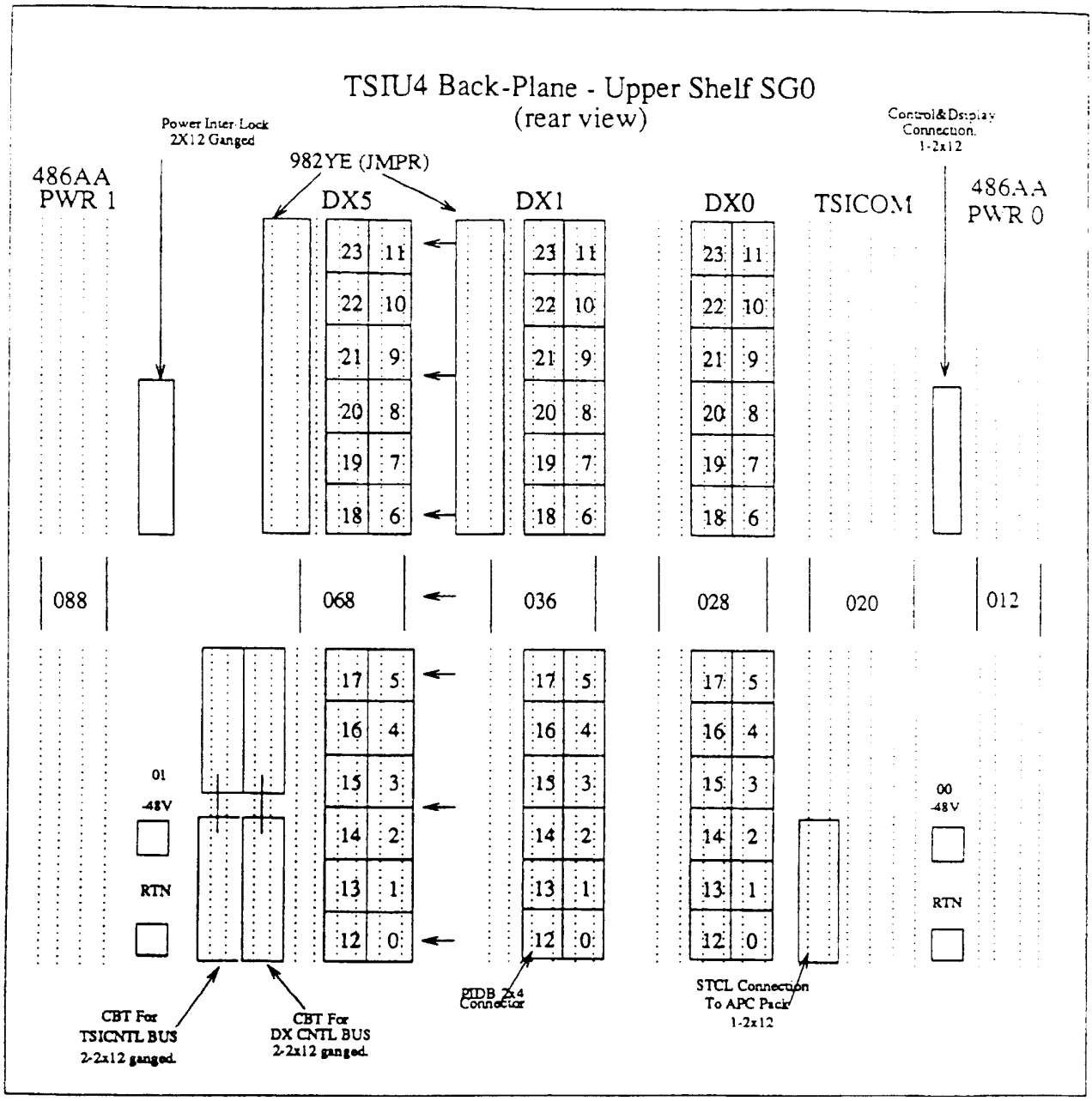


Figure 4a. Rear View Of TSIU4 Unit Upper Shelf- SG0

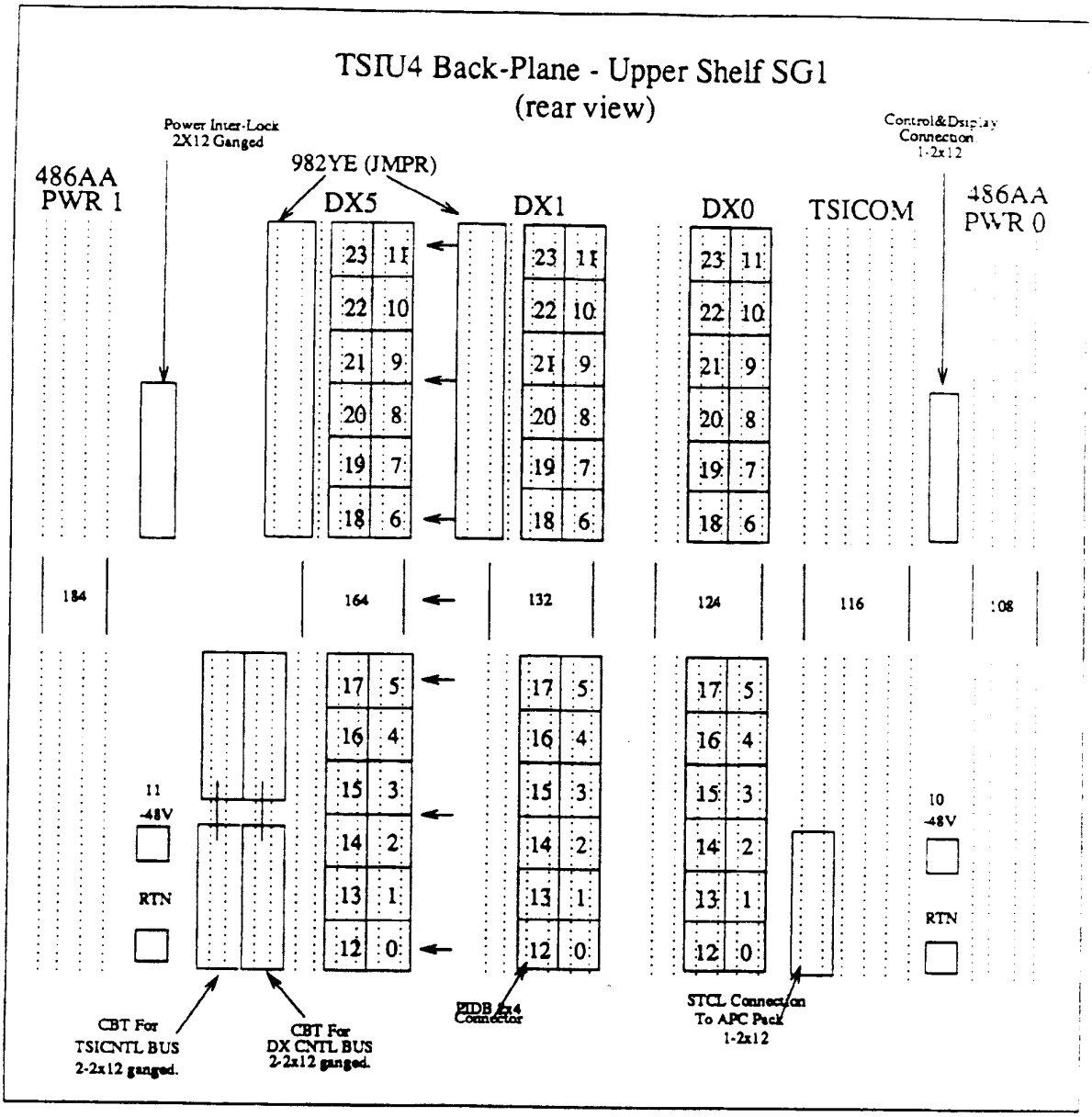


Figure 4b. Rear View Of TSIU4 Unit Upper Shelf- SG1

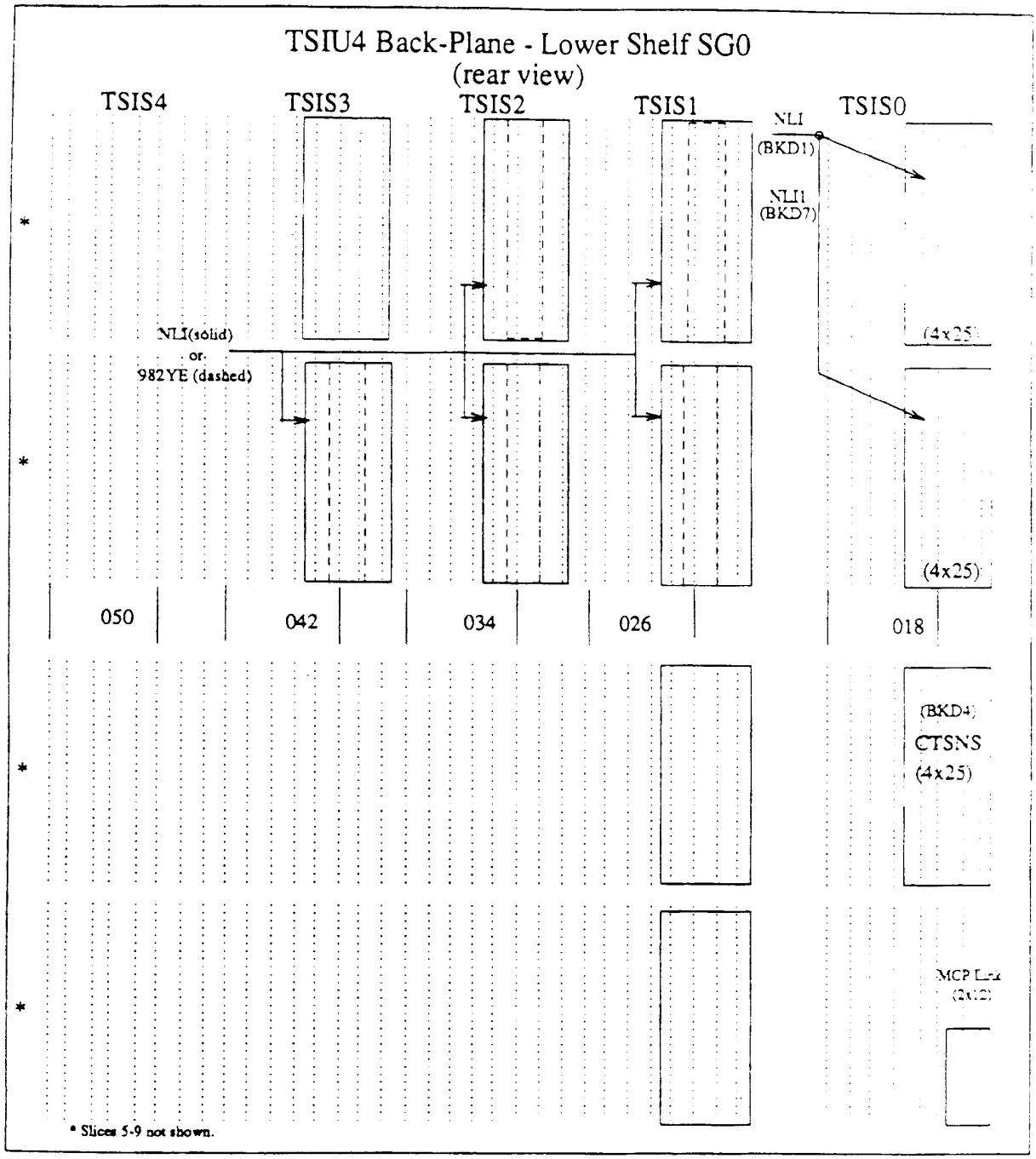


Figure 4c. Rear View Of TSIU4 Unit Lower Shelf- SG0

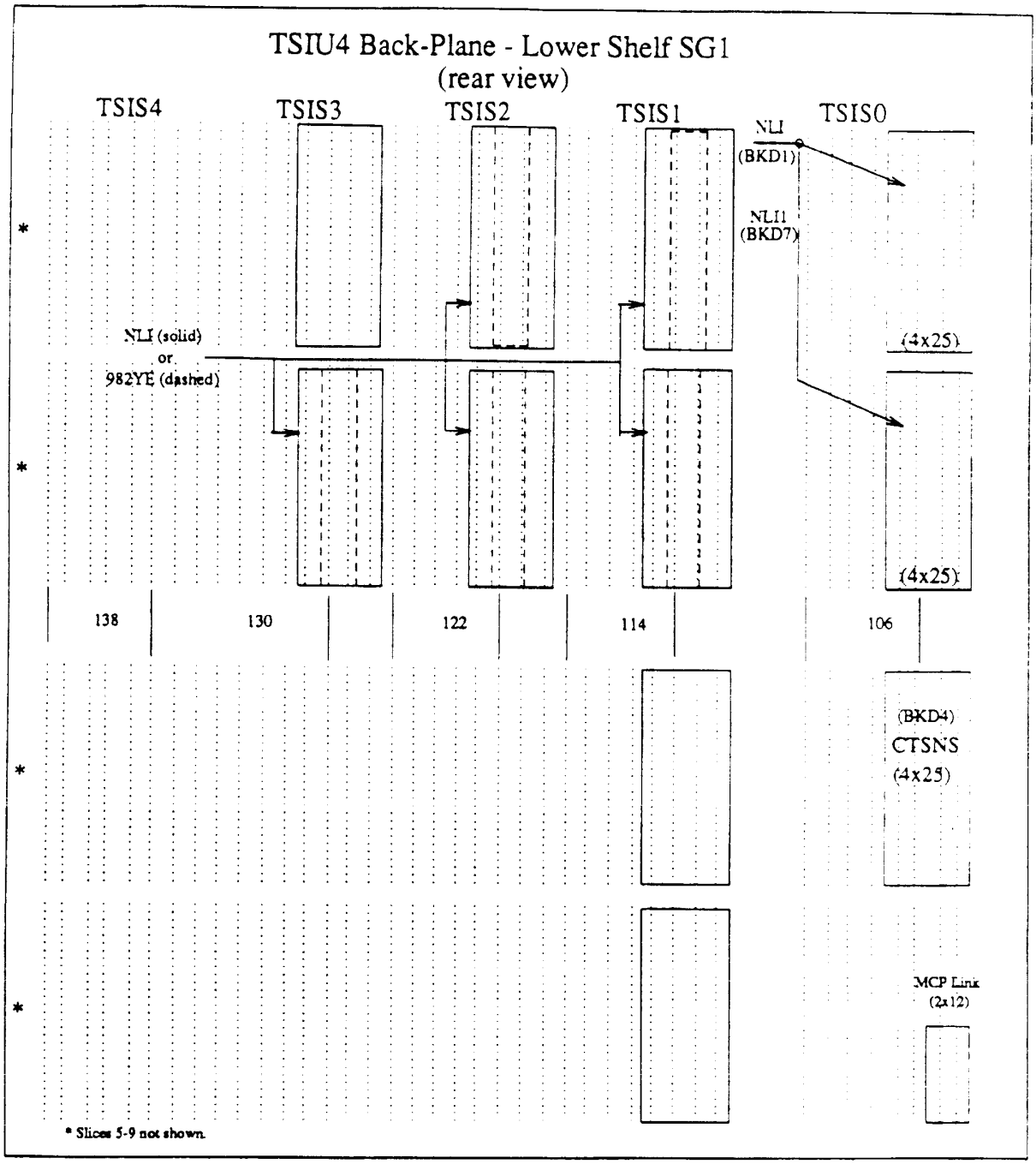


Figure 4d. Rear View Of TSIU4 Unit Lower Shelf- SG1

For Release 1, a minimally equipped operational TSIU4 service group will contain:

1. One power converter
2. The TSICOM
3. One TSIS
4. One DX
5. Two control bus terminator (CBT) paddle boards
6. One control time slot number select (CTSNS) paddle board
7. One power interlock board (PIB) paddle board
8. Two NLI paddle boards

This equipage would provide 1024 network time slots and 768 peripheral time slots. At least 256 peripheral time slots would be used for the LDSF. Note that the DX circuit pack and the CTSNS paddle boards are not required for the SM to be operational. In the system lab environment, there may be SM-2000's which do not have these.

Figure 5, the SM-2000 functional block diagram, does not show the detail of the data flowing from the TSISs to the first TSIS prior to storage in the data RAM.

The S1 and S2 switches shown in Figure 5 are implemented for diagnostic purposes. The S1 switch is in the NLIT device on the *LI paddleboard; the S2 switch is in the DXC device on the DX circuit pack. They are not intended to be used by operational software. The S1 switch is a link based switch, rather than a per time slot switch (it loops the entire TSI link not just a single time slot). The S2 switch can be configured as either a single time slot loop switch, or a whole PIDB loop switch. When the S2 switch is used to loop all time slots, it will introduce skew between the output time slot number and the input time slot number.

For SM-2000 release 1, peripheral time slots will arrive at the TSIU4 through PIDBs and terminate on the DX circuit pack. The DX circuit pack terminates 24 PIDBs (768 time slots) and converts them to the TSI link format. As a part of this conversion, the signaling bits are subsampled. The TSI link format carries the signaling bits from each time slot every fourth frame, creating a four frame (500 µs) superframe (also known as the PCT link format), as shown in Figure 6.

Table 1 identifies the usage that has been assigned to the overhead bytes on the TSI links as they terminate on the TSIS. The "Rcv Dir" columns refer to what the TSIS circuit pack will receive. The "Xmit Dir" columns refer to what the TSIS circuit pack will transmit.

The board ID byte is used to uniquely identify the equipment that can terminate the other end of the TSI link. The mapping between this equipment and board ID values is shown in Table 2.

The mapping between PIDB time slots and TSI link time slots is shown in Figure 7.

For local or host SM-2000s, network time slots arrive at the TSIU4 through TSI links from duplex NLIs. Each of these TSI links will contain 512 time slots, thus 256 time slots of the 768 time slots on the TSI link will not be used. The mapping between the time slot numbers on the NCT2 link and the TSI link time slot numbers is shown in Figure 8.

Regardless of the source of the time slots, they first terminate on a TSIS circuit pack. Each of these circuit packs can terminate four duplex TSI links. The AUTISS function selects which of the duplex NLI's NCT time slot data to accept on a time slot basis. Since the connections between the TSIS and the DXs, and those between the TSIS and the APC are simplex, no side selection is performed.

After the side selection operation occurs, the data flows to one of the signal processing devices on the circuit pack and to the first TSIS. TSIS0 accepts data from all of the TSISs that are equipped and begins the processes of sending the data to all of the other TSISs. It does this by transmitting all time slots to the

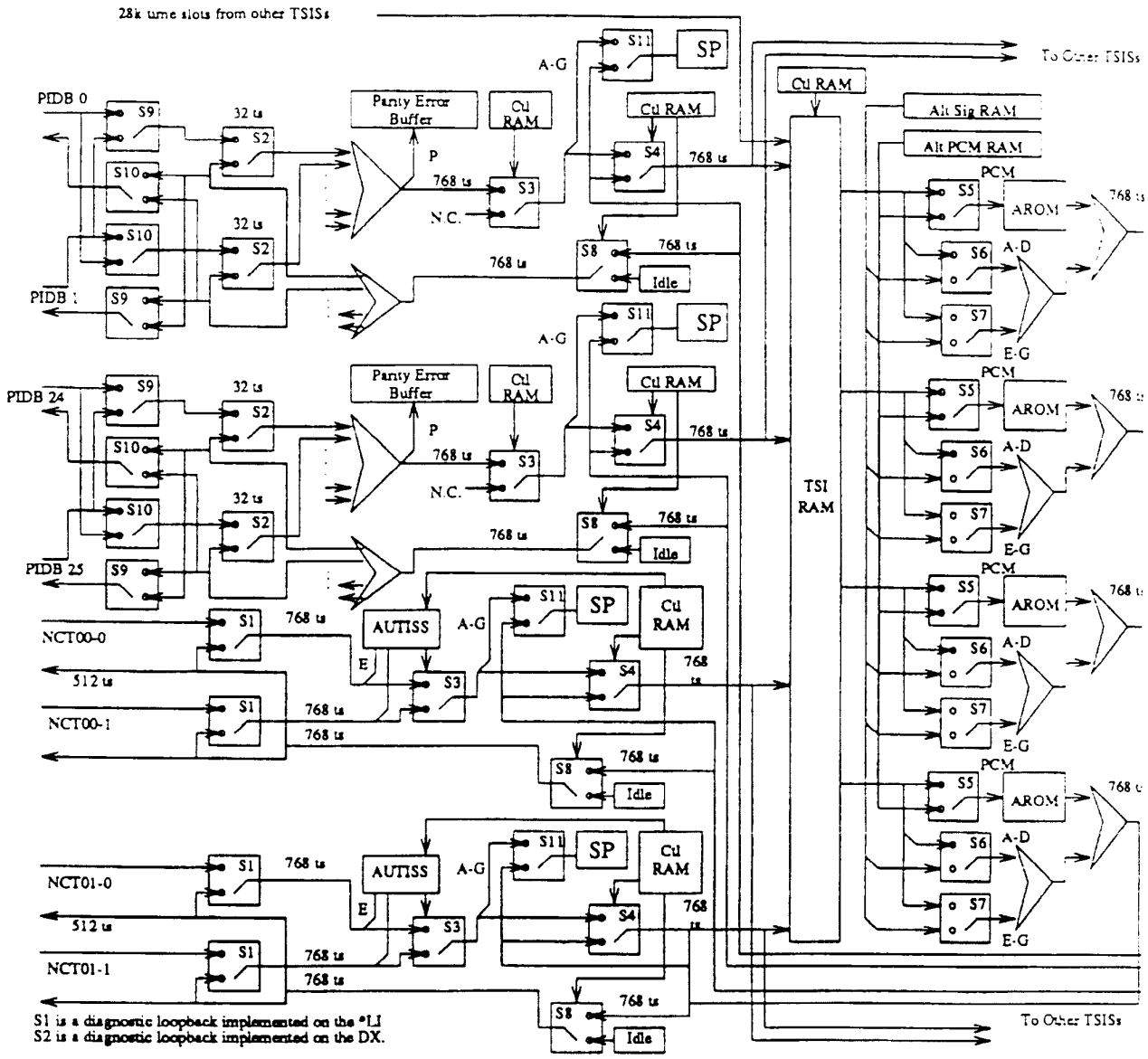


Figure 5. SM-2000 Switching Network Functional Diagram

second TSIS. The second TSIS is responsible for both storing the data in its data RAMs, and passing it to the third TSIS. The third TSIS stores the data and passes it to the fourth, and so on for all TSISs that are equipped. The data on this bus is buffered using elastic stores to compensate for skew between adjacent TSIS's system clocks.

Each TSIS is responsible for using the information that has been stored in its control RAMs to select the time slots that are to be sent out over the four TSI links that terminate on it. The same data is sent out over duplex TSI links, the only exception being the CTSs.

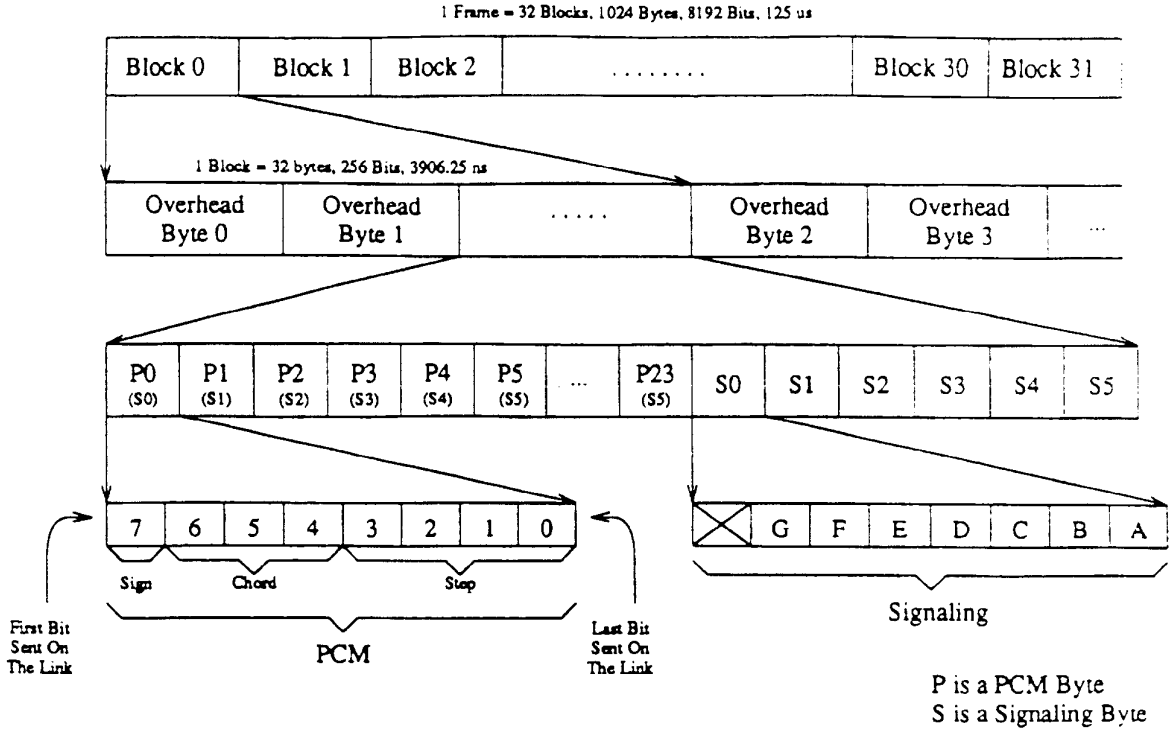


Figure 6. TSI Link Format

2.3 TSICOM DESCRIPTION

The TSICOM block diagram is shown in Figure 9. The major functions of the TSICOM circuit pack are:

1. Unit timing synchronization (a Stratum 4 clock)
2. STCL termination
3. TSICNTL bus generation
4. Collection of interrupts from the TSIU4 circuit packs
5. Collection of SP service requests from the TSIS circuit packs
6. Generation of the TSIU4 unit interrupt

2.4 TSIS DESCRIPTION

A block diagram of the TSIS architecture is shown in Figure 10

The major components that will be used to implement the TSIS functions are:

IF Device: The interface (IF) device serves as the data interface for the duplex TSI links that terminate on the TSIS. A single IF device will handle both the transmit and receive directions of a single duplex link (one TSI port). Since each TSIS has four TSI ports, four IF devices will be required on each of these circuit packs. The IF device will perform the AUTISS function and peripheral side select switch (S3) and will contain the loopback switch (S4) and idle code insertion switch (S8). The per time slot control information required for these switches will be contained in a control RAM internal to each IF device.

TABLE 1. TSI Link Overhead Byte Assignment

Overhead Byte Number	Function	NLI Rcv Dir	NLI Xmit Dir	DX Rcv Dir	DX Xmit Dir	APC Rcv Dir	APC Xmit Dir
0/1	Framing	No	No	No	No	No	No
2	Super Framing Byte	No	No	No	No	No	No
3	CRC Byte	Yes	Yes	Yes	Yes	Yes	Yes
4/5	Link Control Register	Yes	Yes	No	No	No	No
6/7	Link ESR	Yes	Yes	No	No	No	No
8/9	Link EMR	Yes	Yes	No	No	No	No
10/11	Link Check Error Control	Yes	Yes	No	No	No	No
12/13	Link BIST Control Register	Yes	Yes	No	No	No	No
14/15	Link Signature Analysis Register	Yes	Yes	No	No	No	No
16/17	Link Loop Word	Yes	Yes	No	No	No	No
18/19	Peripheral Loop Word	No	No	No	No	No	No
20/21	Peripheral Control Register	No	No	No	No	No	No
22/23	Peripheral ESR	No	No	No	No	No	No
24/25	Peripheral Address Out Register	No	No	No	No	No	No
26/27	Peripheral Data0 Out Register	No	No	No	No	No	No
28/29	Peripheral Address In Register	No	No	No	No	No	No
30/31	Peripheral Data0 In Register	No	No	No	No	No	No
32/33	Peripheral EMR	No	No	No	No	No	No
34/35	Peripheral Data1 Out Register	No	No	No	No	No	No
36/37	Peripheral Data1 In Register	No	No	No	No	No	No
38 - 62	Not Assigned	—	—	—	—	—	—
63	Board ID	Yes	No	Yes	No	Yes	No

TABLE 2. Board ID Byte Assignment

Item	Board ID Value
APC	0x01
DX	0x02
NLI	0x03
NLI1	0x15

CRAM device: The control RAM (CRAM) device generates the per time slot address and control signals for the static RAM (SRAM) devices (the TSIU4's data RAMs) and the AROMs. Two CRAM devices are used on the TSIS circuit pack. CRAM 0 generates addresses and control for time slots to be transmitted on TSI links 0 and 1. CRAM 1 generates addresses and control for time slots to be transmitted on TSI links 2 and 3. The CRAM devices also store the alternate PCM and signaling bit values, and contain the control RAM for switches S5, S6, and S7.

SRAM device: The SRAM device is used to store the PCM and sub-sampled signaling bits. All of the time slots that enter the SM-2000 on all of its TSI links are stored in the SRAMs on each TSIS. A single SRAM will be capable of storing the data from four TSI links. Since there are a maximum of 40 TSI links that can be terminated on an SM-2000, each TSIS will require 10 SRAM devices. The SRAM also contains the switches (S5, S6, and S7) that are used to perform the alternate PCM and/or signaling bit insertion.

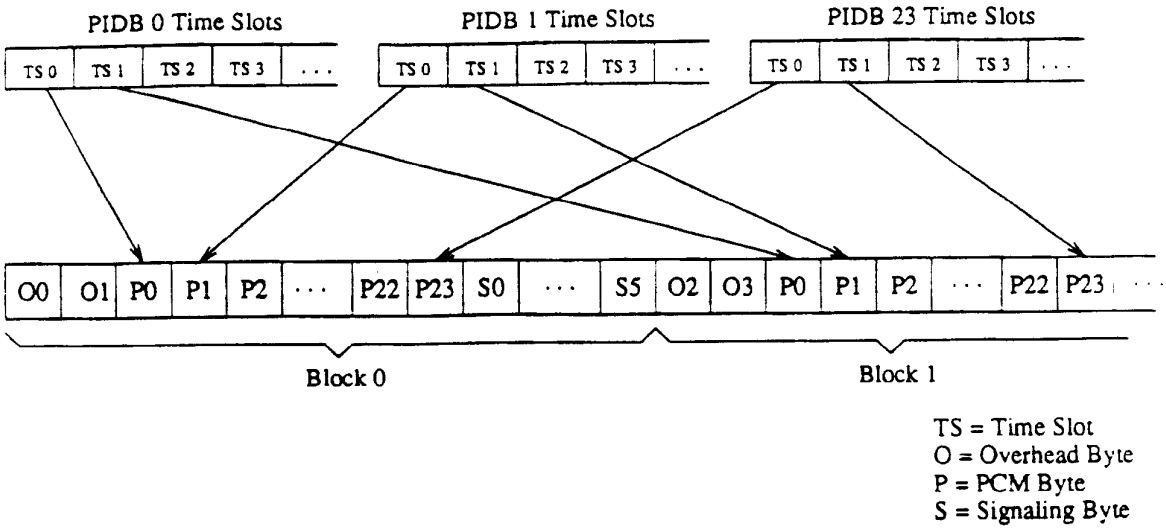


Figure 7. Mapping of PIDB Time Slots to TSI Link Time Slots

SP device: The SP device filters state changes on the signaling bits received on the four TSI links and reports valid changes through the use of an internal FIFO. Two SP devices are used on the TSIS circuit pack. SP 0 operates on the signaling bits for time slots received on TSI links 0 and 1. SP 1 operates on the signaling bits for time slots received on TSI links 2 and 3. The SP devices also collect error reports from all of the other circuitry on the TSIS circuit pack and generate the circuit pack error signal.

AROM Device: As is done in TSIU3, an AROM device will be used to provide the ability to perform attenuation, amplification, and companding conversion. Due to the slow speed of these devices, each TSIS will each have four AROM devices. Each device will be dedicated to one outgoing TSI link. The control signals for the AROM are provided by the CRAMs; each CRAM will control two AROMs.

Boundary scan master device: The boundary scan master (BSM) device is used to control the execution of the circuit pack's BISTs. In the system environment it will provide the diagnostic software with an alternative means to invoke each of the custom device's BISTs. In the manufacturing environment, it will be the primary means of controlling and observing the hardware tests of the circuit pack. Each TSIS circuit pack will contain an electronically programmable read-only memory (EPROM) device that diagnostic software will use to obtain the data necessary for that version of the board to execute the BSM directed circuit pack tests.

The operational data, control, and clock flows between these components on the TSIS are shown in Figures 11, 12 and 13 respectively. It should be noted that there are additional interconnections that are only used for diagnostics (board and unit BIST), which are not shown in Figures 11 and 12.

2.4.1 CTS AND CPI INTERFACE

The first TSIS will provide a mechanism that does not require software control to extract the four CTSs, including the CPI bit, from the four TSI links that carry the time slots arriving on the four primary NCT2 links (two from CM side 0 and two from CM side 1) and will insert them into the MCP link. TSIS0 will also provide a mechanism that does not require software control to extract the four CTSs, including the CPI bit, from the MCP link and insert them onto the four TSI links (one to each TSI link) that carry the time

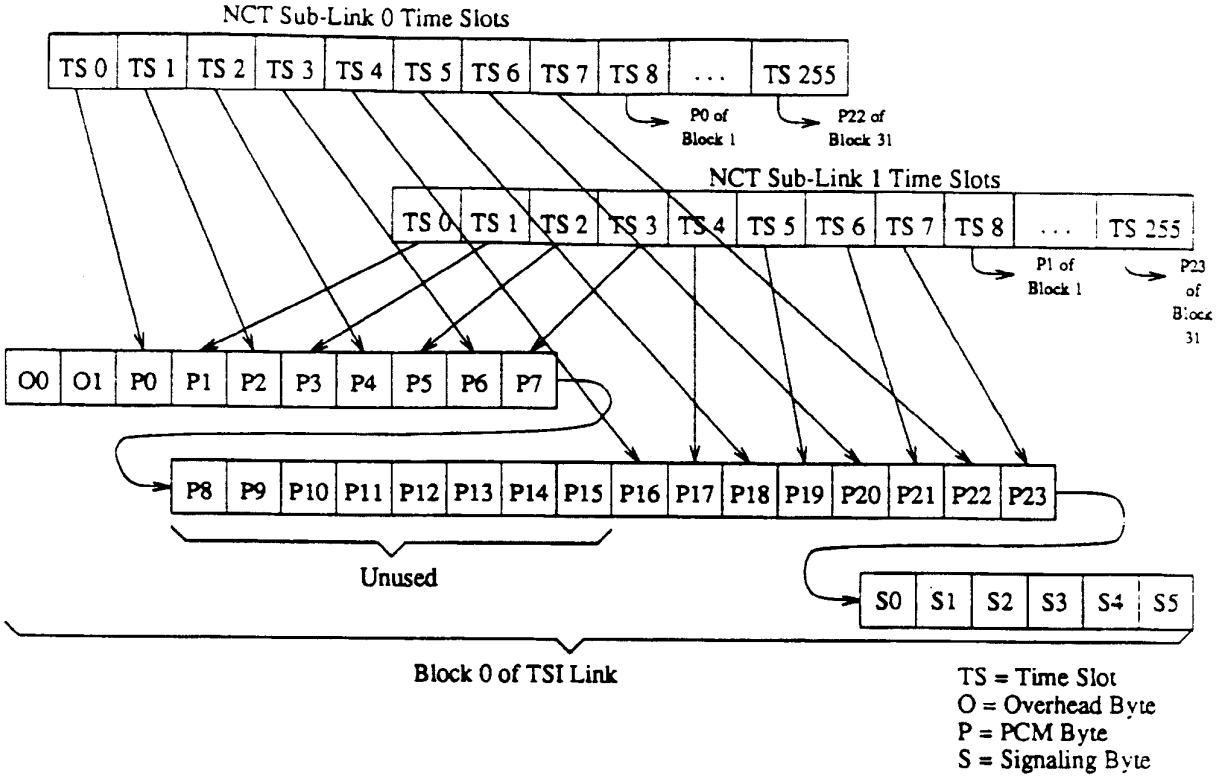


Figure 8. Mapping of NCT2 Time Slots to TSI Link Time Slots

slots departing on the four primary NCT2 links. Prior to inserting the CTSs into the MCP link or a TSI link, the ordering of the CTS's PCM bits will be reversed. All of these links will terminate on TSIS0's TSI ports, according to the mapping shown in Table 3. Table 4 shows which MCP time slots will be used to transport the CTSs.

2.5 DX DESCRIPTION

The DX provides the interface between the TSIU4 and the PIDBs. Figure 14 contains a block diagram of the DX circuit pack. Each DX contains one DX device (DXC) which converts a TSI link to 24 PIDBs. The DX is responsible for:

1. Converting the time slots from the TSI link format to the PIDB format. This includes converting the sub-sampled signaling bits of the TSI link format to the whole time slot PIDB format.
2. Providing a 2:1 data fan-in switch, controllable on a per time slot basis, for each pair of adjacent PIDBs.
3. Providing a 2:1 data fan-out switch, controllable on a per time slot basis, for each pair of adjacent PIDBs.
4. Generating and checking the cyclic redundancy check (CRC) on the TSI link frames.
5. Generating and checking parity on the PIDB time slots using a walking parity scheme.

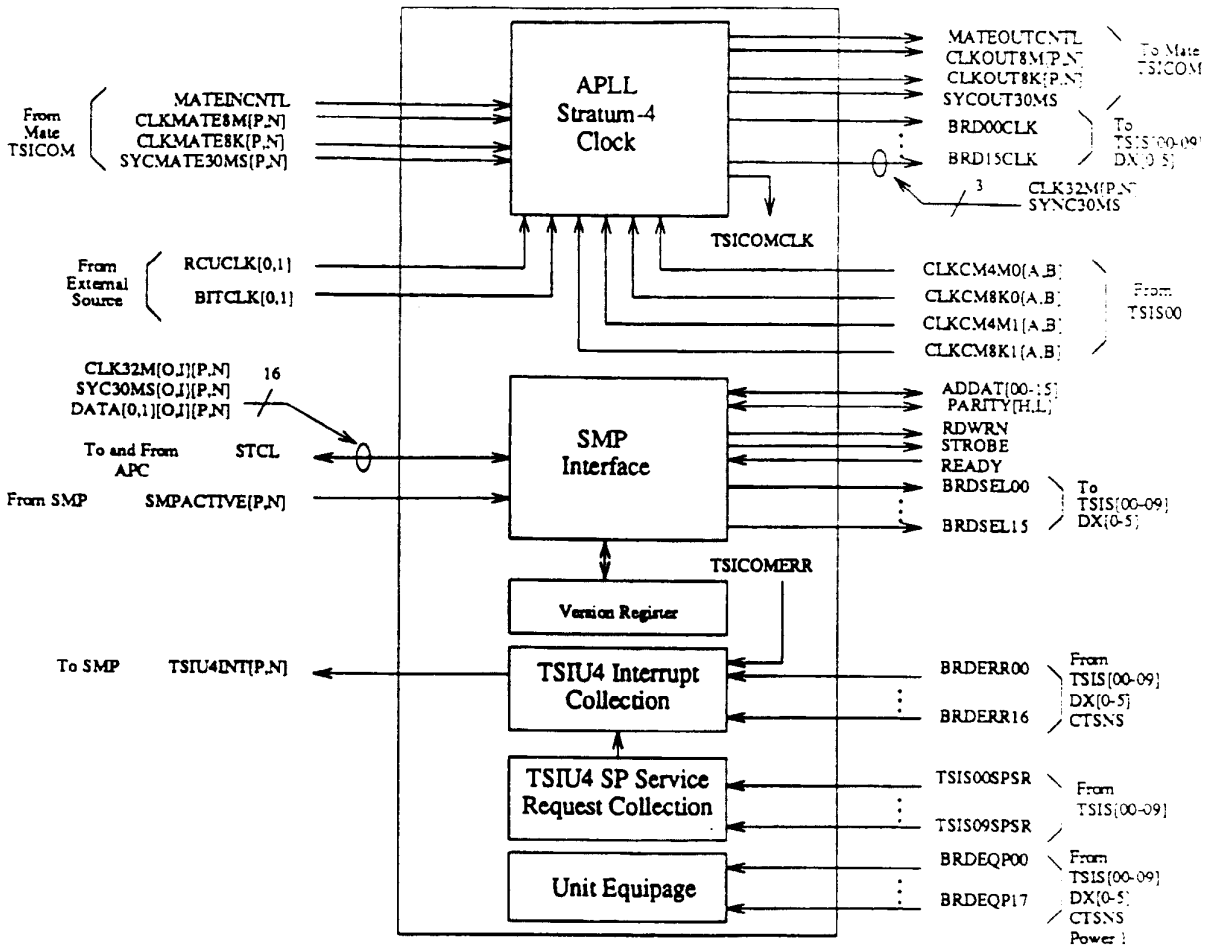


Figure 9. TSICOM Circuit Pack Block Diagram

Each DX contains one DXC chip, an inventory PROM readable over the TSICNTL bus, the PIDB buffers, and a power-up reset circuit.

The interconnection of the TSIU4 with a duplex peripheral is shown in Figure 15.

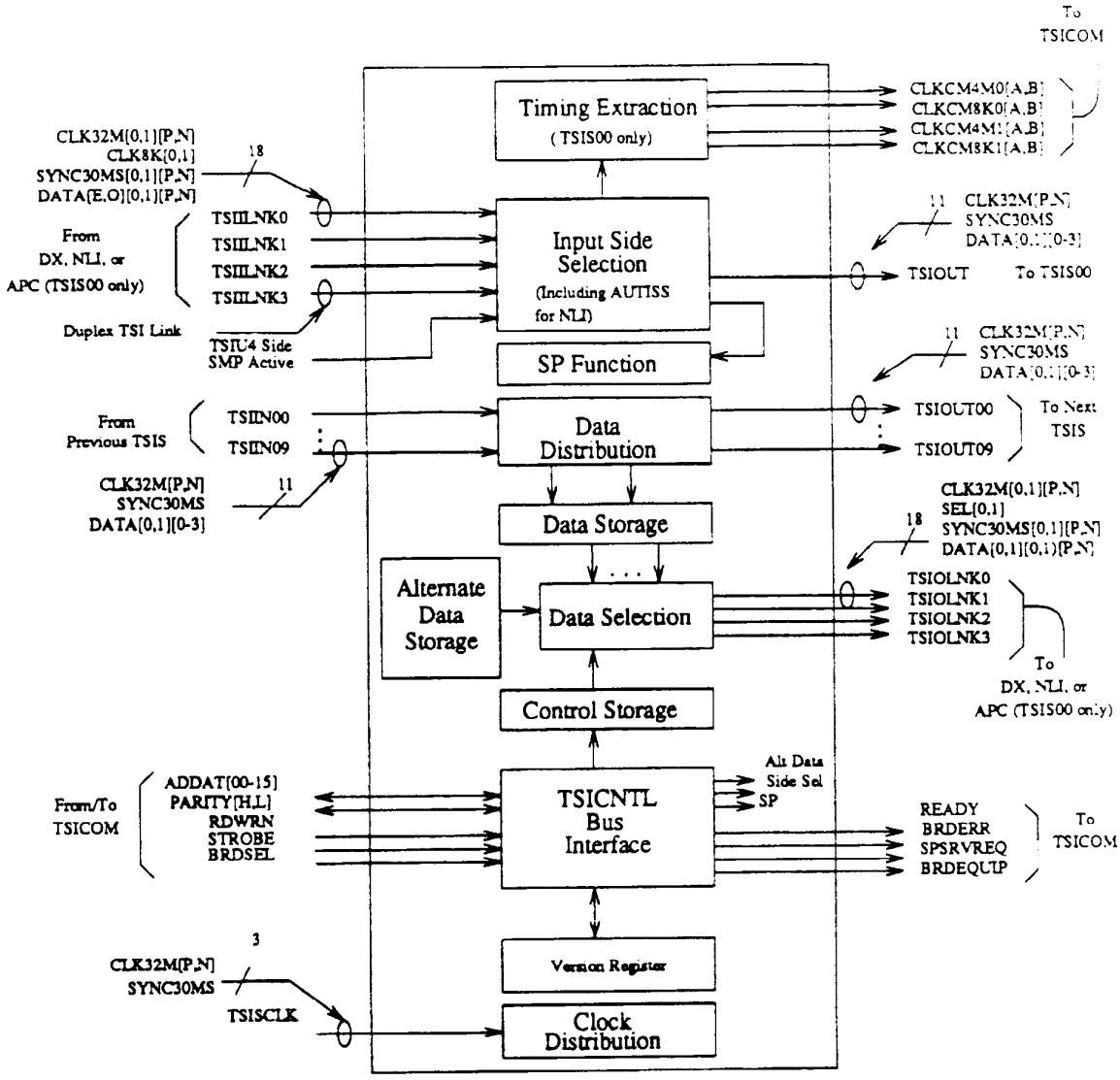


Figure 10. TSIS Circuit Pack Block Diagram

3. TSIU4 UNIT

The layout of the TSIU4 unit is shown in the top two shelves in Figure 3. The unit is divided down the middle of the two shelves into two service groups. The left service group is service group 0 and the right service group is service group 1. Each service group is a member of the corresponding SMPU4 failure group.

The unit can be engineered and equipped to meet the needs of a particular switching module in terms of the number of network and peripheral time slots. Due to the TSIU4's data distribution architecture, it is required that TSIS circuit packs be grown in numerical order (from left to right in the shelf). There can be no empty slots in the middle of the group of TSIS circuit packs.

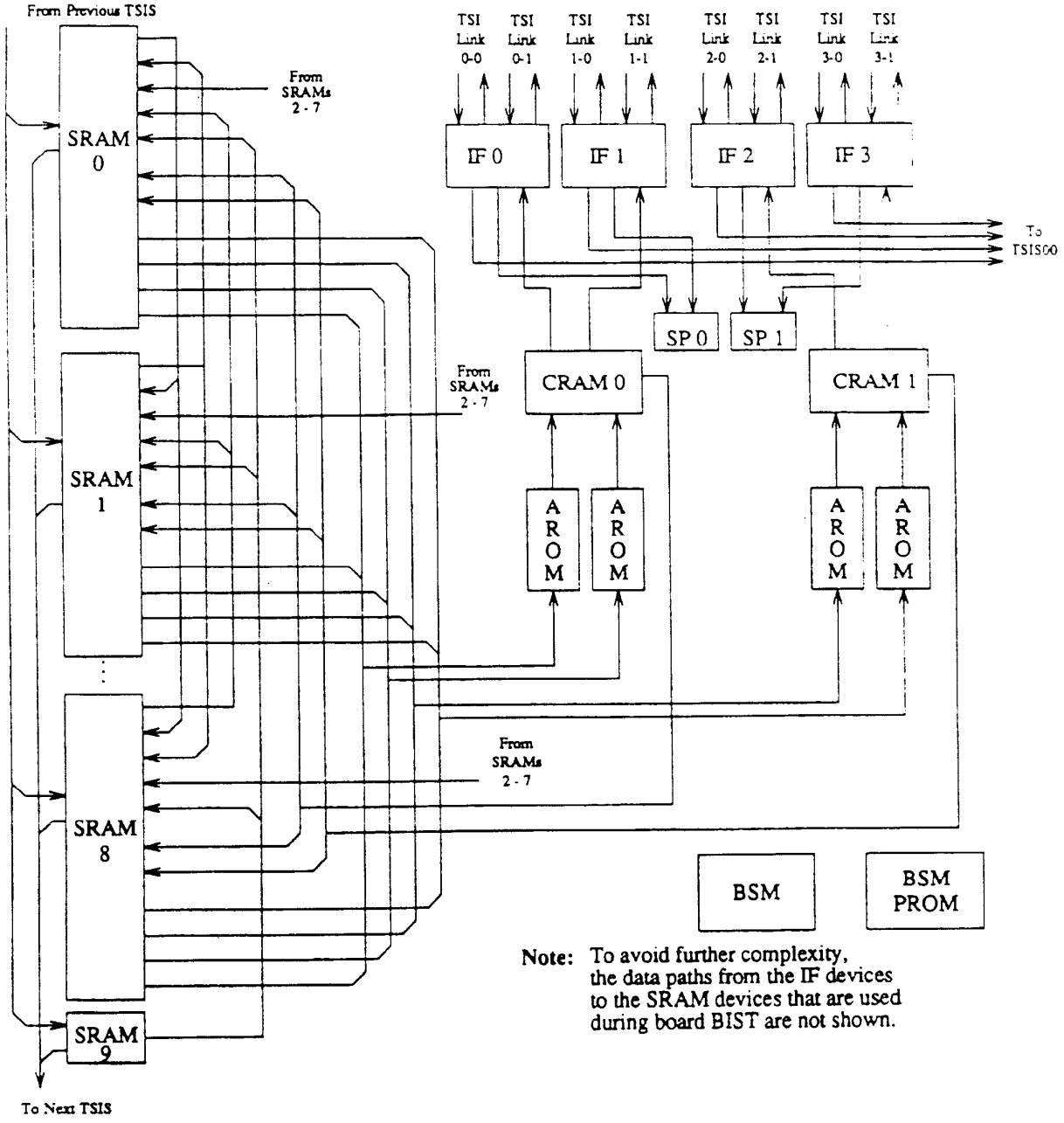


Figure 11. TSIS Data Flow

3.1 SOFTWARE INTERFACE

The interface between the SMPU4 and the TSIU4 will be over the STCL. The STCL interface provides a two Mbyte address spectrum for the TSIU4 which is divided among the TSIU4 circuit packs as shown in Table 5.

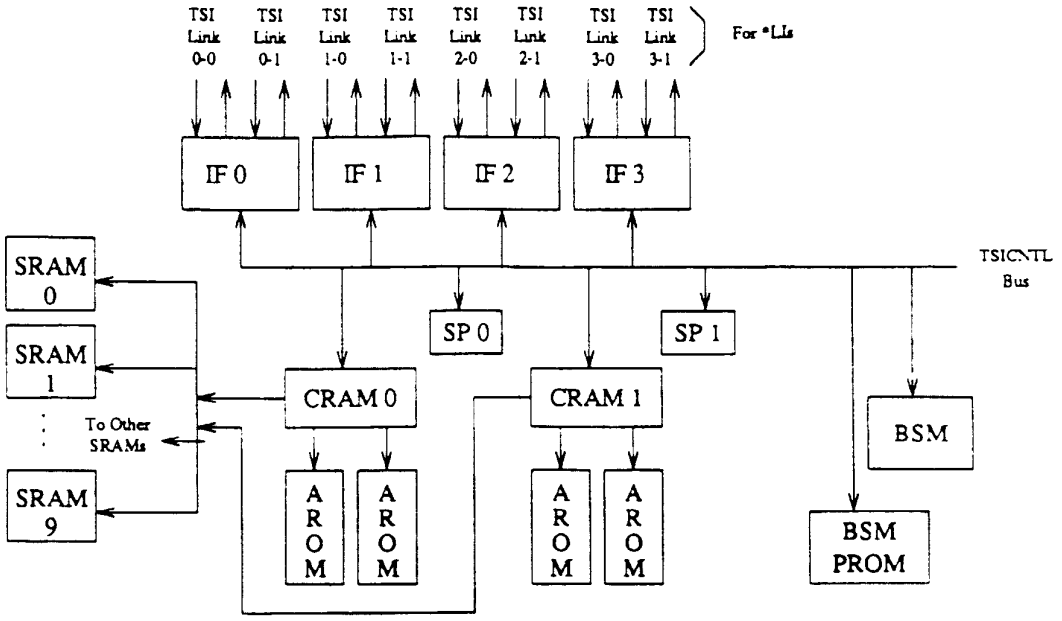
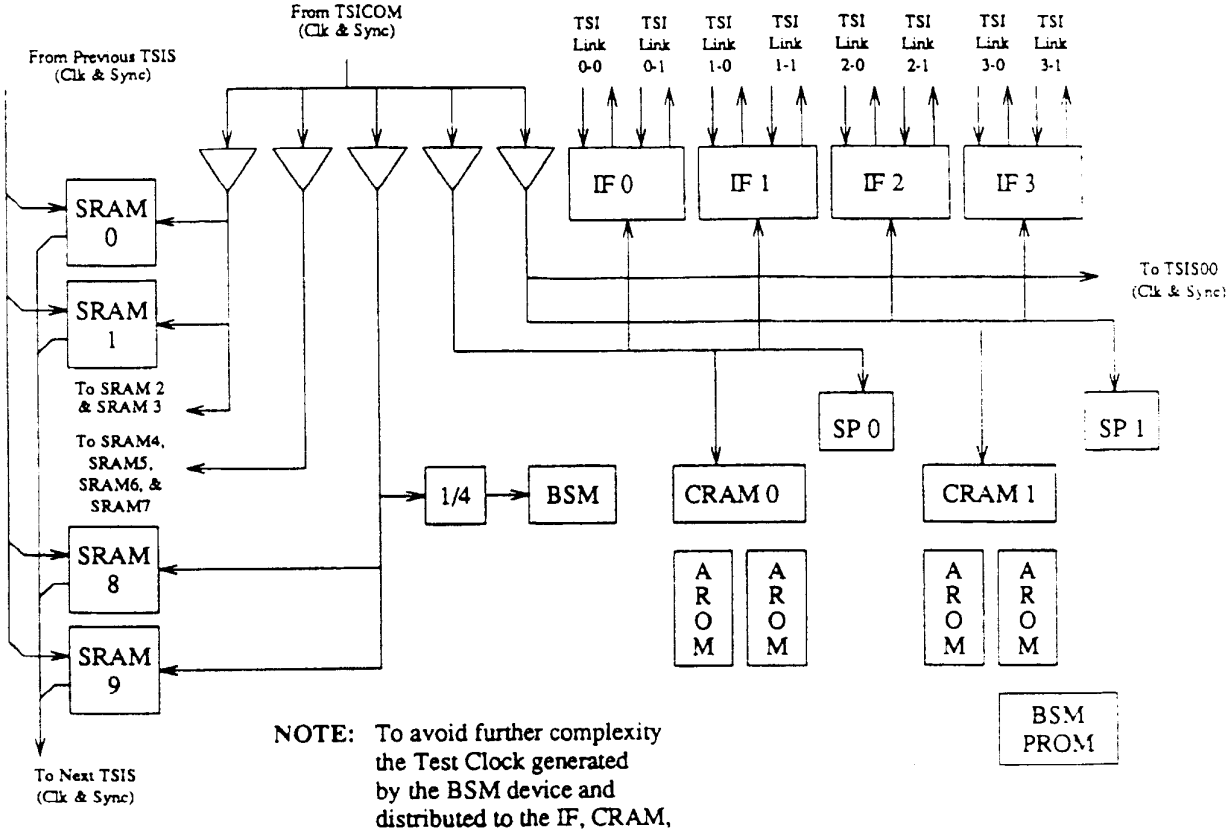


Figure 12. TSIS Control Flow

Both byte and longword addresses and sizes are shown in Table 5 (and similar tables which will follow); from the SMPU4 perspective addresses are byte based, while from the TSIU4 perspective, due to the definition of the STCL, all accesses are longwords (four bytes).

The interrupt structure for the unit is depicted in Figure 16

Table 6 provides a summary of the software controllable switches in the TSIU4.



NOTE: To avoid further complexity the Test Clock generated by the BSM device and distributed to the IF, CRAM, SRAM, and SP devices is not shown.

Figure 13. TSIS Clock Flow

TABLE 3. TSI Port Assignment on the TSIS0 Circuit Pack

Port Number	Used For	Source
0	MCP Link	APC
1	Peripheral Time Slots	DX 0
2	CM/CM2C Even Time Slots	NLI/NLI1
3	CM/CM2C Odd Time Slots	NLI/NLI1

4. MISCELLANEOUS CIRCUIT EQUIPMENT

4.1 POWER CONVERTER

The power converter on the left hand side of each service group (PWRCNVTR 0) is always equipped, while the one on the right side of each service group (PWRCNVTR 1) is only equipped when the number of TSISs in the shelf is greater than or equal to four; that is, the second power converter in each service group needs to be grown before or at the same time that TSIS3 is grown, or when the number of DX circuit packs is equal to 6, (when DX5 is grown).

TABLE 4. CTS Assignment on the MCP Link

CM Source	CTS Number	MCP Link Time Slot Number
CM0 even	0A	P0 in Block 0
CM0 odd	0B	P0 in Block 1
CM1 even	1A	P0 in Block 2
CM1 odd	1B	P0 in Block 3

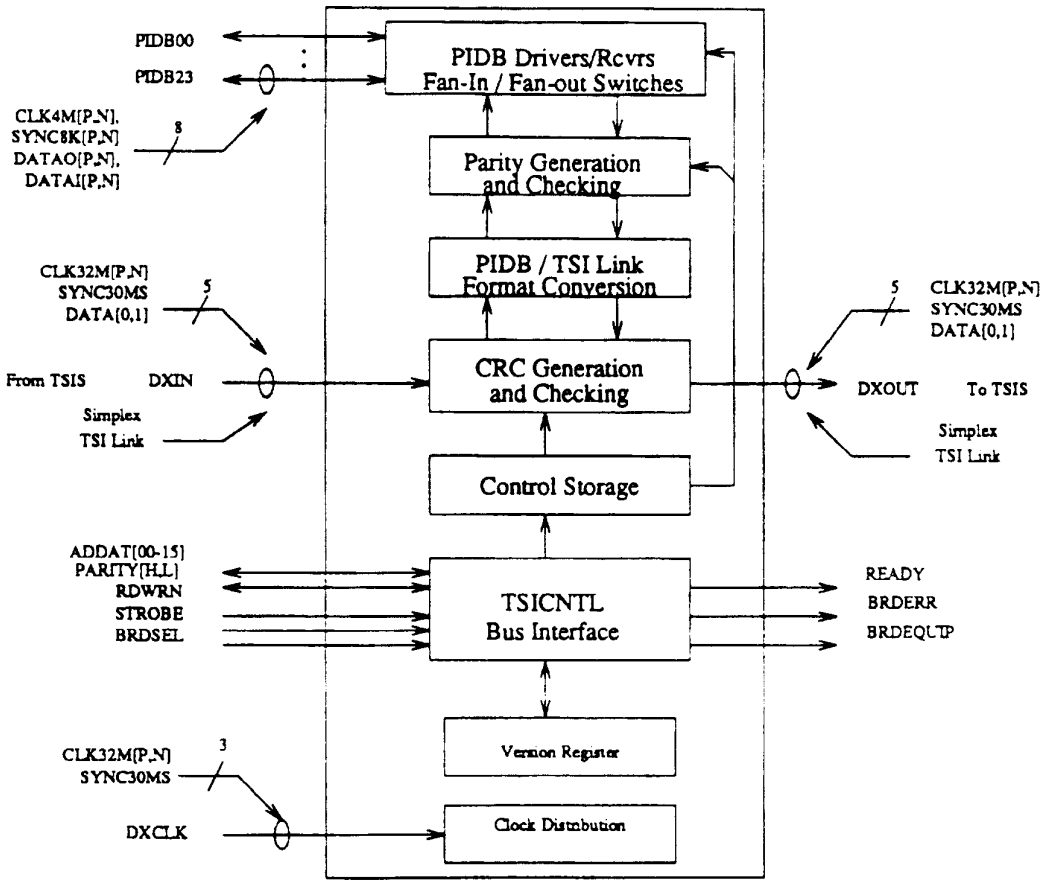


Figure 14. DX Circuit Pack Block Diagram

4.1.1 SOFTWARE INTERFACE

The status of the power converters may be determined by accessing their scan points (an SMPU4 function). A cable from the SMPU4 originating on the SN516B CP (Control and Display) controls the power modules and senses their alarms and presence. The power converters do not have any software addressable location. Due to the electromagnetic fields that are present on a power converter, it was not possible for the power converter to have an inventory PROM that is readable in the system.

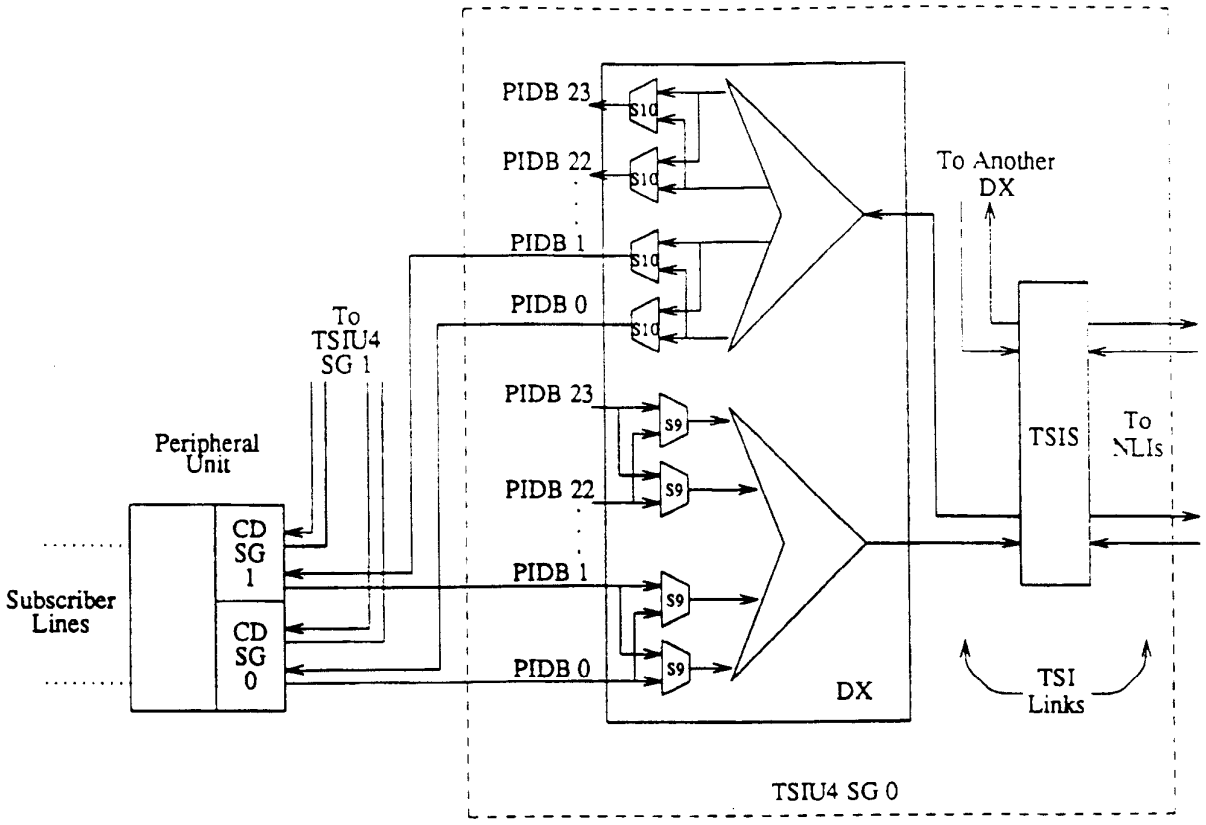


Figure 15. DX Circuit Pack Data Flow Diagram

4.2 CTSNS PADDLE BOARD

Each SM-2000 Release 1 TSIU4 service group will contain one CTSNS paddle board. Each CTSNS paddle board contains two dip switches that are used to store the TSI link byte numbers that will be used to transport the CTSs. One dip switch is used for the byte number for even links from CM side 0 and CM side 1; the other dip switch is used for the byte number for odd links from CM side 0 and CM side 1. The value stored in the dip switches on the two CTSNS paddle boards (one for each TSIU4 service group) must be the same. The mapping between the NCT sub-link 0 time slot number and TSI link byte number is shown in Table 7.

4.2.1 SOFTWARE INTERFACE

While there is no direct software access to the CTSNS paddle board, software can read the TSI byte number stored in the dip switches by reading the TSICTSN register in the IF 2 and IF 3 devices on the first TSIS circuit pack.

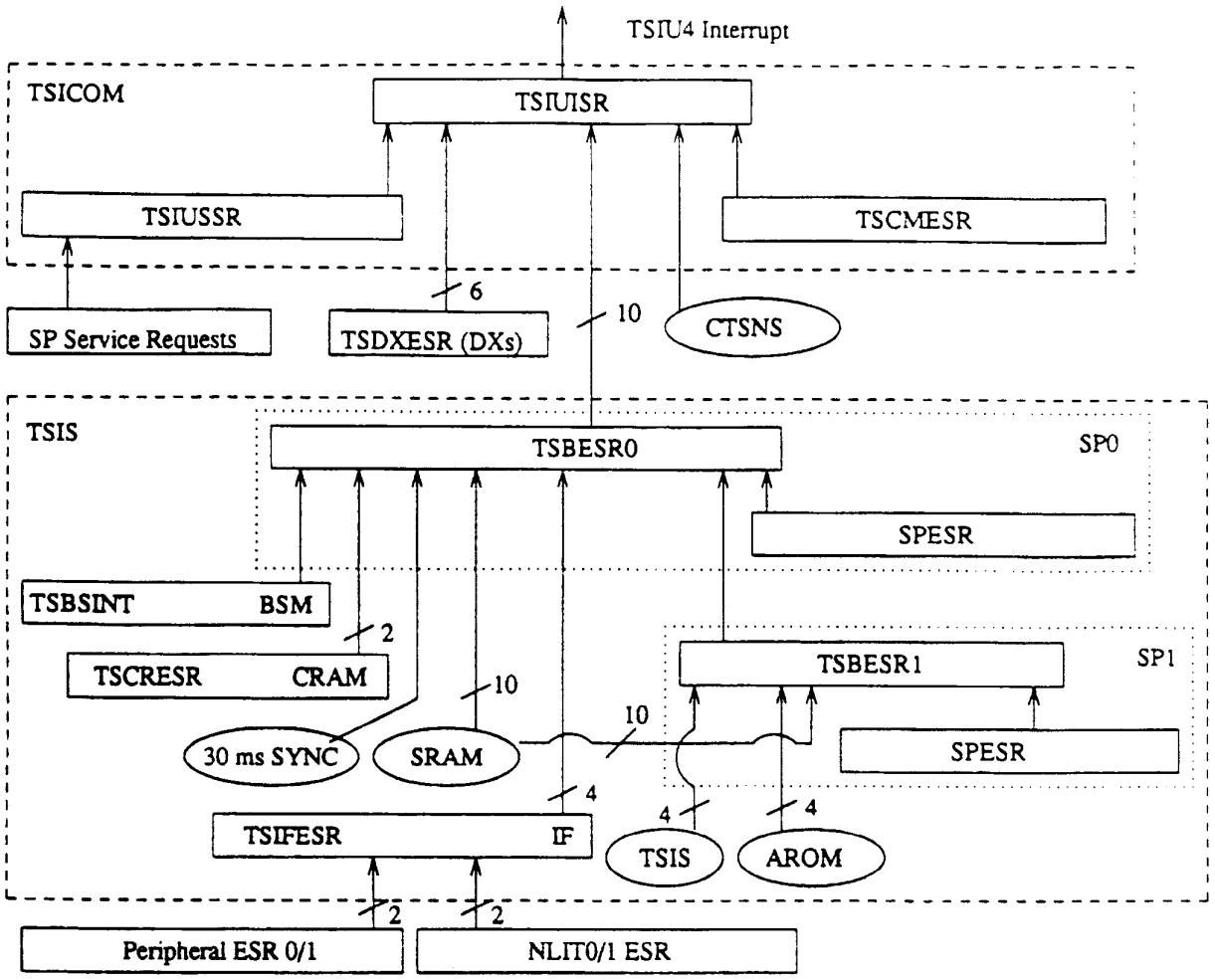
In the event that a CTSNS paddle boards is not equipped, the UCTSE bit in the TSIUISR register will be set, the UCTSP bit in the TSIUEQP register will be cleared, and the IF 2 and IF 3 devices on TSIS 0 will report an error, setting the ICTSE and ICT1E bits in their TSIFESR register. When the ICT1E bit is set (CTS byte number is all 1s), the SMPU4 can set the ICTSO bit in the TSIFCTL register and then write the desired byte number into the TSICTSN register. There may be some applications of SM-2000 after release 1, e.g., ORM-2000, for which the CTSNS paddle board may not be required, and thus not equipped.

TABLE 5. TSIU4 Address Map

Board	SMPU4 Address Range	Size (bytes)	TSIU4 Address Range	Size (longwords)
TSIS 0	0x30200000 - 0x3021ffff	128 k	0xc080000 - 0xc087fff	32 k
TSIS 1	0x30220000 - 0x3023ffff	128 k	0xc088000 - 0xc08ffff	32 k
TSIS 2	0x30240000 - 0x3025ffff	128 k	0xc090000 - 0xc097fff	32 k
TSIS 3	0x30260000 - 0x3027ffff	128 k	0xc098000 - 0xc09ffff	32 k
TSIS 4	0x30280000 - 0x3029ffff	128 k	0xc0a0000 - 0xc0a7fff	32 k
TSIS 5	0x302a0000 - 0x302bffff	128 k	0xc0a8000 - 0xc0affff	32 k
TSIS 6	0x302c0000 - 0x302dffff	128 k	0xc0b0000 - 0xc0b7fff	32 k
TSIS 7	0x302e0000 - 0x302fffff	128 k	0xc0b8000 - 0xc0bffff	32 k
TSIS 8	0x30300000 - 0x3031ffff	128 k	0xc0c0000 - 0xc0c7fff	32 k
TSIS 9	0x30320000 - 0x3033ffff	128 k	0xc0c8000 - 0xc0cffff	32 k
UNUSED	0x30340000 - 0x3035ffff	128 k	0xc0d0000 - 0xc0d7fff	32 k
DX 0	0x30360000 - 0x3036ffff	64 k	0xc0d8000 - 0xc0dbfff	16 k
DX 1	0x30370000 - 0x3037ffff	64 k	0xc0dc000 - 0xc0dffff	16 k
DX 2	0x30380000 - 0x3038ffff	64 k	0xc0e0000 - 0xc0e3fff	16 k
DX 3	0x30390000 - 0x3039ffff	64 k	0xc0e4000 - 0xc0e7fff	16 k
DX 4	0x303a0000 - 0x303affff	64 k	0xc0e8000 - 0xc0ebfff	16 k
DX 5	0x303b0000 - 0x303bffff	64 k	0xc0ec000 - 0xc0effff	16 k
TSICOM	0x303c0000 - 0x303c1fff	8 k	0xc0f0000 - 0xc0f07ff	2 k
UNUSED	0x303c2000 - 0x303fffff	248 k	0xc0f0800 - 0xc0fffff	62 k

4.3 CBT PADDLE BOARD

In order to provide the necessary electrical termination to the TSICNTL bus, each TSIU4 service group is equipped with two CBT paddle boards. One CBT terminates the TSICNTL bus for the DX circuit packs and the second CBT terminates the TSICNTL bus for the TSIS circuit packs.



NLIT0/1 - NLI Error Source Register for TSI link 0 and 1
SPESR - SP Device Error Source Register (SP0 & SP1)
TSBESR0 - TSIS/TSICOM Board Error Source Register in SP0
TSBESR1 - TSIS/TSICOM Board Error Source Register in SP1
TSCMESR - TSICOM Error Source Register
TSCRESR - CRAM Error Source Register
TSDXESR - DXC Device Error Source Register
TSIFESR - IF Error Source Register
TSIUISR - Interrupt Source Register
TSIUSSR - SP Service Request Register (NOT Errors)
CTSNS - Error Active When Board Not Equipped

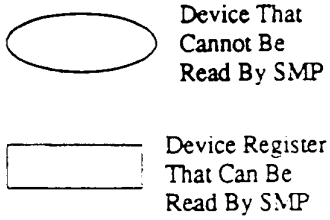


Figure 16. TSIU4 Interrupt Structure

TABLE 6. TSIU4 Switch Control Summary

Switch Num	Switch Description	Register	Bits
S1	Diagnostic/Maintenance Loopback Switch On *LI	Link Control	
S2	Diagnostic/Maintenance Loopback Switch On DX	TSDPLCR	All
S3	Side Selection for Network Time Slots (AUTISS) and PCT Peripherals	TSICRAM TSIFCTL	SDINV IESDI,IEAUT,ISIDE
S4	TSI Per Time Slot Loopback	TSICRAM TSIFDGC	ILOOP IDTSL
S5	Alternate PCM Data Insertion	TSSELCT	APCMA
S6	Alternate A-D Signaling Bit Insertion	TSSELCT	AATDS
S7	Alternate E-G Signaling Bit Insertion	TSSELCT	AEFGS
S8	TSI Idle Code Insertion	TSICRAM	IDLES
S9	Adjacent PIDB Data Fan-In Switch On DX	TSDXDIC	All
S10	Adjacent PIDB Data Fan-Out Switch On DX	TSDXDOC	All
S11	TSI Per Time Slot Loopback For SP	TSICRAM TSIFDGC	ILOOP ISPLB

4.3.1 SOFTWARE INTERFACE

There is no software interface for the CBT paddle boards.

4.4 PIB PADDLE BOARD

In order to ensure proper operation of the control and display circuit pack used for the SM2000 (SN516B) and the power converters used in the SMPU4 and TSIU4, it is necessary to equip each TSIU4 service group with a PIB paddle board when the second power converters are not equipped. If neither the second power converter nor the PIB paddle board is equipped, then neither the SMPU4 nor the TSIU4 will be powered up. Also, if both the second power converter and the PIB paddle board are equipped, then neither the SMPU4 nor the TSIU4 will be powered up. If DX5 or TSIS3 are plugged into the system and the second power supply is not equipped, the service group will not be allowed to power up. This prevents damage from occurring over connections between powered and unpowered boards.

4.4.1 SOFTWARE INTERFACE

There is no software interface for the PIB paddle boards.

4.5 DX/TSIS JMPR BOARD

The TSIS and DX port links are connected by means of these jumpers. The internal backplane wiring is connected to any of the circuit packs by these means. These jumpers are not required for the first DX/TSIS pair(0) as these connections are hardwired in the backplane. The jumpers should be installed in pairs per side (on DX and TSIS port) as needed with growth. See Figures 4c and 4d.

4.5.1 SOFTWARE INTERFACE

TABLE 7. Mapping From NCT Sub-Link 0 Time Slot Number To TSI Link Byte Number

NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte	NCT TS	TSI Byte
0	0x2	32	0x82	64	0x102	96	0x182	128	0x202	160	0x282	192	0x302	224	0x382
1	0x4	33	0x84	65	0x104	97	0x184	129	0x204	161	0x284	193	0x304	225	0x384
2	0x6	34	0x86	66	0x106	98	0x186	130	0x206	162	0x286	194	0x306	226	0x386
3	0x8	35	0x88	67	0x108	99	0x188	131	0x208	163	0x288	195	0x308	227	0x388
4	0x12	36	0x92	68	0x112	100	0x192	132	0x212	164	0x292	196	0x312	228	0x392
5	0x14	37	0x94	69	0x114	101	0x194	133	0x214	165	0x294	197	0x314	229	0x394
6	0x16	38	0x96	70	0x116	102	0x196	134	0x216	166	0x296	198	0x316	230	0x396
7	0x18	39	0x98	71	0x118	103	0x198	135	0x218	167	0x298	199	0x318	231	0x398
8	0x22	40	0xa2	72	0x122	104	0x1a2	136	0x222	168	0x2a2	200	0x322	232	0x3a2
9	0x24	41	0xa4	73	0x124	105	0x1a4	137	0x224	169	0x2a4	201	0x324	233	0x3a4
10	0x26	42	0xa6	74	0x126	106	0x1a6	138	0x226	170	0x2a6	202	0x326	234	0x3a6
11	0x28	43	0xa8	75	0x128	107	0x1a8	139	0x228	171	0x2a8	203	0x328	235	0x3a8
12	0x32	44	0xb2	76	0x132	108	0x1b2	140	0x232	172	0x2b2	204	0x332	236	0x3b2
13	0x34	45	0xb4	77	0x134	109	0x1b4	141	0x234	173	0x2b4	205	0x334	237	0x3b4
14	0x36	46	0xb6	78	0x136	110	0x1b6	142	0x236	174	0x2b6	206	0x336	238	0x3b6
15	0x38	47	0xb8	79	0x138	111	0x1b8	143	0x238	175	0x2b8	207	0x338	239	0x3b8
16	0x42	48	0xc2	80	0x142	112	0x1c2	144	0x242	176	0x2c2	208	0x342	240	0x3c2
17	0x44	49	0xc4	81	0x144	113	0x1c4	145	0x244	177	0x2c4	209	0x344	241	0x3c4
18	0x46	50	0xc6	82	0x146	114	0x1c6	146	0x246	178	0x2c6	210	0x346	242	0x3c6
19	0x48	51	0xc8	83	0x148	115	0x1c8	147	0x248	179	0x2c8	211	0x348	243	0x3c8
20	0x52	52	0xd2	84	0x152	116	0x1d2	148	0x252	180	0x2d2	212	0x352	244	0x3d2
21	0x54	53	0xd4	85	0x154	117	0x1d4	149	0x254	181	0x2d4	213	0x354	245	0x3d4
22	0x56	54	0xd6	86	0x156	118	0x1d6	150	0x256	182	0x2d6	214	0x356	246	0x3d6
23	0x58	55	0xd8	87	0x158	119	0x1d8	151	0x258	183	0x2d8	215	0x358	247	0x3d8
24	0x62	56	0xe2	88	0x162	120	0x1e2	152	0x262	184	0x2e2	216	0x362	248	0x3e2
25	0x64	57	0xe4	89	0x164	121	0x1e4	153	0x264	185	0x2e4	217	0x364	249	0x3e4
26	0x66	58	0xe6	90	0x166	122	0x1e6	154	0x266	186	0x2e6	218	0x366	250	0x3e6
27	0x68	59	0xe8	91	0x168	123	0x1e8	155	0x268	187	0x2e8	219	0x368	251	0x3e8
28	0x72	60	0xf2	92	0x172	124	0x1f2	156	0x272	188	0x2f2	220	0x372	252	0x3f2
29	0x74	61	0xf4	93	0x174	125	0x1f4	157	0x274	189	0x2f4	221	0x374	253	0x3f4
30	0x76	62	0xf6	94	0x176	126	0x1f6	158	0x276	190	0x2f6	222	0x376	254	0x3f6
31	0x78	63	0xf8	95	0x178	127	0x1f8	159	0x278	191	0x2f8	223	0x378	255	0x3f8

There is no software interface for the JMPR paddle boards.

5. TSIU4 INTERFACES

The following text identifies, briefly describes, and characterizes all of the external and internal interfaces associated with the TSI (includes DX) and NLI hardware. The term "external" refers to all interfaces that either enter or leave the TSIU4 unit. The phrase "internal interfaces" refers to interfaces between individual pieces of TSI/NLI hardware. All of the internal interfaces are in printed circuit form found in the TSIU4 backplane. Note that connections on the backplane to 982 type terminations and jumpers are also listed as an interface.

5.1 EXTERNAL INTERFACES

5.1.1 SERIAL TSI CONTROL LINK - STCL

The STCL bus provides control access to the TSI NLI from the processor. The STCL conists of a bibble wide data bus, clock, and sync, in both directions,an interrupt signal sourced from the TSICOM to the APC, and an active signal sourced from the APC to the TSICOM.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point - APC to TSICOM.
SPEED: 32Mhz (protocol - bursty in nature).
DRIVER/RECEIVER TECHNOLOGY: All signals differential TTL.
CABLE TYPE: Twisted shielded pair.
CONNECTOR TYPE: 982 type 2x12.
APPROXIMATE DISTANCE: 4ft.
NUMBER OF CONDUCTORS: 20.

5.1.2 MESSAGE, CPI, AND PUMP LINK - MCP

The MCP link carries the control time-slot (CTS), central processor intervention (CPI), and pump data between the APC and TSI. The MCP link conists of a bibble wide data bus, clock, and sync, all of which are bi-directional.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point - APC to TSI SLICE 0.
SPEED: 32Mhz continuous.
DRIVER/RECEIVER TECHNOLOGY: All signals pseudo-ECL logic levels, differential.
CABLE TYPE: Twisted shielded pair.
CONNECTOR TYPE: 982 type 2x12.
APPROXIMATE DISTANCE: 4ft.
NUMBER OF CONDUCTORS: 16.

5.1.3 NETWORK LINK INTERFACE - NLI

The NLI provides for one NCT2 link connection between the SM and TMS. The first two links, A and B, carry 512 PCM time slots, timing references, and CTS data. The remaining links, C - V, carry only PCM data.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point - NLI to TMS QLI.
SPEED: 65.536Mhz continuous.
DRIVER/RECEIVER TECHNOLOGY: 850 nm wave length, LED transmitter, PIN diode receiver, Optical.
CABLE TYPE: 62.5 micron multi-mode fiber.
CONNECTOR TYPE: AT&T - ST/bayonet.
APPROXIMATE DISTANCE: 0 - 2000ft.
NUMBER OF CONDUCTORS: 2 (transmit, receive).

5.1.4 PERIPHERAL INTERFACE DATA BUS - PIDB

The PIDB carries data to and from the peripherals. It consists of transmit data, receive data, clock, and sync.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point - DX to Peripheral.
SPEED: 4.096Mhz continuous.
DRIVER/RECEIVER TECHNOLOGY: Differential TTL 41NG (transmitter), 41LF (receiver) with termination.
CABLE TYPE: Tight twisted pair, teflon coated.
CONNECTOR TYPE: 963T type 2x4.
APPROXIMATE DISTANCE: 28ft.
NUMBER OF CONDUCTORS: 8.

5.1.5 CONTROL & DISPLAY INTERFACE - C&D

The control display interface cable provides for remote control and status from the C&D pack (SN516B) over TSIU power converters (486AA). Control includes power on/off, status includes power fail alarm and inter-lock feature; removal of any power converter in the MCTSI failure group results in an alarm.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Partially backplane, partially cable.
SPEED: Static.
DRIVER/RECEIVER TECHNOLOGY: Single ended TTL.
CABLE TYPE: 816A type loose twist.
CONNECTOR TYPE: 963T type 2x12.
APPROXIMATE DISTANCE: 5ft.
NUMBER OF CONDUCTORS: 9.

5.1.6 POWER FEEDERS

The power feeders carry -48v current from the fuse and filter unit directly to the TSIU backplane. Two feeders per side terminate one each behind the two TSIU4 power converters. A third feeder per side provides a -48v bus that runs the length of the backplane allowing NLIs to tap power.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Partially backplane, partially cable.
SPEED: N/A.
DRIVER/RECEIVER TECHNOLOGY: N/A.
CABLE TYPE: 16 gauge stranded for NLI, 12 gauge for TSI converters.
CONNECTOR TYPE: Spade.
APPROXIMATE DISTANCE: 3ft.
NUMBER OF CONDUCTORS: 8 (four feeders).

5.1.7 POWER INTERLOCK - PIB

There are two of these required (one per side) to insure proper power sequencing. Two 2X12s are tied together through a PC board with a relay and control logic.

5.1.8 CM2C UNIT INTERFACE TO THE SM2000 TSIU4 UNIT - NLI1

5.1.8.1 NETWORK INTERFACE

The TSIU4:

1. Provides connections, through a duplex TSI link, to duplex NLI1 paddle boards. Each NLI terminates one NCT link. One NLI will be connected to CM2C side 0, and one NLI1 will be connected to CM2C side 1.
2. Provides the capability to select, as a default, which of the duplex NLI1s to accept data from.
3. Provides the AUTISS function to autonomously select which NLI1 to use as the source for time slot data on a per time slot basis, depending on the state of the E signaling bit.
4. Provides the capability to select which of the duplex NLIs to use as the source for the clock. Data can be selected from one NLI1 while using the clock from the other NLI1.
5. Provides the capability to select which of the pair of duplex NLIs, that terminate the primary NCT links, to accept clock synchronization signals from.
6. Provides software with an indication that at least one time slot in each of the last 256 frames has been through the AUTISS function. Software can program which time slots will be used when determining this indication.

5.1.8.2 GENERAL CAPABILITIES

Provides a Stratum 4 clock reference that is synchronized to the timing reference received from the CM2C over one of the primary NCT links. The selection of the timing source is under software control.

5.1.8.3 BLOCK DIAGRAM OVERVIEW

The following components of the SM-2000 switching network terminate and generate new optical and electrical links based on the TSI link and are described further in their circuit description documents.

NLI1 The paddle board that terminates one NCT link, which carries 256 whole time slots, and one duplex TSI link (a simplex TSI link from each TSIU4 service group) and converts the data from one format to the other.

5.1.8.4 TSIU4 EQUIPAGE WHEN INTERFACE WITH CM2C SMALL OFFICE

For Release 1, a minimally equipped operational TSIU4 service group will contain:

1. One power converter
2. The TSICOM

3. One TSIS
4. One DX
5. Two control bus terminator (CBT) paddle boards
6. One control time slot number select (CTSNS) paddle board
7. One power interlock board (PIB) paddle board
8. Two NLI1 paddle boards

For local or host SM-2000s, network time slots arrive at the TSIU4 through TSI links from duplex NLI1s. Each of these TSI links will contain 256 time slots, thus 512 time slots of the 768 time slots on the TSI link will not be used. The mapping between the time slot numbers on the NCT link and the TSI link time slot numbers is shown in Figure 8.

5.1.8.5 NETWORK LINK INTERFACE ONE - NLI1 - SMALL OFFICE INTERFACE BOARD

The NLI1 is very similar to the NLI BKD1 design. The exceptions between the two boards (NLI1-BKD7 and NLI-BKD1) are:

- Link rate: NLI1-BKD7: 32.768 NLI-BKD1: 65.536 MHz
- Timeslots per link: NLI1-BKD7: 256 NLI-BKD1: 512
- Equipage in unit: NLI1-BKD7: Primary slots only NLI-BKD1: All slots
- CM interface: NLI1-BKD7: CM2C-SMLI only NLI-BKD1: CM2 TMS-QLI

All the functionality and design operation of NLI1 works exactly the same as the NLI as it interfaces with TSIU4 unit. The NLI1 provides for one NCT link connection between the SM and TMS. The links, A and B, carry 256 PCM time slots, timing references, and CTS data.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point - NLI1 to CM2C SMLI.
SPEED: 32.768Mhz continuous.
DRIVER/RECEIVER TECHNOLOGY: 850 nm wave length, LED transmitter, PIN diode receiver, Optical.
CABLE TYPE: 62.5 micron multi-mode fiber.
CONNECTOR TYPE: AT&T - ST/bayonet.
APPROXIMATE DISTANCE: 0 - 1000ft.
NUMBER OF CONDUCTORS: 2 (transmit, receive).

5.1.8.6 8K REFERENCE DISTRIBUTION

The four primary NLI1s, two on each side (0 and 1), recover timing from the incoming NCT links and pass that timing through 8Khz on to TSICOM by way of TSI slice 0. Each NLI1 sources two identical 8Khz references, one to side 0 and one to side 1 TSICOM. This is identical to NLI1 design described in a later section

5.2 INTERNAL INTERFACES

5.2.1 TSI TO NLI CROSS COUPLE

Consists of a bibble wide data bus, clock, and sync all of which are bi-directional.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point.
SPEED: 32.768Mhz.
DRIVER/RECEIVER TECHNOLOGY: Differential CMOS inputs and outputs.
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 16.

5.2.2 8K REFERENCE DISTRIBUTION

The four primary NLIs, two on each side (0 and 1), recover timing from the incoming NCT2 links and pass that timing through 8Khz on to TSICOM by way of TSI slice 0. Each NLI sources two identical 8Khz references, one to side 0 and one to side 1 TSICOM.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point.
SPEED: 8Khz.
DRIVER/RECEIVER TECHNOLOGY: CMOS,TTL single-ended
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 4 NLIs x 2 sides = Total 8.

5.2.3 TSICOM CLOCK CROSS COUPLE

The TSICOM clock cross couple carries phase and frequency information from one TSICOM to its mate allowing the mate to lock on to it. Each TSICOM sends to the other TSICOM a 8.192Mhz, 4.096Mhz, and a 30ms sync pulse.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point.
SPEED: 8.192Mhz, 4.096Mhz, 30ms sync.
DRIVER/RECEIVER TECHNOLOGY: 41MG (transmitter), 41MF (receiver) differential pseudo-ECL.
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 6 per cross couple X 2 = total 12.

5.2.4 TSI CLOCK DISTRIBUTION

A TSICOM circuit pack distributes a separate 32Mhz clock to each TSI slice and DX circuit pack and to the CTSNS paddle board.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point.
SPEED: 32.768Mhz.
DRIVER/RECEIVER TECHNOLOGY: 41MG (transmitter), 41MF (receiver) differential pseudo-ECL.
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 17 clocks x 2 (differential) = Total 36.

5.2.5 TSI SYNC DISTRIBUTION

A TSICOM circuit pack distributes a separate 30mS sync to each TSI slice and DX circuit pack and to the CTSNS paddle board.

INTERFACE SPECIFICATIONS:
CONNECTION TYPE: Point To Point.
SPEED: 32.768Mhz.
DRIVER/RECEIVER TECHNOLOGY: ABT244 with series resistor (TSICOM transmitter), F74 (TSIS receiver), DXC custom CMOS device (DXC receiver).
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 17

5.2.6 TSI DATA BUS - TSIDB

The TSIDB scheme is used to distribute the time slots received from the link interfaces to the TSI slice circuit packs. Up to ten buses (40 links) in the receive direction, one each from slices 1-10, terminate on slice 0 and contribute to the larger single transmit bus containing all 44 links worth of time slots.

Each receive bus contains four bibble wide data buses, sync, and a clock. The transmit bus contains 44 bibble wide data buses, sync and a clock. This bus utilizes the "one hop re-clock" scheme to avoid a multi-tap architecture.

INTERFACE SPECIFICATIONS - receive buses:
CONNECTION TYPE: Point To Point
SPEED: 32.768Mhz.
CABLE TYPE: Backplane printed circuit.
DRIVER/RECEIVER TECHNOLOGY: Single-ended advanced BI-CMOS TTL (ABT) transmitters and CMOS receivers on data and sync, differential clock.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 11.

INTERFACE SPECIFICATIONS - transmit bus:
CONNECTION TYPE: Point To Point
SPEED: 32.768Mhz.
CABLE TYPE: Backplane printed circuit.
DRIVER/RECEIVER TECHNOLOGY: Single-ended CMOS transmitters and receivers for data and sync, differential clock.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 91.

5.2.7 TSI CONTROL BUS - TSICNTL

There are two TSICNTL buses, one that extends across the lower portion of the TSIU4 backplane providing read/write access capability to the TSI slices and one that extends across the upper portion of the TSI backplane providing read/write access capability to the DX circuit packs. Both of these buses originate at the TSICOM circuit pack. Each bus consists of a 16 bit wide bi-directional multiplexed address/data bus, two bits of bi-directional parity, three control signals (select, direction, strobe) sourced from the TSICOM, and two signals (ready, interrupt) sourced from each TSI slice or DX depending upon the bus. Ready is common to all circuit packs while the interrupt is unique for each circuit pack on the bus.

INTERFACE SPECIFICATIONS:

CONNECTION TYPE: Multi-Tap bus using Tri-State.
SPEED: 16Mhz (protocol - bursty).
DRIVER/RECEIVER TECHNOLOGY: ABT inputs and outputs.
CABLE TYPE: Backplane printed circuit.
CONNECTOR TYPE: N/A.
APPROXIMATE DISTANCE: N/A.
NUMBER OF CONDUCTORS: 23 per TSIS. Because of some unique signals (interrupt, brdsel) per circuit pack attached to the bus, the bus that extends across the backplane is wider than 23.

CONTROL BUS TERMINATION: CBT - 2 2X12s tied together through PC with surface mount resistors, two per side.

6. REFERENCE DATA

6.1 EQUIPMENT LOCATIONS AND FUNCTIONAL DESIGNATIONS

Equipment locations and functional designations for all component codes in the TSIU4 are shown below:

EQL	FDESIG	MEANING	CIRCUIT PACK CODE
22-012	(0)PRS0	POWER CONVERTER 0	486AA
22-020	(0)TSICOM	TSICOM	UM74
22-028	(0)DX0	DATA EXPANSION PACK 0	UM73
22-036	(0)DX1	DATA EXPANSION PACK 1	UM73
22-044	(0)DX2	DATA EXPANSION PACK 2	UM73
22-052	(0)DX3	DATA EXPANSION PACK 3	UM73
22-060	(0)DX4	DATA EXPANSION PACK 4	UM73
22-068	(0)DX5	DATA EXPANSION PACK 5	UM73
22-088	(0)PRS1	POWER CONVERTER 1	486AA
04-018	(0)TSIS0	TSI SLICE PACK 0	KLU1
04-026	(0)TSIS1	TSI SLICE PACK 1	KLU1
04-034	(0)TSIS2	TSI SLICE PACK 2	KLU1
04-042	(0)TSIS3	TSI SLICE PACK 3	KLU1
04-050	(0)TSIS4	TSI SLICE PACK 4	KLU1
04-060	(0)TSIS5	TSI SLICE PACK 5	KLU1
04-068	(0)TSIS6	TSI SLICE PACK 6	KLU1
04-076	(0)TSIS7	TSI SLICE PACK 7	KLU1
04-084	(0)TSIS8	TSI SLICE PACK 8	KLU1
04-092	(0)TSIS9	TSI SLICE PACK 9	KLU1
22-108	(1)PRS0	POWER CONVERTER 0	486AA
22-116	(1)TSICOM	TSICOM	UM74
22-124	(1)DX0	DATA EXPANSION PACK 0	UM73
22-132	(1)DX1	DATA EXPANSION PACK 1	UM73
22-140	(1)DX2	DATA EXPANSION PACK 2	UM73
22-148	(1)DX3	DATA EXPANSION PACK 3	UM73
22-156	(1)DX4	DATA EXPANSION PACK 4	UM73
22-164	(1)DX5	DATA EXPANSION PACK 5	UM73
22-184	(1)PRS1	POWER CONVERTER 1	486AA
04-106	(1)TSIS0	TSI SLICE PACK 0	KLU1
04-114	(1)TSIS1	TSI SLICE PACK 1	KLU1
04-122	(1)TSIS2	TSI SLICE PACK 2	KLU1
04-130	(1)TSIS3	TSI SLICE PACK 3	KLU1
04-138	(1)TSIS4	TSI SLICE PACK 4	KLU1
04-148	(1)TSIS5	TSI SLICE PACK 5	KLU1
04-156	(1)TSIS6	TSI SLICE PACK 6	KLU1
04-164	(1)TSIS7	TSI SLICE PACK 7	KLU1
04-172	(1)TSIS8	TSI SLICE PACK 8	KLU1
04-180	(1)TSIS9	TSI SLICE PACK 9	KLU1

6.2 REFERENCE DOCUMENTS

Supplementary information is contained in the following documents:

(a) Switching Module Fuse/Filter Unit - CD-5D190-01

(b) Switching Module Fan Unit - CD-5D168-01

(c) Switching Module Processor Unit - CD-5D195-01

(d) Digital Service Unit - CD-5D197-01

(e) CPSM-486AA

(f) CPSM-KLU1

(g) CPSM-UM74

(h) CPSM-UM73

(i) CPSM-BKD1

(j) CPSM-BKD4

(k) CPSM-BKD7 (CM2C Small Office Design Interface board)

(l) CPSM-982AAB (CBT)

(m) CPSM-982AAE (PIB)

6.3 ACRONYMS

ABT	Advanced Bi-Complementary Metal Oxide Semiconductor (CMOS) Transistor to Transistor Logic (TTL)
APC	Applications Controller Circuit Pack
AROM	Attenuation Read Only Memory (ROM)
AUTISS	Automatic Time Slot Switching
BSM	Boundary Scan Master
BIST	Built-In Self Test
CBT	Control Bus Terminator
CM	Communications Module
CMOS	Complementary Metal Oxide Semiconductor
CM2C	Communication Module Small Office
CPI	Central Processor Intervention
CRAM	Control Random Access Memory
CTS	Control Time Slot
CTSNS	Control Time Slot Number Select
CRC	Cyclic Redundancy Check
DSU	Digital Services Unit
DSU3	Digital Services Unit, Model 3
DX	Data Expansion Circuit Pack
EMR	Error Mask Register
ESR	Error Source Register
FIFO	First-In First-Out
I/O	Input/Output

IF	Interface Device
IMR	Interrupt Mask Register
ISR	Interrupt Source Register
LDSF	Local Digital Service Function
MCP	Messaging, CPI and Pump
NCT	Network Control and Timing - Version 1
NCT2	Network Control and Timing - Version 2
NLI	Network Link Interface
NLI1	Network Link Interface To CM2C
OOS	Out Of Service
PCM	Pulse Code Modulation
PCT	Peripheral Control and Timing
PIB	Power Interlock Board
PIDB	Peripheral Interface Data Bus
PROM	Programmable Read Only Memory
RAM	Random Access Memory
ROM	Read Only Memory
SM	Switch Module
SM2000	Switching Module-2000
SMP	Switch Module Processor
SMPU4	Switch Module Processor Unit, model 4
SP	Signal Processor Device
SRAM	Static RAM
STCL	Serial TSI Control Link
TSI	Time Slot Interchange
TSICOM	Time Slot Interchange Common
TSIS	Time Slot Interchange Slice
TSIU	Time Slot Interchange Unit
TSIU4	Time Slot Interchange Unit, model 4
TTL	Transistor to Transistor Logic

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DEPT NA5350300-MS-FNG