ELECTRONIC SWITCHING SYSTEMS
5ESS® SWITCHING EQUIPMENT
DIGITAL CARRIER LINE UNIT
CIRCUIT

CHANGES

A. Changed and Added Functions

A.1

B. Changes in Apparatus

B.1 Added **P** option MC5D203A1C. Added **N** option MC5D205A1C.

C. Changes in Circuit Requirements Other Than Those Caused By Changes

C.1

D. Description of Changes

D.1 Added **N** option MC5D205A1C, ANN5C, and **P** option MC5D203A1C ANN3C Circuit Packs to drawing FS1 Figure, APP Figures, and Block Diagram 1. Added information note 314 and upgraded notes 302, 303, 304 and 309 to reflect the current information.

E. Changes in Transmission Test Requirements

E.1

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F. Changes in Description of Operation or Changes in CD Sections

F.1

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CIRCUIT

CHANGES

D. Description of Changes

D.01 Provide the lead index dropped during reissue 9/10.

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CIRCUIT

CHANGES

D. Description of Changes

D.1 Wiring options R and Q are added to show –48V bus wiring.

D.2 Information Notes 302 and 303 are updated to reflect options R and Q.

D.3 Information Note 311 is changed to reflect options R and Q.

D.4 Information Note 312 is added with additional information on options R and Q.

D.5 Allows use of 1249 cable as an alternative to ABAM or 600-type cable for T1 interconnections. Information Note 310 is added and Information Note 302 expanded to reflect the use of 1249 cable.

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CHANGES

D. Description of Changes

D.1 Wiring options S and T are added to show –48V bus wiring to ANN5B packs for RSM applications.

D.2 Information Notes 302 and 303 and APP FIG. 19 are changed to reflect options S and T.

D.3 Information Notes 304 and 309 are updated to show current production.

D.4 Information Notes 310 and 311 are added with additional information on –48V wiring.

D.5 CADs 002, 003, 004, and 005 are updated to show S and T options.

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HANGES

D. Description of Changes

D.1 Two new circuit packs, the ANN3B (MC5D203A1B) and the ANN5B (MC5D205A1B), have been added; they replace the ANN3 and the ANN5 circuit packs, respectively.

D.2 The ANN5 circuit pack cannot be used for multi-module remote switching modules (RSMs), whereas the ANN5B circuit pack can be used for multi-module RSMs as well as single-module RSMs.

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CHANGES

D. Description of Changes

D.1 This change adds restrictions to the use of the ANN3 (MC5D203A1) and the ANN5 (MC5D205A1) circuit packs. These packs can only be used in certain slots in a DLTU shelf. These slots are fixed by the software generic.

D.2 The above restriction applies to all ANN3 and ANN5 circuit packs.

D.3 The ANN3 and ANN5 circuit packs will be rated Mfr Disc and replaced by the ANN3B (MC5D203A1B) and ANN5B (MC5D205A1B) circuit packs, respectively.

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CHANGES

D. Description of Changes

D.1 The ANN3 (MC5D203A1) circuit pack replaces the ANN1 (MC5D201A1) circuit pack for the 5E1.2 release 1 and later software generics.

D.2 A new circuit pack, the ANN5 (MC5D205A1), may be optionally used in a DLTU. The ANN5 is used for RSM-FIU applications with 5E1.2 release 1 and later generics.

D.3 The unused FIU leads have been deleted.

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CIRCUIT

CHANGES

D. Description of Changes

D.1 Straps that are no longer needed have been removed from the backplane.

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ELECTRONIC SWITCHING SYSTEMS
NO. 5
DIGITAL LINE TRUNK UNIT
CIRCUIT

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The digital line trunk unit (DLTU) is a peripheral of the 5ESS digital switch. The DLTU allows the 5ESS to terminate digital trunks with a DS1 line format.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The DLTU consists of one 8-inch high shelf, one equalizer CP, one power start pack, and up to 10 digital facility interface (DFI) circuit packs. Each DFI terminates one T1 facility and converts it to the 5ESS peripheral interface data bus (PIDB) format. The PIDB then goes to the duplicated 5ESS time slot interchanger unit (TSIU). The T1 facility can be either the standard D4 channel bank format (ATT PUB-43801) or the extended framing (Fe) format (Technical Advisory No. 70).

2.02 Each DFI communicates with the duplicated 5ESS module processor (MP) via the peripheral interface control bus (PICB). The DFI monitors the T1 facility and reports to the MP, via the PICB, the following facility information:

- red alarm
- yellow alarm
- error rate
- severe errored seconds
- change-of-frame alignment count
- slip count
- errored seconds
- CRC-6 error count (Fe)
- out-of-frame count.

This facility monitoring meets or exceeds the requirements described in the Local Switching System General Requirement (LSSGR) document. See the LSSGR circuit and facility maintenance section for more details. In addition to monitoring, the MP may diagnose the DFI via the PICB.

SECTION II - DETAILED DESCRIPTION

1. EQUALIZER CIRCUIT PACK (CP SN215-219)

1.01 The equalizer CP contains 15 passive equalizers and therefore no power is required. Each DS1 signal leaving a DFI must go through an equalizer. The length of the cable between the DSX-1 crossconnect and the DLTU determines which equalizer code to use. (See Table A below.)

TABLE A

EQUALIZER CODE	CABLE LENGTH (FEET)
SN215	0-133
SN216	133-267
SN217	267-400
SN218	400-533
SN219	533-655

2. POWER START PACK (CP SN346)

2.01 The power start pack prevents the DLTU from powering up when the -48 volt supply is first applied. This is done to prevent current surges when the 5ESS is powered up. To turn on power, push the switch on the front of the power start pack. Once power is on, power cannot be turned off, even if circuit packs are replaced. A red LED indicator lights up if the DLTU is shut off. Two leads are distributed to the DFIs to turn power on while two leads enter the power start pack to indicate that DFI power is on.

3. DFI, CP MC5D203 (CP ANN3)

3.01 The ANN3 terminates the 24 time slot, 1,544 Mb/s T1 facility and converts it to a 32 time slot 4.096 Mb/s 5ESS PIDB format that is synchronized to the 5ESS system timing. Separate circuitry is provided for both the receive and transmit direction of transmission. In the receive section, the clock is extracted from the T1 facility. The framing is done to determine the time slot positions and the signaling frames. Next the line frame is synchronized with the PIDB frame. Finally, the signaling is extracted from the T1 signaling frame and put into the PIDB format.

3.02 In the transmit direction, the PIDB format is converted to the T1 line format. A phase lock loop is used to derive a synchronized 1.544-MHz clock from the 4.096-MHz PIDB clock.

3.03 Electrically, the T1 facility is a 1.544-Mb/s, 3-level, bipolar return-to-zero digital signal. The plus and minus levels correspond to a logic one while zero is a logic zero. The polarity of the logic one levels alternates between plus and minus, ie, +-+-0+00-+. (See TA34 for more details.)

3.04 Each DFI in the DLTU has two PICB interfaces: one PICB goes to side 0 while the other goes to side 1 of the duplicated 5ESS MP. The PICB consists of five twisted pairs of wires used to control the DFI from the 5ESS MP. One pair sends serial address and data to registers on the DFI from the MP. Another pair returns data to the MP when the MP reads DFI registers. This control data is clocked by a third signal from the MP. The clock is active only when control data is being sent or received. Another signal, the peripheral service request, is an active low signal sent by the DFI to the MP to indicate that the DFI needs service. Finally, one side of the 5ESS MP can gain control from the other side by changing state on the side select lead of the PICB.

3.05 The PICB interfaces to a microcomputer on the DFI pack which monitors the T1 facility for such things as slips, out-of-frames, etc, as mentioned in paragraph 2.02 of SECTION I.

3.06 Each DFI pack in the DLTU has two PIDB interfaces: one PIDB goes to side 0 while the other goes to side 1 of the duplicated 5ESS TSIU. The PIDB consists of four twisted pairs of wire. Two pairs are used to send the PCM data to and from the DFI. This dat consists of 32 16-bit time slots clocked at 4.096 Mb/s. Eight bits of each time slot are used for PCM data while the remaining eight bits are used for signaling and control. The two remaining pairs of wires supply a 4.096-MHz clock and an 8-kHz sync to the DFI for the time slot data.

3.07 The T1 facility has 24 eight-bit time slots followed by one framing bit. The ANN3 can be put into one of two framing modes. When the ANN3 is put into the standard D4 channel bank framing mode, the framing bit pattern in consecutive frames follows the D4 framing format as described in ATT PUB-43801.

3.08 The ANN3 may, under software control, be put into the extended framing (Fe) format as described in Technical Advisory No. 70. This format uses the T1 framing bit to do 24-frame super frame framing using 25 percent of the framing bits. Another 25 percent of the framing bits is used to do CRC-6 error checking. The remaining 50 percent of the framing bits are reserved for a 4-kb/s data link. This facility data link (FDL) is not used in the ANN3. The MC5D205 (ANN5) pack will use this data link, as described later.

A. ANN3 Signaling Options

3.09 The ANN3, under software control, can do one of five signaling methods. The first option uses 2-state signaling where the least significant bit of every time slot is robbed every 6th frame.

3.10 The second option is the D4 channel bank method of 4-state A and B bit robbed bit signaling in the 6th and 12th frames.

3.11 The third option provides 16-state A, B, C, and D bit robbed bit signaling in the 6th, 12th, 18th, and 24th frames. This signaling option must use the Fe framing format.

3.12 The fourth signaling option is to have no robbed bit signaling at all. All 24 time slots have no robbed bit signaling which, along with B8ZS and Fe out-of-band yellow alarm, provides the 64-kb/s clear channel capability.

3.13 The fifth signaling option is to put all of the signaling information into time slot 24. This leaves the remaining 23 time slots with a 64-kb/s clear channel capability, (ie, no robbed bit signaling). This signaling option must use the Fe framing format.

B. ANN3 Zero Code Suppression Options

3.14 To prevent too many consecutive zeros on the T1 facility, three zero code suppression options are provided under software control. The first option is not to provide zero code suppression.

3.15 The second zero code suppression option forces the least significant bit high in a time slot that has all zeros. This is the method used in D4 channel banks.

3.16 The third zero code suppression option is to use the bipolar with eight zero substitution (B8ZS) coding as described in Technical Advisory No. 69.

4. DFI, CP MC5D205 (CP ANN5) FOR RSM APPLICATIONS

4.01 The ANN5 does all of the functions of the ANN3 with the addition of a data link sent over the T1 facility. The Fe framing format uses half of the framing bits to generate the 4-kb/s data link. This data link will use a BX.25 level 2 protocol for data link control.

4.02 The link layer (level 2) of BX.25 is compatible with CCITT recommendation X.25 "Link Access Procedure" (LAPB), "International Standards Access Procedure" (ISO) standard, "High Level Data Link Control" (HDLC), and ANSI Standard "Advanced Data Communication Control Procedure" (ADCCP). For more information see TA 70 and PUB 54001.

4.03 The first application of the ANN5 is to remote a 5ESS interface module over a T1 facility. The ANN5, therefore, provides two additional outputs for the remote switching module (RSM). This is the T1 clock (1.544 kHz) that provides synchronization of the RSM with the host 5ESS and a T1 status lead to indicate the status (good/bad) of the T1 facility.

4.04 Since the ANN3 is a subset of the ANN5, the ANN5 may be used as a replacement for the ANN3.

5. DFI, CP MC5D200 (CP ANN1)

5.01 The ANN1 is an earlier version of the ANN3. The ANN1 will be available only as an addition to or replacement for existing DLTUs, using ANN1 (A&MO).

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The DLTU has an operating temperature range of 0°C to 70°C.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packs:

Designation	Meaning
(none)	Equalizer Pack
(none)	Power Start Pack
DFI	Digital Facility Interface
DFI-R or RSM-DFI	Digital Facility Interface for RSM Application

2.02 Interface Cables:

Designation	Meaning
PIDB	Peripheral Interface Data Bus
PICB	Peripheral Interface Control Bus

3. FUNCTIONS

3.01 The primary DLTU functions are:

(a) to frame on incoming T1 facility and synchronize to system timing.

(b) to convert from T1 format to PIDB format.

(c) to generate framing information on outgoing T1 facility.

(d) to monitor T1 facility and report problems to 5ESS MP.

(e) to provide a 4-kb/s data link on the T1 facility (ANN5 only).

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) The T1 facility interfaces with the DSX1 cross connecting bay, SD-99503-01.

(b) The PIDB interfaces to the 5ESS data interface (DI) circuit pack (CPS 836, CPS 837) which is part of the 5ESS interface module's TSIU (SD5D045-01).

(c) The PICB interfaces to the 5ESS control interface (CI) circuit pack, CPS TN 876 which is part of the 5ESS interface module MP (SD5D040-02).

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are contained in the following X-specifications.

(a) X-19829: Line Equalizer Circuit Pack, CPS SN215-219

(b) X-18928: Power Start Pack, CPS SN346

(c) X-19299: Digital Facility Interface, CPS ANN3

(d) X-19301: Digital Facility Interface For RSM Application, CPS ANN5.

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