ELECTRONIC SWITCHING SYSTEMS
5ESS® SWITCHING EQUIPMENT
DIGITAL CARRIER LINE UNIT
CIRCUIT

CHANGES

A. Changed and Added Functions

A.1

B. Changes in Apparatus

B.1 Added **Z** option MC5D204A1, and added **Y** option MC5D204A1B.

C. Changes in Circuit Requirements Other Than Those Caused By Changes

C.1

D. Description of Changes

D.1 Added **Z** option MC5D204A1, ANN4, and **Y** option MC5D204A1B, ANN4B circuit packs to drawings FS1 and FS2 figures, block diagrams BD1 and BD2. Added information notes 307 and 308 and upgraded notes 302, 303 and 304.

D.2 Added cabling information notes 305 and 306 on use of 1249 cable. Updated note 302 to reflect new 1249 cable use.

ELECTRONIC SWITCHING SYSTEMS
5ESS® SWITCHING EQUIPMENT
DIGITAL CARRIER LINE UNIT
CIRCUIT

E. Changes in Transmission Test Requirements

E.1

F. Changes in Description of Operation or Changes in CD Sections

F.1

AT&T BELL LABORATORIES

DEPT 54636-RCH-TJL

CIRCUIT DESCRIPTION

CD-5D202-01
ISSUE 2A
APPENDIX 1M
DWG ISSUE 3M
DISTN CODE BT13

ELECTRONIC SWITCHING SYSTEMS
5ESS SWITCHING EQUIPMENT
DIGITAL CARRIER LINE UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Allows the use of 1249 cable as an alternative to ABAM or 600-type cable for DS-1 interconnections. Information Note 305 is added, and Information Note 302 is expanded to reflect the use of 1249 cable.

AT&T BELL LABORATORIES

DEPT 54224-RCH-TJC

ELECTRONIC SWITCHING SYSTEMS
5ESS* SWITCHING EQUIPMENT
DIGITAL CARRIER LINE UNIT
CIRCUIT

TABLE OF CONTENTS — PAGE

Printed in U.S.A.

TABLE OF CONTENTS PAGE

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 One of the economic advantages of the 5ESS* digital switch is its ability to serve low telephone demand areas. The digital carrier line unit (DCLU), a peripheral of the 5ESS digital switch, implements this advantage. The DCLU allows the 5ESS to terminate digital subscriber lines with a DS1 line format and to provide varying concentration ratios of up to 9:1.

1.02 The Subscriber Loop Carrier (SLC*-96) is the system that the DCLU presently terminates.

2. GENERAL DESCRIPTION OF OPERATION

2.01 Fig. 1 is a overall block diagram showing the interrelationship among the 5ESS, the DCLU, and the SLC-96. For the purposes of this discussion the 5ESS office is shown to consist of three functional entities: Message switch, Switching Modules, and Line side connections. The DCLU is part of a switching module (SM). The SLC-96 is the remote terminal (RT) tying in as many as 96 subscribers.

2.02 The call-processing functions of the message switch consist mainly of routing and resource allocation. Routing involves the determination of the switching module on which the terminating line or trunk appears and the selection of an available trunk in a trunk group. The message switch also allocates and releases central resources, such as a time-multiplexed switch time slot.

2.03 In addition, the message switch performs many non-call-processing-related functions, such as error detection, diagnostics, and fault recovery. Within the message switch entity, there is error-checking circuitry for detecting and isolating faults.

2.04 Lines and trunks terminate on switching modules (SMs). These switching modules convert signals received from lines and trunks into the digital format used in the switch. The switching modules also perform time slot switching and most of the call processing.

2.05 Switching modules differ in the types and quantities of interface equipment they contain, depending upon the characteristics of the lines or trunks terminating thereon. Certain equipment is, however, common to all switching modules. The common equipment includes a pair of Digital Service Units (DSU), duplicated switching module processor units (SMPU), and duplicated time slot interchange units (TSIU). For simplicity, Fig. 1 shows a simplex configuration of a typical switching module (No. 2). Notice that the SMs connect to the message switch via Network Control and Timing Links, also referred to as NCT links. Notice also that this SM contains a DCLU which interfaces with the SMPU via a Peripheral Interface Control Bus (PICB) and the TSIU via a Peripheral Interface Data Bus (PIDB).

2.06 The DCLU is equipped with SLC* Digital Facility Interfaces (SDFIs), data multiplexers, control multiplexers, equalizers, and power units. Each SDFI terminates one T1 line coming from the SLC-96.

2.07 The SLC-96 carrier RT is that part of the digital subscriber system that is remote from the 5ESS switch office and is connected to it by T1 lines. An integrated SLC-96 carrier may operate in one or two modes (Mode I or Mode II). Mode I is the carrier-only mode in which up to 96 subscribers without concentration at the RT are provided with 96 channels to the 5ESS switch office. Mode II is the carrier-concentrator mode in which up to 48 subscribers share access to 24 channels to the 5ESS switch office (2:1 concentration ratio at RT).

2.08 The SLC-96 basically performs the following functions:

(a) Analog voice frequency signals from subscriber lines connected to the RT are converted to unipolar digital signals. In the opposite direction, unipolar digital signals are converted to analog voice-frequency signals for transmission to subscriber lines.

(b) Unipolar digital signals are synchronized into frames of time slots and are time multiplexed along with other signals into a bipolar serial bit stream for transmission to the 5ESS switch office. In the opposite direction, the RT demultiplexes signals from the bipolar serial bit stream. The digital signals are converted to unipolar then to analog voice-frequency signals and transmitted over the appropriate lines.

2.09 The RT is made up of four equipment shelves (A, B, C, and D) which consist of channel units (CUs) and common equipment circuit packs. Common equipment circuit packs are as follows:

- Power control unit (PCU)
- Line switch unit (LSU)
- Transmit/receive unit (TRU)
- Line interface unit (LIU)

- Time assignment unit (TAU)**
- Alarm control unit (ACU)
- Special service unit (SSU)
- Channel test unit (CTU)
- Data link unit (DLU).

2.10 Each SLC-96 carrier operating in Mode I (carrier-only) requires four to five T1 lines (four active and one optional protection standby). Each SLC-96 carrier operating in Mode II (carrier-concentrator) requires two to three T1 lines (two active and one optional standby) as shown. Each T1 line utilizes repeaters for digital signal regeneration.

> NOTE: SLC-96 shelves A and B, group A/B, interface with one T1 line, while shelves C and D, group C/D, connect to the other T1 line in Mode II configuration. In Mode I each shelf corresponds to one T1 line.

2.11 Data transmitted over the T1 digital line is a bipolar data stream sent at a 1.544 M bit/second rate (DS1). One T1 frame consists of twenty-four 8-bit time slots plus one additional bit referred to as the frame bit. To communicate control information over a T1 line, every other frame bit is used to form a derived data link. The communications over the derived data link are synchronous and a complete set of derived data fields are sent every 9 milliseconds. Each field is used to control and/or monitor RT operation.

** The TAU is required only in channel banks where the system is operating in Mode II (carrier-concentrator).

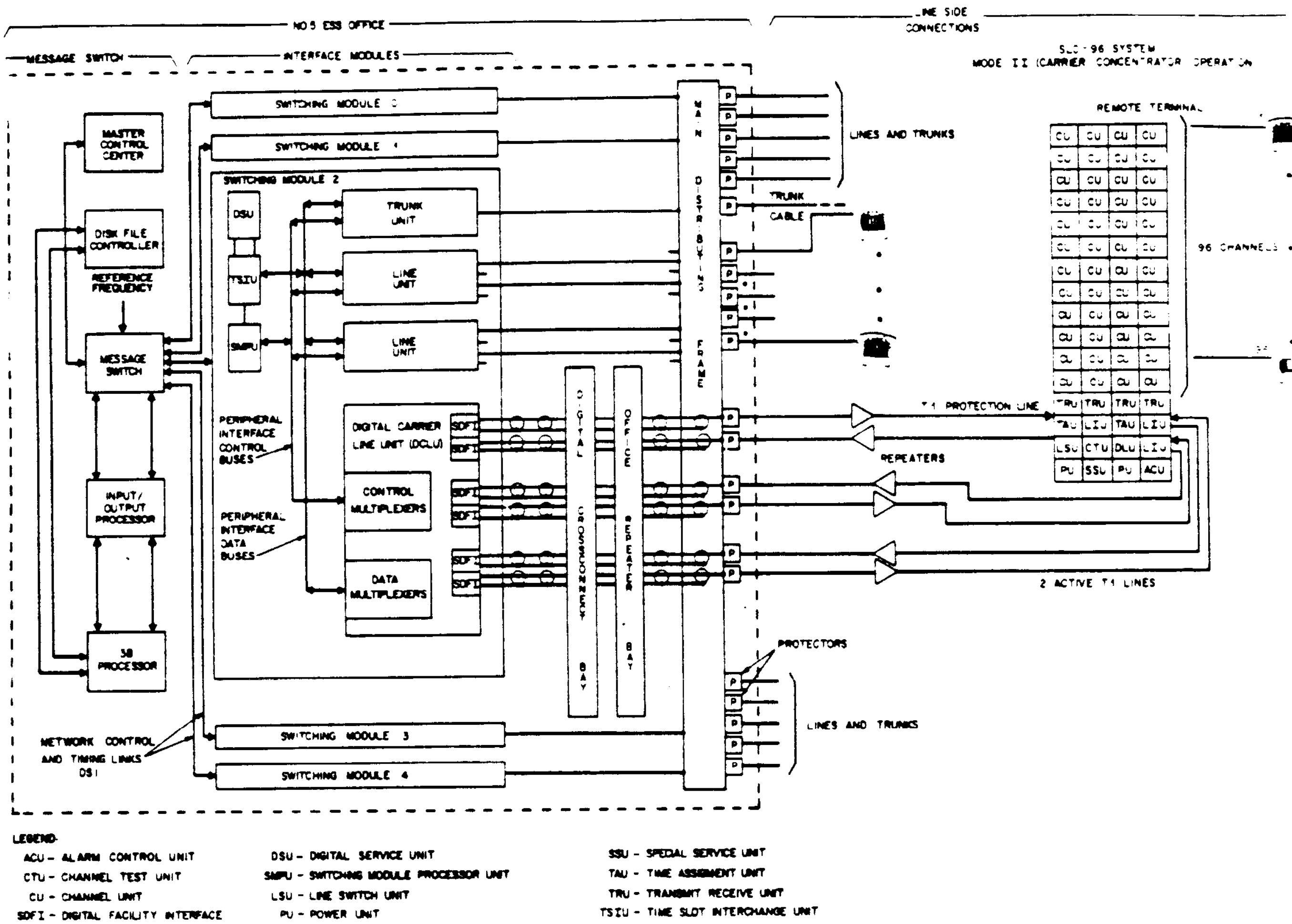


Figure 1 Block Diagram of SLC-96 Carrier Integrated into a Multi-module 5ESS Switch Office

SECTION II - DETAILED DESCRIPTION

1. BASIC OPERATION, SIGNALING, AND CIRCUIT PACK (CP) DESCRIPTION

DCLU BASIC OPERATION

1.01 The block diagram of the DCLU is shown in Fig. 2. The DCLU consists of two service groups. A maximum of six SLC-96 carrier RTs may be terminated on a DCLU. If one DCLU service group is removed from service, the other service group will handle data and control to and from the SDFIs in both service groups.

1.02 Each DCLU service group connects to the time slot interchange unit (TSIU) over two peripheral interface data buses (A and B), and each DCLU service group connects to the switching module processor unit (SMPU) over two peripheral interface control buses (A and B).

MODE I VERSUS MODE II

1.03 As mentioned in Section I, 2.10, Mode II operation is the SLC-96 carrier-concentrator mode. Since Mode II SLC-96 has a time slot interchange (TSI) capability at the RT, only a space switch is needed at the DCLU to provide concentration. This function is performed by the Data Mux circuit pack. However, to accommodate Mode I operation and because the MODE I SLC-96 has no TSI capability at the RT, the Digital Facility Interface CP (SDFI) provides this TSI function. Mode I SLC-96 RT, unlike the Mode II SLC-96 RT, has no signaling detection capability at the DCLU; hence this function is assumed likewise by the SDFI.

1.04 As shown in Fig. 2, Mode II operation has a maximum of 30 SDFIs while Mode I operation has a maximum of 18 SDFIs. Therefore, on the line (facility) side, the DCLU interfaces with six Mode II SLC-96 RTs. Each RT terminates 96 subscribers and concentrates them on to two T1 lines (48 channels). In addition, each RT has one spare T1 line. Thus Mode II operation requires maximum of (6X3) 18 SDFIs. Mode I operation performs no concentration; thus 96 subscribers are sent out on four T1 lines (24 channels) and one spare. Mode I operation requires maximum of (6X5) 30 SDFIs.

SLC* DIGITAL FACILITY INTERFACE (SDFI)

A. Purpose

1.05 The SDFIs (ANN4 circuit packs) terminate the SLC-96, T1 PCM digital lines to interface with the 5ESS via internal peripheral data and control buses as shown in Fig. 2. Each SDFI provides a direct digital interface for a T1 digital carrier line connected to a SLC-96 carrier RT. The SDFI in the DCLU converts the T1 line data format to the internal control and data line formats used in the 5ESS switch. Conversely, the SDFI converts data from a peripheral interface data bus (PIDB) and control information from a peripheral interface control bus (PICB) into a T1 line data format for transmission over a digital line.

B. Definition of PIDB, IPIDB, PICB, and IPICB

1.06 A PIDB or IPIDB consists of four electrical signals:

(a) 4-MHz clock lead

(b) 8-KHz Sync lead

(c) 32-time slot PCM data sent in one direction (4 Mb/s) lead

(d) 32-time slot PCM data sent in the opposite direction (4 Mb/s) lead

A PICB or IPICB consists of five electrical signals:

(a) 2-MHz burst clock lead

(b) write a register serial data lead

(c) read a register serial data lead

(d) interrupt lead

(e) control select lead

A PIDB and a PICB use balanced twisted pairs of wire, whereas an IPIDB and an IPICB use a single wire for each signal mentioned. Also an IPIDB has a slightly different timing than a PIDB.

---

* SLC is a Trademark of AT&T Technologies, Inc.

C. Conversion

1.07 The SDFI converts the 24-time slot, T1 line into two 32-time slot IPIDBs. One IPIDB connects to the Data Mux in service group 0, while the other IPIDB connects to the Data Mux in service group 1.

D. Origination, Signaling, and Maintenance

1.08 The ANN4 is designed to terminate either Mode I or Mode II SLC-96 RTs. A 4-KHz derived data link (DDL) carries origination information for the Mode II (concentrated) case, and a time slot interchanger and signaling LSI device (TSI-S) monitors the A and B signaling bits [see 1.03 for directing Mode I (unconcentrated) originations]. Some Mode II switched Special Services also have origination information in the A and B bits. In addition, since Mode I RTs have no TSI capability, the TSI-S device can interchange any incoming and outgoing time slot.

1.09 All origination processing and maintenance of the ANN4 is controlled by an on-board microcomputer (uC), with 4096 bytes of read only program memory and 256 bytes of scratch-pad RAM. Several options are available under software control regarding the way in which the DDL, TSI-S, and maintenance processing is handled.

Timing

1.10 T1 Line:

- 1.544 Mb/s
- 4-KHz DDL
- 24 time slots per 8-KHz PCM Frame
- 8 bits per time slot.

IPIDB:

- 32 time slots per 8-KHz, PCM Frame (4Mb/s)
- 4-MHz System Clock
- 16 bits per time slot
- 8-KHz System Sync

E. Summary

1.11 In summary, the ANN4 performs the following functions:

(a) Extracts PCM, signaling, and timing information from the incoming digital line.

(b) Reformats the data such that the per time slot signaling information is individually grouped with its associated PCM traffic data when it is sent to the TSIU via the Data Mux.

(c) Converts from line to system timing.

(d) Sends the PCM and signaling bits to the TSIU via the PIDB and via the Data Mux. The signaling bits are subsequently sent to the Signal Processor for further processing.

(e) Reformats and transmits the traffic and signaling bits received from the switch out on to the digital facility.

(f) Performs facility and circuit pack maintenance functions.

DATA MULTIPLEXER (DATA MUX)

A. Service Groups

1.12 As shown in Fig. 2, two identical Data Muxes are used in the DCLU, one for service group 0 and the other for service group 1. Each Data Mux concentrates PCM data from all SDFIs. Notice that any SDFI has a path (internal peripheral interface data bus) to both Data Muxes. Under normal operating conditions each Data Mux provides a concentration network for all the SDFIs.

B. Concentration

1.13 The DCLU via the two Data Muxes must concentrate the data from six RTs to four PIDBs. Each PIDB provides 32 time slots between the data interface of the SMPU/TSIU and the Data Mux. Thus, the concentration ratio for the SLC-96/DCLU system will be 576 (6X96) customers at full capacity to 128 (4X32) time slots, or 4.5:1. By removing two of the four PIDBs between the DCLU and the TSIU, the concentration ratio can be increased to 9:1.

1.14 The data concentrator is a space switch, and no time slot interchange capability is provided. Hence, the n-th time slot of the PIDB must come from the n-th time slot of any selected SDFI. This concentrator network when used in conjunction with the time slot interchanger found in ANN4 SDFI provides a rich network. Data concentrator control is provided by the Control Mux (Section II, 1.27).

C. Failure Operation

1.15 If one Data Mux fails, the other can take the additional concentration load; however, the concentration ratio doubles for it, hence traffic will be lower. If one Service Group is taken out of service for routine testing, software will route all new calls in the other Data Mux while the software will wait three minutes for old calls to be completed. Hence, no calls will be lost. Each SDFI must be told which Data Mux to get the 4.096-MHz clock and 8-KHz sync pulse. The SDFI reconfiguration is done through the Control Mux and 5ESS software.

D. PIDB-A and B Interfaces

1.16 As discussed, each of the two PIDBs (A and B) interface with the Data Mux in the same manner. A PIDB consists of two sets of twisted pair cables, each cable containing four twisted pairs. One set goes to side 0 of the SMPU/TSIU, and the other set goes to side 1. The four signals are described in Section II, paragraph 1.06.

1.17 For each PIDB, the incoming data must be selected from either side 0 or side 1, depending on which SMPU/TSIU is active. The Data Mux is told which side to listen to by a command from the Control Mux circuit pack. In the opposite direction, data is always sent to both TSIUs.

1.18 The PIDBs time slot data are validated by a parity loop-back circuit within the Data Mux. Each time slot coming to the Data Mux can have either even or odd parity in it. The requirement is that during the next frame, the Data Mux must send back the same sense of parity in each time slot that it received. For example, if the SMPU/TSIU sends odd parity in time slot 13 during a particular frame, odd parity must be sent back to the SMPU/TSIU in time slot 13 during the next frame.

1.19 The Data Mux accomplishes this by first detecting the sense of parity for each time slot. This information is sent to a parity generate circuit which uses this per-time-slot information to generate the correct parity on each time slot going back to the SMPU/TSIU. Because of the way that the incoming and outgoing data are aligned on the PIDB, a 28-time slot delay is needed between the detect circuit and the parity generate circuit to ensure that the parity sense is sent back out on the same time slot during the next frame.

1.20 Parity loop-back is the main technique used to protect the data. The Data Mux sends back to the SMPU/TSIU the same parity that it received on a PIDB for each time slot. The SMPU/TSIU is responsible for checking this looped-back parity and performing the necessary error analysis to determine whether the Data Interface (DI) or the PIDB/Data Mux is at fault. The same scheme is used on the IPIDB.

CONTROL MULTIPLEXER (CONTROL MUX)

A. Service Groups

1.21 As in the case of the Data Muxes, the DCLU has two Control Muxes, one for service group 0 and one for service group 1. Each connects to all of the SDFIs via IPICBs. See Fig. 2. Each IPICB provides different information to a particular Control Mux.

1.22 Under normal operating conditions, half the SDFIs are assigned to Control Mux 0, while the other half are assigned to Control Mux 1. If a Control Mux fails, both it and its corresponding Data Mux are removed from service. However, control to the SDFIs is not lost, because each Control Mux has full access to all SDFIs.

B. PICBs, SDFIs, 5ESS, and Data Mux Interfaces

1.23 Each Control Mux interfaces with the 5ESS SMPUs via two duplicated PICBs. PICB-A0 and B0 connect to the SMPU0, control interface (CI), while PICB-A1 and B1 connect to SMPU1 CI. See Fig. 2. The PICBs allow the SMPU to write registers in the Control Mux, Data Mux, and any SDFI.

1.24 From the hardware interconnect point of view, each PICB contains five pairs of wires. Each wire pair is used for communication in one direction only. Three wire pairs carry information from the SMPU to the Control Mux; these pairs include a 2.048-Mbit wire pair for data out and a 2.048-MHz wire pair for clock and an opto-isolated wire pair for control select. In the other direction, two pairs return information to the SMPU from the Control Mux. These pairs include: a 2.048-Mbit wire pair for data in and an opto-isolated wire pair for interrupt.

1.25 From the functional point of view, PICB-A connects the Control Mux and the SMPU together as described. PICB-B connects the SDFIs to the SMPU via the control Mux. It should be evident that two-way interaction between SDFIs and the SMPU uses all the hardware interconnection PICB wires. Thus, PICB-B configuration differs for each transaction (data-in and data-out).

1.26 PICB-A controls the switching of PCM data paths through the associated Data Mux as determined by 5ESS software from its corresponding SMPU. PICB-A, therefore, selects the particular SDFIs which will interface with PICB-B. This will occur when a service request occurs on PICB-B due to a service request condition in the SDFIs. PICB-B provides a path between the selected SDFI and the 5ESS SMPU for servicing and maintenance.

C. Data Mux Time Slot/Concentrator Control

1.27 For SDFI/time slot concentrator control, a time slot is selected to be sent to/from a particular SDFI. This is accomplished by 5ESS software via SMPU instructions to a time slot selector register in the Control Mux. Control information is transferred over PICB-A. In this way PICB-A controls the switching of the PCM data path (PIDB-A and PIDB-B) through the concentrator network. Since a time slot can be connected to different SDFIs, the control information must be sent for each PIDB time slot.

D. Fault Reporting/Failure Operation

1.28 The 5ESS software via the SMPU writes or reads the Control Mux registers. The latter replies to SMPU with an all-seems-well status. This 3-bit generated response determines whether faults lie in the control link portion of the Control Mux. If either the Control Mux or the Data Mux has failed, both are put out of service, and the other service group takes over.

E. Maintenance Exercises/Service Requests

1.29 A service request occurs on PICB-A only when an error condition exists. As a result maintenance exercises are requested. Then 5ESS software via the SMPU exercises the faulty device. The following are exercised:

(a) PICB-A and PICB-B serial loop back

(b) PICB-A/PICB-B service request

(c) Error source register

(d) SDFI select register

(e) TSSR A/B

(f) Time slot parity

(g) Parity checker device

(h) PICB-B and PICB-A side select

INTERNAL PERIPHERAL INTERFACE DATA AND CONTROL BUSES

A. General

1.30 The SDFIs interconnect with the Data Mux via the internal peripheral interface data buses (IPIDBs) and interconnect with the Control Mux via internal peripheral interface control buses (IPICB). As shown in Fig. 2, each SDFI connects to a service group, 0 and 1; thus each SDFI has four internal peripheral bus interconnects.

1.31 The IPIDB which connects to Data Mux 0 is identical with the one which connects to Data Mux 1. Each bus consists of four leads:

(a) SDFI transmit data providing a 32-time slot, 4 Mb/s data stream out

(b) 4-MHz SDFI clock

(c) 8-KHz SDFI frame sync

(d) SDFI receive path providing a 32-time slot, 4-Mb/s data stream in.

NOTE: The total data output from each SDFI is two, 32-time slot, 4-Mb/s data streams.

1.32 The IPICB which connects to Control Mux 0 is identical with the one which connects to Control Mux 1. Each bus consists of five leads as follows:

(a) 2-MHz burst clock

(b) 2-MHz control data out

(c) 2-MHz control data in

(d) clock select control (IPICB select

(e) Service request lead.

B. Timing

1.33 The IPIDBs used by the SDFIs have timing and format similar to PIDBs used by the Data Mux. Some timing changes are necessary, however, to accommodate the additional delay resulting from the Data Mux hardware. Of the four signals, only the 4-MHz clock remains unchanged in time relative to the PIDB timing from the DI. The IPIDB sync is advanced by 1/4 of a time slot (4-bits,about 1 usec) relative to the PIDB sync. Because the Data Mux data has a 1/4 time slot delay in the receiving direction, the IPIDB clocks data out of the SDFI 1/4 time slot earlier to the Data Mux to keep the PIDB standard. Therefore, the relationship between the SDFI data out and the sync it receives remains unchanged, and timing in this direction looks identical to a PIDB.

1.34 Data to the SDFIs, however, is delayed by 3/4 of a time slot(12 bits, about 3usec) relative to the data entering the Data Mux from the SMPU. This delay combined with the 1/4-time slot advance in the IPIDB sync, results in the IPIDB data being one full time slot late in reaching the SDFIs relative to the IPIDB sync. This then, is not a standard PIDB interface.

C. Control

1.35 In the SDFI a clock select circuit automatically switches IPIDBs' clocks, if a clock failure is detected. On the SDFIs, traffic can be transmitted and received on both IPIDBs simultaneously. A maximum of 24 out of 64 time slots may be active over both IPIDBs, while the other time slots have idle code. Idle code is different in each direction:

(a) From SDFIs to Data Mux, idle code= 01111111 0000111p =12345678 ABCDEFG where p=1 in odd numbered time slots.

(b) From Data Mux to SDFIs, idle code =01111111 1100110p=12345678 ABCDEFG where p is defined as in a.

DS1 FRAMING AND SIGNALING

A. Channel Frame DS-1 Format

1.36 As mentioned in Section I, 2.08 (b), unipolar digital signals are transmitted and received via a frame format. The DS-1 compatible frame, Fig. 3, consists of 24 consecutive 8-bit, PCM words preceded by one bit called the framing bit (F-bit) for a total of 193 bits per frame. The period equals 125 usec and the rate is 8000 frames per second. The bit rate is 1.544 Mb/s.

1.37 The 24 communication time slots are compatible numerically with the SLC-96 shelf capacity of 24 channel units (CU) as shown in Fig. 1. The 8-KHz frame rate

Table 1 - Channel Functional Identification

Channel Frame Number	F-Bit Channel Framing Ft-bit	F-Bit Signaling Framing Fs-bit	Information Coding Bits	Signaling Bit	Signaling Channel
1	1	-	1-8	-	-
2	-	0	1-8	-	-
3	0	-	1-8	-	-
4	-	0	1-8	-	-
5	1	-	1-8	-	-
6	-	1	1-7	8	A
7	0	-	1-8	-	-
8	-	1	1-8	-	-
9	1	-	1-8	-	-
10	-	1	1-8	-	-
11	0	-	1-8	-	-
12	-	0	1-7	8	B

is compatible with SLC-96 8-KHz PCM rate. Channel framing identifies the location of time slot one for each channel frame. Channel framing is achieved by alternating the F-bit (1,0,1,0.....) in the odd numbered channel frames. These alternating bits are referred to as Ft bits. See Table 1 and 1.42.

1.38 For MODE I operation a one to one relationship exists between CU location and channel frame time slot number. For MODE II operation, no fixed time slot to CU number exists. Instead, CU assignment to time slots is effected by DCLU messages via data links. See 1.42. These messages assign a line number to a time slot where the line number is related to the CU physical location.

B. Signaling Frame

Frame Format

1.39 A signaling frame consists of 12 consecutive channel frames and lasts 1.5 msec. See Fig. 4. Signal framing identifies those channel frames in which two signaling channels, called A and B, are transmitted on a time-shared basis. Signaling framing is achieved by setting the F-bits of even numbered channel frames to a 0,0,0,1,1,1 pattern. F-bits of this pattern are referred to as Fs bits. Table 1 presents the channel identification method. Note that the channel frames are identified by the odd-numbered channel F-bit alternating pattern (Ft bits) while the signaling frames are identified by the even-numbered channel s-bit a 0,0,0,1,1,1 pattern (Fs bits).

A and B Signaling Bits

1.40 The A and B signaling channels provide a per-channel signaling capability and are obtained by replacing the eighth bit (LSB) of the PCM word of the appropriate channel during the sixth and twelfth channel frames of each signaling frame. When the Fs bits are present, the sixth frame is identified as the frame following a "zero-to-one" Fs transition and the twelfth frame is identified as the frame following a "one-to-zero" Fs transition. When the Fs bits are replaced by data link bits, the sixth and twelfth frames must be identified by some equivalent means. The bit replaced in the sixth channel frame is termed the A-signaling bit; that replaced in the twelfth channel frame is termed the B-signaling bit. Figure 4 illustrates how the A and B signaling channels are identified. The sixth frame is expanded to show the 24 time slots. Any time slot can contain the A/B identifiers. In this case, time slot 10 (typical) has been expanded to show the PCM word's eighth bit on identifying A signaling bit (Table 1). In the twelfth frame the time slot 10, PCM word likewise shows the eighth bit on to identify B-signaling channel.

1.41 The A- and B-signaling bits provide for a maximum of nine possible signaling states by using a 3-level logic system that allows both the A- and B-signaling bits to take the values of either all ones, all zeros, or alternating ones and zeros. The relationships between channel frame, signaling frame, and per-channel signaling channels A and B are summarized in Table 1. The use of the A and B-signaling bits is CU dependent. The translation of signaling states to the values of the A- and B-signaling bits transmitted to and received from the DCLU on the derived signaling channels is defined in Table 2 for the various SLC-96 system channel unit types.

C. Derived Data Link (DDL) Frame

General

1.42 A data link frame is composed of six consecutive signaling frames and is 9 msec long. See Fig. 5. Data link framing identifies those signaling frames in which the signaling framing bits (Fs) are replaced by bits that comprise a serial data link message. Data link framing is achieved by transmitting the signaling framing pattern twice in succession during six consecutive signaling frames. The first two frames represent resynchronization data as shown in Fig. 5. During the last four signaling frames the Fs bits are replaced with data link bits.

Derived Data Link

1.43 The derived data link (DDL) carries control and alarm information between the RT and the DCLU. Two data links, called the A data link and the C data link, are transmitted over the A and C DS-1 links, respectively. The A data link is always present; the C data link is present only if SLC-96 shelf group CD is operating in Mode II. The data link is referred to as "derived" since it is formed by displacing Fs bits. Normal signaling framing is present on DS-1 links that do not have a DDL.

Data Link Format

1.44 The data link consists of 24 Fs bits which are grouped into six fields of fixed format as follows:

Fs bits 1-11	Concentrator field (C-field)
Fs bits 12-14	Spoiler Bit field (fixed pattern of 010)
Fs bits 15-17	Maintenance field (M-field)
Fs bits 18-19	Alarm Data Link field (A-field)
Fs bits 20-23	Protection Line Switch field (S-field)
Fs bit 24	Spoiler Bit field (fixed pattern of 1)

1.45 The structure of the DDL frame is shown in Fig. 5. All fields are present on the a data link; the C-field is used, however, only if shelf group AB is operating in Mode II.

1.46 The spoiler bit fields shown are required to prevent the RT from misframing due to the inadvertent transmission of the signaling framing pattern. There are no other restrictions on the content of any field (or portion of any field) transmitted to the DCLU that is not used on either data link.

Concentrator Field

1.47 The C-field is used to control channel assignment/deassignment and other functions relating to Mode II operation. The A data link C-field carries information for both SLC-96 shelves A and B and is used only if shelf group AB is operating in Mode II. On the C data link the C-field carries information for both shelves C and D and is used only if shelf group CD is operating in Mode II. Message specifications and communication protocol are discussed in the subsequent paragraphs, while maintenance functions are discussed in SECTION II 2.20 through 2.33.

C-Field Messages Sent From DCLU

1.48 The C-field messages that can be sent from the DCLU are given in Table 3. These messages control DS-1 time slot assignment/deassignment and various maintenance functions. Each message except "Idle" requires three data link frames (27 ms) for transmission. Those messages consisting of three identical submessages will be recognized at the RT only if at least two of the three submessages agree; otherwise, the message will be ignored. All three of the submessages that make up a three part message must be sent to the RT before sending another new message to the RT. When the first two submessages agree, a message will be recognized at the RT after only two frames (18 ms). Messages consisting of a header followed by a true submessage and its complement will be recognized at the RT only if the true and complemented submessages agree.

Table 2 - Signaling States for RT Channel Units

Channel Unit Type	Station Condition To Channel Unit	Bits Received From The Digital Interface A	Bits Received From The Digital Interface B	Bits Sent To The Digital Interface A	Bits Sent To The Digital Interface B	Channel Unit Condition To Station
Single Party	On-Hook	0	0	0	1	Channel Test
	Off-Hook	1	0	1	0	Forward Disconnect
	Unequipped	1	1	1	1	Idle [4]
				1	1/0	-R Ringing
Superimposed Ringing Multiparty (SPR-MP)	On-Hook	0	0	0	1	Channel Test
	Tip Party Ground	0	1	1	0	Tip Party Test
	Off-Hook	1	0	1	1	Idle [4]
	Unequipped	1	1	1	1/0	-R Ringing
				10	0	+T Ringing
				10	1	-T Ringing
				10	1/0	-R Ringing
Frequency Selective Ringing Multiparty (FSR-MP)	On-Hook	0	0	0	1	Channel Test
	Off-Hook	1	0	1	1	Idle [4]
	Unequipped	1	1	1	1/0	Freq Band 1 Ringing [5]
				1/0	1/0	Freq Band 2 Ringing [5]
				1/0	1	Freq Band 3 Ringing [5]
				1/0	0	Freq Band 4 ringing [5]
Coin	On-Hook	0	0	0	0	Negative Loop Mode
	Coin Ground	0	1	0	1	Channel Test
	Off-Hook	1	0	1	0	Positive Loop Mode
	Unequipped	1	1	1	1	Ground Start [4]
				0	1/0	Positive Coin Check
				1	1/0	-R Ringing
				1/0	0	Coin Collect
				1/0	1	Coin Return
				1/0	1/0	Negative Coin Check
Ground Start	On-Hook	0	0	0	0	Ground Start
	Ring Ground	0	1	0	1	Channel Test
	Off-Hook	1	0	1	1/0	-R Ringing
	Unequipped	1	1	0	1/0	Idle

Notes:

1. A and B bit values are given as they appear on the DS-1 links.
2. 1/0 indicates alternating 1s and 0s.
3. Unused signaling states are not sent to the DCLU.
4. This code is sent to the DCLU for channels that are unassigned or installed but not in use, except as otherwise noted.

Table 3
C-Field Messages Sent From DCLU

MESSAGE FUNCTION	FORMAT		
Trunk Assign/ Deassign	MESS1	MESS1	MESS1
Assignment Update	HEADER	MESS1	CMESS1
Looping Test	HEADER	MESS2	CMESS2
Activity Update Request	MESS3	MESS3	MESS3
Idle	MESS4		

NOTES:

1. The format shown here represents the three submessages that are sent to the RT in the concentrator data bit fields of three consecutive DDL frames; the left-most of these submessages is sent first. Bit C1 is the most significant bit (MSB) of each submessage and is sent first. The submessages are defined as follows:

   MESS1: Bits C6-C11 (C6 is the MSB) are the binary representation of the line number (0-47) or the deassignment command (63). Bits C1-C5 (C1 is the MSB) are the binary representation of the time slot number (1-24).

   CMESS1: Complement of MESS1.

   HEADER: Bits C1-C11 set to octal 3470.

   MESS2: Bits C1-C11 set to octal 3714.

   CMESS2: Complement of MESS2.

   MESS3: Bits C1-C11 set to octal 3466.

   MESS4: Bits C1-C11 set to octal 3760.

2. The "Idle message consists of only one submessage.

C-Field Messages Sent to DCLU

1.49 The C-field DDL messages that can be sent to the DCLU are shown in Table 4. These messages contain both activity and maintenance information. Activity messages report a transition from on-hook to off-hook or vice versa. The "Idle" message will be received from the RT in the absence of any other messages. As in the case of messages transmitted from the DCLU, each received message except "Idle" is three data link frames (27 ms) long. No new messages will be received from the RT before the message currently in progress is completed. Messages received from the RT are interpreted using the protocol described in 1.48. For example, if a 3-part message is received from the RT and none of its three submessages agree, the entire message will be discarded. If, however, the garbled message received from the RT is (or could be) the response to a message sent to the RT, the message that was originally sent to the RT is sent again.

Table 4

C-field Messages sent to DCLU

MESSAGE FUNCTION	FORMAT		
Activity	MESS1	MESS1	MESS1
Activity Update	HEADER	CMESS1	MESS1
Looping Test	HEADER	CMESS2	MESS2
Assign Update Request	MESS3	MESS3	MESS3
Idle	MESS4		
No Alarm	MESS5	MESS5	MESS5

NOTES:

1. The format shown here represents the three submessages that are received from the RT in the C-fields of three consecutive DDL frames; the left-most of these submessage will be received first. Bit C1 is the most significant bit (MSB) of each submessage and will be received first. The submessages are defined as follows:

   MESS1: A line is said to be "active" if its A and B signaling bits are in any state other than "on hook" or "unequipped." The number (1-6) of each of the six 8-line groups is coded in bits C1-C3. Bits C4-C11 indicate which of the eight lines in a line group are active. A "one" in any of bits C4-C11 indicates that the corresponding line is active. See Table 5 for the mapping between line numbers (which in turn are defined in Table 6) and MESS1 bits C1 to C11.

   CMESS1: Complement of MESS1.

   HEADER: Bits C1-C11 set to octal 3470.

   MESS2: Bits C1-C11 set to octal 3714.

   CMESS2: Complement of MESS2.

   MESS3: Bits C1-C11 set to octal 3466.

   MESS4: Bits C1-C11 set to octal 3760.

2. The "Idle message consists of only one submessage.

Table 5
Mapping between Line Numbers
and MESS1 Bits in "Activity" Messages

Line Group	C4	C5	C6	C7	C8	C9	C10	C11
1	2	3	4	5	6	7	8	9
2	10	11	12	13	14	15	16	17
3	18	19	20	21	22	23	24	25
4	26	27	28	29	30	31	32	33
5	34	35	36	37	38	39	40	41
6	42	43	44	45	46	47	0	1

NOTES:

1. The Line Group (1-6) is given (in binary) by bits C1 to C3. (C1 is the most significant bit and will be received at the Digital Interface first.)

2. A "one" ("ones") in any of bits C4 to C11 indicates (indicate) the "active" state for the line number(s) given by the element(s) in this table that is (are) at the intersection(s) of the row corresponding to the Line Group specified in bits C1 to C3 and the column(s) corresponding to the bit(s) (C4 to C11) having a "one" ("ones") in it (them).

Table 6 - Line No./Shelf Group Channel No. Assignments for Mode II

Line No. Used In C-Field Messages	Shelf Group AB Channel No.	Shelf Group CD Channel No.
0	1	49
1	25	73
2	13	61
3	37	85
4	2	50
5	26	74
6	14	62
7	38	86
8	3	51
9	27	75
10	15	63
11	39	87
12	4	52
13	28	76
14	16	64
15	40	88
16	5	53
17	29	77
18	17*	65*
19	41*	89*
20	6	54
21	30	78
22	18**	66**
23	42**	90**
24	7	55
25	31	79
26	19*	67*
27	43*	91*
28	8	56
29	32	80
30	20**	68**
31	44**	92**
32	9	57
33	33	81
34	21*	60*
35	45*	93*
36	10	58
37	34	82
38	22**	70**
39	46**	94**
40	11	59
41	35	83
42	23*	71*
43	47*	95*
44	12	60
45	36	84
46	24**	72&&
47	48**	96

* These channels may be used for coin or D4 special service.

** These channels are not used when the preceding number channel is used for coin or D4 special services.

Maintenance Field

1.50 The M-field (Fig. 5) is used to control channel and distribution pair (drop) testing. The A data link M-field carries information for all shelves. Specification of the messages sent over the M-field and their timing requirements are discussed in 2.21.

Alarm Field

1.51 The A-field is used to transmit or receive alarm information or system control commands; the A data link A-field carries these for all shelves. The A-field is used to send one 2-bit message during each data link frame. Since the system requires more alarm messages than is possible with only two bits, an alarm data link frame, which consists of either thirteen or sixteen consecutive data link frames, as described below, is created.

1.52 The alarm data link frame leaving the DCLU will always consist of sixteen consecutive data link frames independent of the type of ACU installed in the RT.

1.53 Alarm data link framing is identified by the framing alarm message that consists of both alarm field bits equal to "one". (See Fig. 5.) The alarm data link frame permits assignment of messages to specified alarm conditions or system control commands. The various formats of the alarm data link frame and specification of the messages sent over the A-field are defined.

Protection Line Switch Field

1.54 The S-field (Fig. 5) is used to control the switching of the protection DS-1 link. The A data link S-field carries information for all shelves. Specification of the messages sent over the S-field and their timing requirements are defined.

2. FUNCTIONAL DESCRIPTION

2.01 To accomplish its purpose the DCLU performs the following functions:

(a) Converts T1 line data format to 5ESS internal data and control line formats

(b) Provides data concentration

(c) Detects line signals

(d) Monitors alarms and implements maintenance exercises.

2.02 These functions are described in the paragraphs that follow. The discussions in some instances make reference to SD-5D202-01 Block Diagram 1 and 2 (BD1 and BD2). In referring to these block diagrams note that the DCLU makes use of 20 SDFIs rather than 30 as discussed in previous paragraphs. Ten additional SDFIs can be added with the DCLU-SUPP - SD203-01.

T1/DS1 5ESS FORMAT CONVERSION

A. Unipolar/Bipolar and T1 Line Format

2.03 The SLC-96 performs a framing operation and a unipolar to bipolar conversion. The T1 line carries a 1.544 Mb/s data stream which is formatted into a 24-time slot (8-bit per time slot) channel frame occuring at an 8-KHz rate. This digital stream passes via a DSX-1 cross-connect to connector J2, as shown in BD1. In Mode II operation, two T1 lines and the protection line come from each SLC-96 RT. In the present configuration the DCLU is capable of handling six SLC-96 RTs operating in Mode II. Three are handled by DCLU shelf 0 while the other three are handled by shelf 1. A T1 line consists of two twisted pairs of wires.

B. T1 Line Format to 5ESS Format Conversion

2.04 Each SDFI analyses the T1 line format serial bit stream. It syncs on to the line timing established by the F-bits (framing bits) and reframes the data stream into two 32-time slot (16-bit per time slot), 4-Mb/s data streams.

2.05 Each data stream goes out on a separate lead of an IPIDB. One of these leads feeds Data Mux 0 via one IPIDB, while the other lead feeds Data Mux 1 via the other IPIDB.

C. Timing and Sync/Send and Receive

2.06 Timing and sync signals are taken from the Data Mux via the IPIDB. The IPIDB comprises:

(a) Time slot data out to Data Muxes

(b) 4-MHz clock

(c) 8-KHz sync

(d) Time slot data in from Data Muxes.

D. Failure Operation

2.07 By switching to the protection line, software can take any SDFI out of service without taking any customer out of service.

E. BD2

2.08 Equipment shown on BD2 operates identically as that on BD1. Thus, six RTs are handled via SDFIs. In the event of a failure of either Data Mux, the other takes over via the buses from the other shelf. The 50-lead bundles interconnecting control Muxes provide the necessary control to effect shutdown of one Service Group and allowing the other to take over the full load.

CONCENTRATION

A. Mode I versus Mode II

2.09 As mentioned in Section II, 2.10, the facts determining whether the DCLU operates in Mode I or Mode II is the physical makeup of the SLC-96-RT. Fig. 1 showed a schematic representation of a typical Mode II designed SLC-96. Table 7 shows a typical SLC-96 Mode II shelf arrangement.

2.10 A SLC-96 RT channel bank consists of four shelves that are referred to as the A, B, C, D shelves. Each shelf contains 12 slots for channel unit plug-ins and additional slots for common equipment plug-ins. This 96-channel bank is made up of upper and lower shelf groups of 48 channels each (24 slots), called shelf group CD and shelf group AB, respectively. Aside from certain common maintenance functions, the protection T1 line, the ringing generator, and the powering equipment, shelf group AB and shelf group CD operate independently of each other.

Table 7

RT Channel Bank Physical Channel Numbering Scheme

CD Group	73/74	75/76	77/78	79/80	81/82	83/84	85/86	87/88	89*/90	91*/92	93*/94	95*/96	SHELF D
	49/50	51/52	53/54	55/56	57/58	59/60	61/62	63/64	65*/66	67*/68	69*/70	71*/72	SHELF C
AB Group	25/26	27/28	29/30	31/32	33/34	35/36	37/38	39/40	41*/42	43*/44	45*/46	47*/48	SHELF B
	1/2	3/4	5/6	7/8	9/10	11/12	13/14	15/16	17*/18	19*/20	21*/22	23*/24	SHELF A

* For Mode II, single circuit plug-ins may only be used in the channel unit positions to the right of the double bar; the star (*) indicates the channel unit number that should be assigned a time slot when so utilized.

2.11 Mode I refers to a nonconcentrated shelf group that is served by two primary T1 lines. Each of the two shelves in the shelf group is served by a dedicated T1 line having the same designation (A, B, C, or D) as the shelf it serves. For example, if shelf group AB is operating in Mode I, its A shelf is served by the A T1 line and its B shelf by the B T1 line. If all 12 slots of a shelf are filled with dual circuit channel units, the 24 time slots on the T1 line associated with that shelf are fully utilized. Single circuit channel units may be substituted for dual circuit channel units with no restrictions.

However, for each single circuit channel unit that replaces a dual circuit unit, one time slot on the T1 line will be unused.

2.12 Mode II refers to a shelf group that uses a digital concentrator and is connected to the DCLU by one primary T1 line. The A T1 line is used for shelf group AB and the C T1 line for shelf group CD. A maximum of 24 dual single party or multiparty channel units may be plugged into the channel unit slots in a shelf group, resulting in 48 lines competing for the 24 T1 time slots, or 2:1 concentration. Although either dual or single circuit channel units can be used, only the dual circuit types are concentrated. The concentration ratio remains at 2:1 even if single circuit channel units are substituted for dual circuit ones since each single circuit channel unit displaces one dual channel unit and takes away one T1 time slot. In order to maintain sufficient traffic capacity, a minimum of 16 time slots on each T1 line must be available for concentrated traffic. Hence, a maximum of 8 single circuit channel units may be assigned to a shelf group. Furthermore, in Mode II, Coin or D4 special service plug-ins may be used only in the four rightmost channel unit slots on each shelf (see Table 4).

CALL AND CONTROL SIGNALING DETECTION

2.13 Call control of individual customer channels depends upon modes of operation of the SLC-96 and the Channel Unit (CU) types installed. For all modes the signaling channel bit patterns are sent to and received from the DCLU which detects A and B sub-channels used to convey information.

2.14 In addition, controlling a MODE II system requires sending and receiving specified messages in the C-field of the DDL that is carried on the DS-1 link over which the customer will be served. See 1.43 through 1.49. The DCLU/SLC-96 interaction follows a prescribed protocol. The only call control information not sent over the served DS-1 link is alarm information indicating that it is out of service. This alarm information is sent over the DDL A-data Link. See Section I, 2.01. The discussion that follows applies to SLC-96 single party CU's only.

A. OFF-HOOK/Dial Tone Call Origination

2.15 During on-hook conditions for Mode II operation, the customer loop pair between the subscriber's set and SLC-96 has normal battery feed. When a subscriber goes off-hook, the SLC-96 and the DCLU interact via a prescribed protocol as follows:

(a) The SLC-96 CU detects the change in the loop current.

(b) When a calling customer goes off-hook a single activity message identifying the calling customer is sent by the SLC-96 RT to the DCLU over the C-field of the DDL. See Table 4.

(c) The DCLU responds by assigning a time slot to the customer line via 5ESS software and the DDL C-field. See Table 5.

(d) After SLC-96 receives the assignment message, it enters a looping mode to verify transmission over the assigned DS-1 time slot. Successful results conclude the origination protocol.

2.16 Once an origination has been reported, the following occurs:

(a) Dial tone is sent from the 5ESS over the DS-1 time slot associated with the originating customer.

(b) After receiving dial tone, the originating customer inputs address digits. Dial pulse digits are encoded by SLC-96 as changes between off-hook and on-hook of the A signaling bit associated with the assigned DS-1 time slot, and dial pulsing will be received by the DCLU over this bit.

B. Call thru-put Terminating on RT

2.17 The addressing digits are interpreted by the 5ESS and the destination path is determined. For a call terminating on the SLC-96 RT, the SLC-96/DCLU interaction protocol proceeds as follows:

(a) The RT connects the DS-1 time slot assignment by means of the trunk assign DDL message from the 5ESS DCLU. See Table 3.

(b) Upon receiving the message the RT enters a PCM looping mode for the specified DS-1 time slot. Successful completion of this loop test causes the RT to cut through the called party to the assigned DS-1 time slot and to so inform the 5ESS via the DCLU.

C. Ringing and Ring Trip

2.18 Once a DS-1 time slot assignment has been made the remaining SLC-96/DCLU protocol for controlling a terminating call are as follows:

(a) The ringing cycle at the RT is controlled by alternating the A/B signaling bit patterns sent from the DCLU between the ringing and the idle patterns at the times necessary to produce the desired ringing code. The ringing generator is located at the RT. When the RT called party CU recognizes the ringing pattern (A=1,B=1/0), it responds by applying the -R ringing to the loop. See Table 2. The RT switch hook detector output becomes disabled during ringing.

(b) When the RT called party CU detects an off-hook it trips ringing. Shortly thereafter, the signaling bit pattern received by the DCLU from the CU being rung will change from on-hook to off-hook. Once this off-hook signaling bit pattern has been received by the DCLU, the ringing signaling bit pattern is no longer sent from the DCLU.

D. On-Hook and Time Slot De-assign

2.19 Call termination is detected by observing the change in A/B signaling bit pattern (from off-hook to on-hook) termination protocol proceeds as follows:

(a) Whichever party hangs up causes the customer loop current to drop below a threshold value. This alters the A and B signaling bit pattern which is sensed by the 5ESS.

(b) The on-hook signaling bit pattern (A=0,B=0) is sent from the RT to the DCLU.

(c) A trunk de-assign message is sent to the RT from the DCLU/5ESS. This message contains the DS-1 time slot number to be de-assigned and the invalid line number (Hex 63) used as the de-assign code.

DCLU MAINTENANCE

2.20 Basically, DCLU maintenance consists of monitoring the SLC-96 RT and itself. Regular self-diagnostic tests, called exercises, are performed under 5ESS software direction. In addition, any faults detected are reported via alarms.

2.21 The DCLU maintenance functions include:

(a) Monitoring by means of exercises

(b) Fault reporting by means of alarms

(c) Loop testing via metallic pair/DDL, M-field

(d) Protection line switching.

A. Derived Data Link and Self Diagnostics

2.22 The majority of SLC-96/RT maintenance information is carried as messages in the various fields of the DDL. DCLU maintenance is implemented by self-monitoring, by means of exercises provided via 5ESS software on SDFI firmware. Controlled diagnostic capabilities are also provided to further ensure correct circuit operation and to check on automatic error-detecting circuits.

2.23 Most of the maintenance messages are carried by the A, DS1 link, DDL A-field. However, other fields also perform maintenance. The DDL fields are described as follows:

(a) "C"-field (Fig. 5) provides a "no-alarm" message and the looping test message once every 2.3 seconds. If either message is not received in time, an alarm message is sent to SMPU via DCLU.

(b) DDL Alarm Data Link "A"-field Format consists of 12 or 16 consecutive DDLs and lasts 144 ms. Messages are communicated via two message bits in the "A"-field. See Fig. 5.

2.24 Alarm messages are received from or sent to the DCLU as specific values of the two alarm field bits A1 and A2 (see Table 8). These bits take the values of: "1,1" for the framing message, "0,0" for an active alarm condition, and "0,1" for an inactive alarm condition. (Only the framing, major alarm, and four shelf alarm messages are received from the RT over the DDL A-field [Table 8].)

Table 8

Alarm Data Link Format With a DCLU

Alarm Message No.	Bit A1	Bit A2	Alarm Message
1	1	1	Framing
2	0	1	Not Used
3	0	1	Not Used
4	0	1	Not Used
5	0	1 or 0	Major Alarm
6	0	1	Not Used
7	0	1	Not Used
8	0	1 or 0	A Shelf Alarm
9	0	1 or 0	B Shelf Alarm
10	0	1 or 0	C Shelf Alarm
11	0	1 or 0	D Shelf Alarm
12	0	1	Not Used
13	0	1	Not Used
14	0	1	Not Used
15	0	1	Not Used
16	0	1	Not Used

1. Bit value are as they appear on DS-1 links.

2. The alarm state is active when bit A2 is a zero.

3. The alarm messages indicated as being "Not Used" will not be received from the interface in the active state.

4. The transmittal of the active state to the interface for the messages indicated as being "Not Used" will have no effect on the RT.

2.25 The framing message allows the interfacing hardware to establish alarm data link frame.

2.26 The major alarm message indicates that a major alarm condition exists. A major alarm condition is defined as a system state characterized by a loss of service to subscribers served by a shelf of shelf group.

2.27 There are four shelf alarm messages, each corresponding to a particular shelf (A, B, C, or D) to indicate that a shelf alarm condition exists. A shelf alarm condition is defined as a system state characterized by a loss operational integrity for a shelf. When a major alarm is also present, the shelf alarm indicates the location of the major alarm fault condition.

2.28 One of the messages that can be received from the RT is the "Test Alarm RC" message in the M-field. See Figure 5. Receipt of this message indicates that channel and drop testing cannot be performed.

2.29 The DCLU diagnostics exercises each Control Mux/Data Mux group and individual SDFIs. The purpose is to determine whether a service group or a particular SDFI is faulty.

B. Maintenance Communication Protocol

2.30 Maintenance communications between the SMPU and the DCLU takes place by way of a specific protocol/data link format called PICB-A.

2.31 Thus, the SMPU can demand that an exercise be done on a certain SDFI by writing to that SDFI via the Control Mux PICB-B and receiving a reply to confirm receipt. The SDFI firmware implements the demanded exercise and writes results in registers. To these, the SMPU sends a write order to read the results; and the write reply brings back the report.

2.32 One vehicle for error reporting is the all-seems-well (ASW) field of the reply word. See Table 9. This table presents code versus error conditions being reported. Note that Order Messages signify read and write commands as well as respective replies.

Table 9

All-Seems-Well (ASW) Code/Error Assignments

ASW2	ASW1	ASW0	ERROR
0	0	0	Addressing Error
0	0	1	Parity Error on Order Message
0	1	0	All Seems Well
0	1	1	Bad start code on Order Message

C. Faults and Alarms

2.33 Various circuits throughout the DCLU monitor the T1 line input and output for faults and errors. In addition, maintenance is performed both internally and externally. Devices in the circuit packs are self checked as well as the line timing, sync, and data. Faults or errors will produce the following alarm reports to SMPU:

(a) Red Alarm - Indicates that the SDFIs cannot frame up on the incoming signal from the RT.

(b) Major Alarm - A Major Alarm will be sent if the line error rate crosses the 1E-3 threshold.

(c) Minor Alarm - A Minor Alarm will be sent if the line error rate crosses the 1E-6 threshold.

(d) Protection Switching - Fast error rate processing algorithms will send an alarm if the line error rate crosses the 1E-4, 1E-5, or 1E-6 thresholds, but only if enable by the SMPU. Also, a fast loss-of-frame indicator is provided in the 1E-4 message location.

(e) Loss-of-IPIDB-Clock Alarm - A loss of both incoming IPIDB clocks from the SMPU will result in the SDFIs automatically going into a looped state which will generate a message to the SMPU.

(f) Loss-of-DDL Alarm - If the Fs framing pattern received from the RT is lost, or if the framing pattern is continuously received without any data fields, this alarm will be sent to the SMPU.

(g) Slip counts - The total number of controlled slips is constantly monitored and reported if major or minor thresholds are crossed.

(h) Change of Frame-Alignment (COFA) counts - The total number of times the SDFIs changes frame alignment is constantly monitored and reported.

(i) Errored Seconds Alarm - A count of the number of seconds which contains one or more line errors is kept and reported if the total crosses a certain threshold.

(j) Out-of-Frame (OOF) Count - A count of the number of OOF conditions (Loss of Frame Alignment Signal [FAS]) is kept. No threshold is used.

D. Loop and Channel Unit Tests

2.34 A metallic test pair from the SLC-96 CO (or 5ESS) to RT provides metallic access to the customer loop (MC Loop Test System). Messages sent to and received from the DDL "M"-field permit metal pair-to-customer loop connection: also, they allow RT CU test.

2.35 After a series of DCLU SLC-96 RT protocol steps, CU and loop tests are performed. When all tests are completed, a disconnect signal from the MC loop testing system causes the DDL "M" field protocol to cease, unless errors or faults are detected at either the RT or DCLU. In either event, a DDL alarm message is formatted by 5ESS software.

E. Protection Switching

2.36 Protection line switching can be initiated from either the DCLU or the RT. The parameter monitored by DCLU has been mentioned and others are monitored by SLC-96. It takes 9 ms or one data link frame to transmit a protection line switching message. However, it takes three consecutive identical messages for action to be taken. A line switch takes 30 ms to complete. Protection switching is an optional feature.

3. SCHEMATIC DISCUSSION

INTRODUCTION

3.01 The descriptions that follow refer to SD-5D202-01, FS1/FS2 and BD1/BD2. The mnemonics are translated whenever they are mentioned; descriptions are to the details shown in the SD. However, for a fuller circuit pack understanding; at times, reference is made to circuit or devices details not shown. These are kept to a minimum.

POWER START PACK (CP SN346)

3.02 The SN346 is a circuit pack required for operation of the power converters that are found on each SDFI. Each SDFI contains its own power converter. The power start pack prevents the DCLU from powering up when the -48 volt supply is first applied. This is done to prevent current surges when the 5ESS is powered up. To turn on power the front switch is turned on. Once power is on, power cannot be turned off, even though circuit packs may be replaced. A red LED indicator lights up when the DCLU is shut off. One lead is distributed to the SDFI's to turn power on while one lead enters the power start pack to indicate that power is on.

3.03 Each shelf of SDFI's has its own POWER START PACK and its own -4.8 Volt feeder. See paragraph 4.05. The -48V power is available to all SDFIs, and the power start pack in service group 0 (shelf 0) by the lead identified by mnemonics -48VA and -48VARTN. See FS1 (sheet B#1AA). Service group 1 (shelf 1) is served by -48VB and -48VBRTN. See FS2 (sheet B#2AA). After the power start pack switch is depressed, the power path to all SDFIs is completed via 0START (FS1) and 1START (FS2). The SDFI power-on leads are identified as follows: 0PWRON (FS1) and 1PWRON (FS2). Successful power application causes the Power Start red LED to extinguish. Power interruption and re-application causes the red LED to re-light.

EQUALIZER CIRCUIT PACK (CP 215-219)

3.04 The equalizer is a circuit pack that ensures that the characteristics of signals between the DCLU and digital cross connect bay remain essentially unchanged. The equalizer is equipped according to the distance the DCLU is located from the digital cross connect bay. One equalizer in the DCLU provides equalization for all of the SDFIs equipped in one DCLU service group.

3.05 The equalizer CP contains 15 passive equalizers , therefore no power is required. Each DS1 signal leaving an SDFI must go through an equalizer. The length of the cable between the DSX-1 cross connect and the DCLU determines which equalizer code to use. See Table 10.

TABLE 10

EQUALIZER CODE	CABLE LENGTH (FEET)
SN215	0-133
SN216	133-267
SN217	267-400
SN218	400-533
SN219	533-655

3.06 In FS1 sheet B#1AA, the SDFI 00-09 outputs (equalizer 0T1CEQU inputs) are identified by the mnemonics 0T10N(00-09) and 0T10P(00-09) which translate as follows:

- Service Group 0, output, T1 negative for SDFIs 00 through 09, and
- Service Group 0, T1 output, positive for SDFIs 00 through 09.

The ten equalizer outputs to DSX-1 cross connect connector J2 are identified by the mnemonics 0T10R(00-09)A and 0T10T(00-09)A which translate as follows:

- Service Group 0, output ring of equalizer for DFI's 00 through 09, and
- Service Group 0, output tip of equalizer for DFI's 00 through 09.

3.07 In FS2 sheet B#2AA, the SDFI 15-24 outputs (equalizer 1T1CEQU inputs) are identified by mnemonics 1T10N(15-24) and 1T10P(15-24) which correspond to Service Group 1. The ten equalizer outputs to the DSX-1 cross connect connector J4 are identified by the mnemonics 1T10R(15-24)A and 1T10T(15-24)A which correspond to Service Group 1. Notice that for both shelves the SDFI mnemonic number is the same as the SDFI number on the DCLU e.g. 0T10P<u>08</u> and 0T10N<u>08</u> go to SDFI mnemonics 8 etc.

SDFI (CP ANN4)

3.08 In the discussion that follows reference is made to SD-5D202-01 FS1/BD1 and FS2/BD2. In referring to these documents, note that in its present configuration the DCLU makes use of 20 SDFIs rather than 30 as discussed in previous paragraphs. However, functionality is not affected.

3.09 As described in Section I 2.00 the SLC-96 output on the T1 line is a 1.544-Mb/s, bipolar bit stream. It is formatted into a 24-time slot (8-bits per time slot) channel frame which lasts 125 usec, thus recurring at an 8-KHz rate. See Fig 3.

3.10 Referring to the BD1 sheet H1, T1 data enters and leaves the DCLU by way of the DSX-1 Cross Connect Cable Connector, J1; and Equalizer, Symbol No. 2 from whence 20 lines are distributed among 10 SDFIs (symbols No 3-15). Referring to SD FS1 sheets B#1AA, #1AB and #1AE; these communication lines are identified by the mnemonics 0T10N(00-09) and 0T10P(00-09). The mnemonic translation is: shelf 0, T1 input (N lead) and (P lead) for SDFIs 00-09. The T1 input to SDFI00 is identified by mnemonics 0T1IR(00) and 0T1IT(00) which translates into: Service Group 0, input Ring (P lead) and Tip (N lead), respectively.

<u>NOTE</u>: In the subsequent discussion regarding SDFIs, reference will be made to 0SDFI00 symbol No 3 on SD Sheet B#1AA only, because all SDFIs operate identically and thier lead mnemonics are distinguished solely by the trailing numbers.

3.11 Upon entry into the SDFI the T1 data stream undergoes a format conversion so that the SDFI outputs two, 32-time slot, 4-Mb/s data streams. These are passed on to the Data Muxes via IPIDBs, one stream going to Data Mux 0 while the other going to Data Mux 1.

3.12 Referring to BD1 observe that SDFI 00 has four leads representing the IPIDB. This bus bundles with the IPIDBs from the nine other SDFIs and terminates (40 leads) on Data Mux 0. Referring to SD FS1, the IPIDB to Data Mux 0 is identified by the mnemonics:

(a) 00PBIN00 - Service Group 0, Group ODFI, Peripheral Bus Data in to Data Mux 0 -one lead

(b) 00(PB0,4MC,8KS)N00 - Service Group 0, Group ODFI, Peripheral Data Bus out of Data Mux 0, 4MHz Clock and 8KHz Sync- three leads

Note that "Group ODFI" indicates the the wires <u>do</u> <u>not</u> cross shelf (Service Group) boundaries.

3.13 Referring again to BD1 note that SDFI00 has leads representing the IPIDB 1 going to Data Mux 1 of shelf 1. Functionally these leads are identical with those of IPIDB0. On FS1, these are identified by the mnemonics:

(a) 11PBIN16 - Service Group 1, Group 1DFI, Peripheral Bus data into Data Mux 1 -one lead

(b) 11(PB1,4MC,8KS)N16 - Service Group 1 DFI, Group 1 Peripheral Data bus out of Data Mux 1, 4-MHz Clock, and 8-KHz Sync- three leads

Note that "Group 1DFI" indicates that the wires cross shelf (Service Groups) boundaries.

3.14 On BD1 notice that there are five leads connecting SDFI00 to Control Mux 0. These represent the IPICB. The five leads bundle with the IPICBs from SDFIs 00-09 to form the 50-lead bundle shown. Referring to FS1 the IPICB mnemonics are identified as follows:

(a) 00(C,OD,S)P00 - service Group 0, Side 0, burst clock, out control- data, and select control for SDFI00 - three leads

(b) 00(ID, NIT)P00 - Service Group 0, Side 0, in control-data and interrupt for SDFI00 - two leads.

Note that "Side 0" indicates that the wires do not cross shelf boundaries.

3.15 On BD1 notice that five IPICB leads also go to Control Mux 1 of shelf 1 via a 50-lead bundle. This represents the alternate bus feeding Control Mux 1 to provide uninterrupted service should shelf 0 Control Mux 0 or Data Mux 0 fail. On FS1, the mnemonics are identified as follows:

(a) 11(C,OD)P16 - Service Group 1, Side 1, burst clock and out control-data for SDFI16 - two leads

(b) 11SP16 - Service Group 1, Side 1, select for SDFI16 - one lead

(c) 11IDP16 - Service Group 1, Side 1, in control-data for SDFI16 - one lead

(d) 11NITP16 - Service Group 1, Side 1, interrupt for SDFI16 - one lead.

Note that "Side 1" indicates that the wires cross shelf boundaries.

3.16 The remaining leads are identified as follows:

(a) -48VB and -48 RTNB represent -48-volt power from power bus "B",

(b) three ground leads,

(c) 0START - signal lead from Power Start Circuit Pack that starts the Power converters in the SDFIs.

POWER UNIT (494A)

3.17 The 494A is a dc-to-dc power converter (-48 volts to +5volts) for the Control Multiplexer and the Data Multiplexer Circuit Packs. Each SDFI has its own power converter. The -48-volt power entering the 494A is identified by the mnemonics: -48VB and -48RTNB as shown on FS1 and -48VA and -48RTNA per FS2. These translate as follows: -48-volt DCLU power input bus A for shelf 0, -48 volt power bus return for bus A shelf 0; and the same for bus B of shelf 1.

3.18 The Power Unit (PU) converts -48 volts to +5 volts and distributes the latter to the Data Mux and the Control Mux. In FS1 the +5-volt power mnemonic is +5V0 signifying +5 volts power for shelf 0, while in FS2 this mnemonic is identified as +5V1 for shelf 1. In both BD1 and BD2 this is represented as POWER which is a bus to which each circuit pack connects by means of two leads. Notice in BD1 and BD2 that the power bus at the Data Mux lead is tapped by the SENSE line. This is identified by the mnemonic +5V0 in FS1 and +5V1 in FS2. This line provides a means of measuring (sensing) the voltage at the Data Mux and causing the PU to maintain correct voltage at the Data Mux via power bus +5V0 or +5V1 as applicable. This compensates for the voltage drop in the bus and leads between the PU and the Data Mux.

3.19 If either the Control Mux or Data Mux should fail, the 5ESS software determines this and illuminates a warning lamp on the PU. The software commands the Control Mux of the opposite shelf (that is the one without the failure) to act as a switch-closer to light this lamp. Thus, on BD1 the lead "to Control Mux of Shelf 1" is the switch lead, while the lead "+5V P.U.on Shelf 1" is the power lead. If any of the aforementioned CPs on shelf 1 fail, the software causes the shelf 1 Control Mux to act as a closed switch; and the +5 volts will light the lamp on shelf 0 PU. The same applies to shelf 1 PU whose switch is shelf 0 Control Mux and whose power to light its lamp comes from shelf 0 PU.

3.20 In FS1, lead identified by mnemonic 00S1, translates to "out-of-service lamp, shelf 1" and is the shelf 1 Control Mux switch lead. The lead identified by mnemonic +5V1 is the power lead from shelf 1 PU. Thus the lamp on shelf 0 PU has the capability to light. The same applies to FS2 except shelf 0 Control Mux provides switching, and shelf 0 PU provides power to light shelf 1 PU lamp.

3.21 In BD1 the 0PU leads marked PROGRAM act to tell the PU how much maximum power it should supply to the load CPs. If the max power is exceeded, the PU shuts down. In FS1 the program leads are identified by the mnemonic 0PROG(1,2) which translates to "Service Group 0, Power Unit current program resistors (1 and 2)". A resistor in each CP acts as a programmable current threshold which causes 5ESS software to shut down the PU, if excessive current flows. On FS2, the same discussion applies to its PU and the mnemonic is 1PROG(1,2).

DATA MUX (UN121)

3.22 On shelf 0 Data Mux 0 provides concentration for all SDFIs. Each SDFI connects to the Data Mux 0 via four leads which go to make up the two, 40-lead bundles going to Data Mux 0, shelf 0. The 54-lead bundle between Data Mux 0 and Control Mux 0 represents the necessary control interface. The POWER, SENSE and PROGRAM leads have been discussed in paragraphs 3.18 through 3.21.

3.23 Under normal conditions the SDFIs 00-09, 32-time slot, 4 Mb/s outputs are sent to both Data Muxes. See FS1 (sheet B#1AD). At the same time, Data Mux 0 outputs go to all SDFIs as shown. The mnemonics involved are: 00PBIN 00-09 for shelf 0 SDFIs and 00PBIN 16-25 for shelf 1 SDFIs. Each lead comprises one of the four IPIDB leads interconnecting each SDFI to Data Mux 0.

3.24 The other three IPIDB leads are identified as follows:

(a) From shelf 0: 00(PB0, 4MC, 8KS)N,00-09 - three leads,

(b) From shelf 1: 00(PB0, 4MC, 8KS)N,16-25 - three leads.

See section II 3.12 and 3.13.

3.25 The Control Mux 0 sends the Data Mux 0 a seven-bit data word which assigns an SDFI to a time slot. The leads implementing this are identified as follows:

(a) Transmit: AXMXCT(0-5) and AXMXCTP which translate into PIDB-A transmit Mux control bits 0-5 (bits 0-4 give the SDFI address and bit 5 indicates active or idle state of the time slot); bit 6(P) gives even parity to protect control leads - seven leads.

(b) Receive: ARMXCT(0-5) and ARMXCTP which translate the same as that for transmit except they apply to the receive direction - seven leads.

The PIDB-B leads are functionally identical and are as follows: BXMCT(0-5), BXMCTP, BRMXCT(0-5), and BRMXCTP.

3.26 The Control Mux 0 receives a 16-bit word via PICB-A from SMPU and 5ESS software to assign a given SDFI to a particular time slot. This information is communicated to the Data Mux 0 via the 54-lead bundle discussed, and it is updated at a 256KHz/s rate. See 0256CK1 on FS1 (sheet B#1AC). Serial data transfer is clocked at 4MHz/s. See 04MCLK on FS1 (sheet B#1AC).

3.27 Table 11 identifies the leads which provide Data Mux 0 control for read, write, sync and clocking as well as maintenance. The table applies to Data Mux 1 except that Service Group 0 becomes 1.

TABLE 11

Data Mux 0 Control and Maintenance Mnemonics Identity

Mnemonic	Identification
ORAMSYNC Mux 0 Ram refresh	Service Group 0 synchronizes Control
ORDPULSE parity checker	Service Group 0 Command to read
ORDDATA 32X8 Control Mux 0 RAM	Service Group 0 Command to read
OWRPULSE distribute order	Service Group 0 Command to write word to Data Mux 0
OWRPULSE command	Service Group 0 Prepare distribute
OSIDESEL Data Mux 0	Service Group 0 Command to select
OPIDBSEL PIDB-B from Mux 0 or 1	Service Group 0 Selects PIDB-A or Data
ODESTA maintenance	Service Group 0 Address select for
ODSTRST reset	Service Group 0 Addressed register
OA ADRPER parity error	Service Group 0 PIDB-A address
OASW	Service Group 0 All seems well maintenance
ODFILP command	Service Group 0 PCM(SDFI) Loop back
OCLEAR	Service Group 0 in Clears parity Check device in Data Mux 0

3.28 On FS1 (sheet B#1AD) the leads going to and coming from the CONN CKT comprise the four PIDBs interconnecting Data Mux 0 to the 5ESS TSIU side 0. Each PIDB comprises four leads and is identified by the following generalized mnemonics:

(a) (00,01) (A,B) PBON - 32-time slot, 4Mb/s data out negative lead

(b) (00,01) (A,B) PBOP - 32-time slot, 4Mb/s data out positive lead

(c) (00,01) (A,B) 4MCN - 4 MHz clock negative lead

(d) (00,01) (A,B) 4MCP - 4 MHz clock positive lead

(e) (00,01) (A,B) 8KSN - 8KHz sync negative lead

(f) (00,01) (A,B) 8KSP - 8KHz sync positive lead

(g) (00,01) (A,B) PBIN - 32-time slot, 4Mb/s data in negative lead

(h) (00,01) (A,B) PBIP - 32-time slot 4Mb/s data in positive lead.

The four Data Mux 0 PIDBs are identified as follows:

(a) PIDB-A0: 00APBIP,00APBIN, 00APBON, 00APBOP, 00A4MCN, 00A4MCP, 00A8KSN 00A8KSP

(b) PIDB-B0: 00BPBIP, 00BPBIN, 00BPBON, 00BPBOP, 00B4MCP, 00B4MCN, 00B8KSN 00B8KSP

(c) PIDB-A1: 01APBIP, 01APBIN, 01APBOP, 01APBON, 01A4MCN, 01A4MCP, 01A8KSN, 01A8KSP

(d) PIDB-B1: 01BPBIP, 01BPBIN, 01BPBON, 01BPBOP, 01B4MCN, 01B4MCP, 01B8KSN, 01B8KSP.

Those leads going to make up Data Mux 1 PIDBs have the same mnemonics except that they are preceded by Service Group 1 rather than 0 (ie, 10,11 vs 00,01)

3.29 The remaining Data Mux 0 leads are those going to and coming from the Digital Carrier Line Unit Supplement Circuit as well as various grounds. See FS1 (sheet B#1AC). The supplement circuit connections are not active in the present configuration but allow for expansion to 30 DFIs (ie, CPs 10-14 and 25-29). The mnemonics have the same function as those mentioned in Section II 3.24 and 3.25. Notice, however that the mnemonic numbers going to SDFI, 25-29 are one higher e.g., 01SP26 goes to SDFI 25. Likewise, Data Mux 1 connections and mnemonics are defined the same as for Data Mux 0.

CONTROL MUX (UN 120)

3.30 On shelf 0 Control Mux 0 provides the required concentration control and maintenance control for Data Mux 0 and SDFIs 00-09. See BD1. The SDFIs connect to the Control Mux 0 via five leads each which form the 50-lead bundle shown. Each 5-lead connection represents an IPICB as described in Section II 1.32. Besides these SDFIs, Control Mux 0 provides control for SDFIs 14-25 via 5-lead IPICBs forming the 50-lead bundle coming from shelf 1. See BD1. The OOS, POWER and PROGRAM leads have been discussed in Section II 3.18 and 3.21.

3.31 On FS1, sheet B#1AC a typical 5-lead IPICB is identified by the following generalized mnemonics:

(a) 00(ID,NINT)N/P 00-09 - Service Group 0 Side 0, control data in from SDFIs 00-09, and interrupt - 2 leads

(b) 00(C,OD,S)N/P 00-09 - Service Group 0, side 0, control data out to SDFIs 00-09, burst clock,select - 3 leads.

Note that Side 0 indicates that the leads do not cross shelf boundaries.

On FS1, sheet B#1AC the typical 5-lead IPICB feeding side 1 is given by the following generalized mnemonics:

(a) 01IDP 16-25 - Service Group 0, Side 1, control data in from SDFIs 15-24 - 1 lead

(b) 01NITP 16-25 - Service Group 0, Side 1, SDFI 15-24 interrupt - 1 lead

(c) 01(C, OD)P 16-25 - Service Group 0, Side 1, burst clock and control data out to SDFI 15-24 - 2 leads

(d) 01SP 16-25 - Service Group 0, Side 1, select to SDFIs 15-24 - 1 lead.

Note that Side 1 indicates that the leads do cross shelf boundaries. Also note that mnemonic numbers are one higher than SDFI numbers.

3.32 Data Mux 0 control is effected via the 54-lead bundle shown on BD1. On FS1 these leads comprise the bundles (bracketed) shown going to 1/10. See Section II 3.26, 3.27 and Table 11 for the identification of each lead.

3.33 As discussed in Section II 3.29 the DCLU Supplement Circuit provides for expansion to ten more SDFIs. The generalized IPICBs are identified as follows:

(a) 00IDP 10-14 - Service Group 0, Side 0, control data in from SDFIs 10-14 - 5 leads one each per SDFI

(b) 00NITP 10-14 - Service Group 0, Side 0 interrupt - 5-leads one each per SDFI

(c) 00(C, OD, S)P 10-14 - Service Group 0, Side 0, burst clock, control data out to SDFs 10-14, select - 15 leads 3 each per SDFI

(d) 01IDP 26-30 - Service Group 0, Side 1, control data in from SDFIs 25-29 - 5 leads one per each SDFI

(e) 01NITP 26-30 - Service Group 0, Side 1, SDFIs 25-29 interrupt - 5 leads one each per SDFI

(f) 01(C, OD, S) 26-30 - Service Group 0, Side 1, burst clock, control data out to SDFIs 25-29, select - 15 leads three each per SDFI.

The preceding discussion applies to Control Mux 1 shown on FS2, sheet B#2AC, except Service Group 0 becomes 1.

3.34 The interface between the Control Mux and SMPU is effected by PICBs. Control Mux 0 connects to SMPU 1 via PICB-A0, PICB-A1, PICB-B0 and PICB-B1. All interconnects pass through CONN CKT as shown in FS1. Each PICB comprises five leads. The PICB-A0 mnemonics are identified as follows:

(a) 00ACN - Service Group 0, Side 0, A-bus, burst clock negative - one lead

(b) 00ACP - Service Group 0, Side 0, A-bus, burst clock positive - one lead

(c) 00AODN - Service Group 0, Side 0, A-bus, control data out negative - one lead

(d) 00AODP - Service Group 0, Side 0, A-bus, control data out positive - one lead

(e) 00ASN - Service Group 0, Side 0, A-bus, select negative - one lead

(f) 00ASP - Service Group 0, Side 0, A-bus, select positive - one lead

(g) 00AIDN - Service Group 0, Side 0, A-bus, control data in negative - one lead

(h) 00AIDP - Service Group 0, Side 0, A-bus, control data in positive - one lead

(i) 00ANINTN - Service Group 0, Side 0, A-bus, interrupt negative - one lead

(j) 00ANINTP - Service Group 0, Side 0, A-bus, interrupt positive - one lead

The PICB-A1 leads are identically defined except that side 0 becomes 1. Thus, for example, 00ACN becomes 01ACN, etc. The PICB-B0 leads are identically defined except that all A-bus references are replaced by B-bus mnemonics. Thus 00ACN becomes 00BCN, etc. In the PICB-B1 case side 0 becomes side 1 and 00BCN becomes 01BCN.

3.35 On FS2 the PICBs are identical with those just discussed except that Service Group 0 becomes 1. Thus in the case of PICB-A0 the mnemonic for burst clock is 10ACN vs 00ACN; and for PICB-A1, the mnemonic is 11ACN vs 01 ACN. For PICB-B0 the mnemonic is 10BCN vs 00BCN; and for PICB-B1 it is 11BCN vs 01BCN, etc.

PIDB AND IPIDB TIMING

3.36 The leads and their corresponding signals for PIDBs and IPIDBs have been discussed. Figure 6 illustrates the relative timing of the bus signals. Going from the 5ESS TSIU to the DCLU, the 8KHz sync is sent via the PIDB. The DCLU responds by starting a new 32-time slot frame (ie, TS0) as shown. The 4-MHz clock coming from TSIU via the PIDB defines the 16 bits per time slot (ie, bits 0-15) which communicate data from DCLU to TSIU. Simultaneously built into the system timing, the last half of time slot 29 (TS29) is fed into the DCLU from the TSIU, as shown.

Note: Because of the way that the incoming and the outgoing data is aligned on the PIDB a 28-time slot delay is needed between the parity detect circuit and the parity generate circuit to ensure that the detected parity sense is sent back out on the same time slot during the next frame.

3.37 The IPIDB timing relationships are quite similar to those of the PIDB. Going from 5ESS TSIU to DCLU, the 8KHz sync pulse is passed on to a Sync Generator in the Data Mux where an approximately four-bit delay between SDFI sync and Data Mux sync occurs as shown in Fig 6. This compensates for data passage time through the Data Mux. The 4-MHz clock derived from that of the PIDB serves the same purpose as described, and there is a 28-time slot alignment difference between in-data and out-data signals.

PICB AND IPICB TIMING

3.38 The PICB provides scan and distribute order/reply messages between SMPU/TSIU and Control Mux. Each message has a particular format established by the 2-MHz clock, and data is conveyed back and forth, as required. Scan orders are read orders, while distribute orders are write orders. Both originate from 5ESS software via the SMPU interface. Scan messages formats are illustrated in Fig 7, and distribute messages formats are shown in Fig 8. Timing relationships for scan and distribute messages are shown in Fig 9 and 10 respectively. Timing on the IPICBs is identical with that on the PICBs. The difference lies in the interfacing which for the IPICBs takes place between Control Mux and SDFIs.

4. HARDWARE DESCRIPTION

CABINET, SHELVES AND CONNECTIONS

4.01 The DCLU is equipped with BELLPAC hardware arranged for mounting in the 5ESS cabinet which has forced air flow for cooling. The cabinet width is 25-15/16 inches which is the same as a standard frame, and the depth is 21 inches. The circuit packs are mounted in the BELLPAC 132B apparatus housing, 8-1/2 inches high by 14-3/8 inches deep, which has no vertical supports across the front of the shelf; therefore providing maximum space. Due to the large number of connections required, the 300-pin, 963L connector is used for the Data and Control Muxes.

4.02 Figure 11, shelves J5D003AR, layout shows that the present configuration accommodates 20 SDFIs circuit packs. The DCLU can grow easily up to 30 SDFI circuit packs with the addition of the third shelf, J5D003AS at the top as shown. This additional shelf has the same arrangement as the other two shelves, except it has no MUX circuit packs or power unit. This shelf is connected to the lower two shelves with paddleboard connectors via the supplement circuits from the Control and Data MUXs.

4.03 To prevent the forced air from escaping through the front of the circuit pack mountings, end fillers are provided as shown. In addition each plug-in has an air flow restrictive faceplate.

4.04 Connections for the PIDB and PICB busses from the respective MUX circuit packs to the SMPU/TSIU interfaces are effected on 982 type paddleboard connectors. The input and output T1 connections to/from the SDFIs to the DSX-1 are on separate 12-pair 607B shielded cables which terminate on two separate microribbon connectors mounted at the rear of the DCLU shelf. In Fig 11 the shelf equipment locations (EQL) and slot positions are given as well as the 963 connection for each circuit pack.

POWER AND FUSING

4.05 Two pairs of feeders for -48V to the DCLU originate at the fuse panel located near the base of the cabinet and terminate on lugs mounted on the backplane. These lugs provide input to the 494L power units and to the power circuit on each SDFI circuit pack on the third shelf. One -48V pair designated "A" feeds the bottom shelf, and the second -48V pair, designated "B", feeds the second shelf. The third shelf has both A and B feeders. Each supplies power for five SDFI circuit packs on the third shelf.

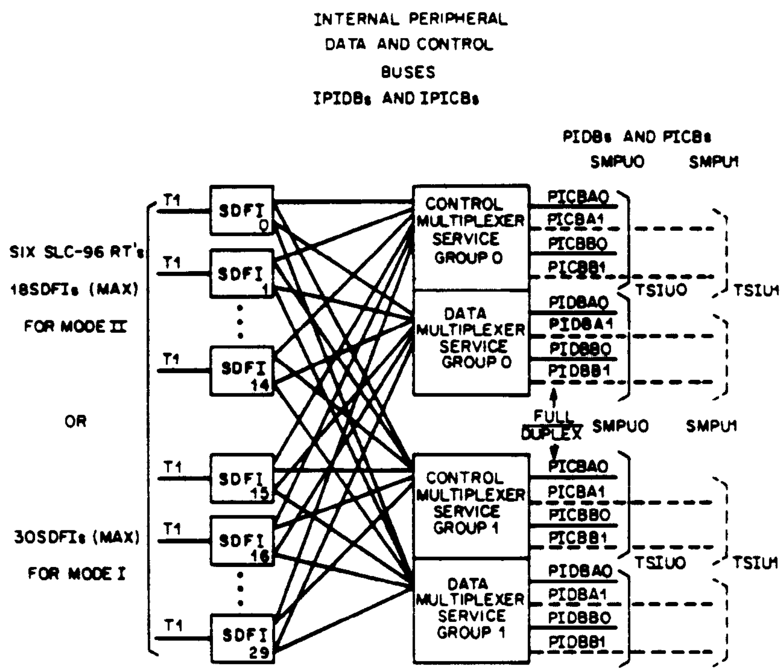
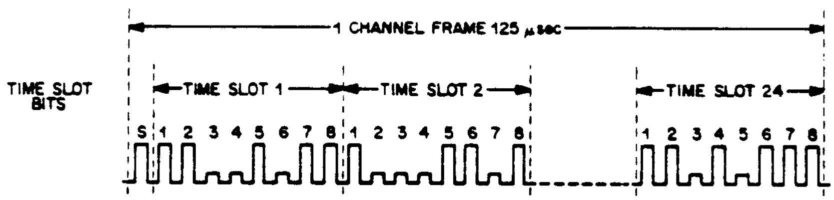


Figure 2 Digital Carrier Line Unit (DCLU) Block Diagram



SAMPLING FREQUENCY	8000 HERTZ
OUTPUT BIT RATE	1.544 Mb PER SECOND
BITS/CHANNEL FRAME	193
TIME SLOTS/CHANNEL FRAME	24
SIGNALING	EIGHTH BIT EVERY SIXTH FRAME AS SHOWN IN TABLE 1.

THE FRAMING BIT (S) IS TIME-SHARED BETWEEN CHANNEL FRAMING (F_T) BIT AND SIGNALING FRAMING (F_S) BIT AS SHOWN IN TABLE 1

Figure 3 SLC-96 Channel Frame Format

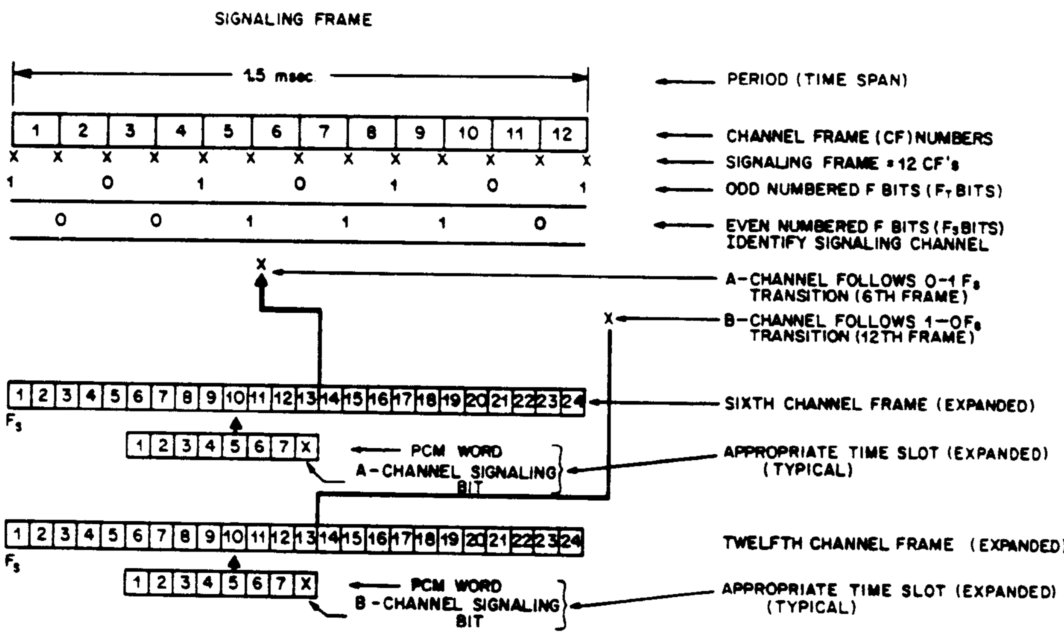
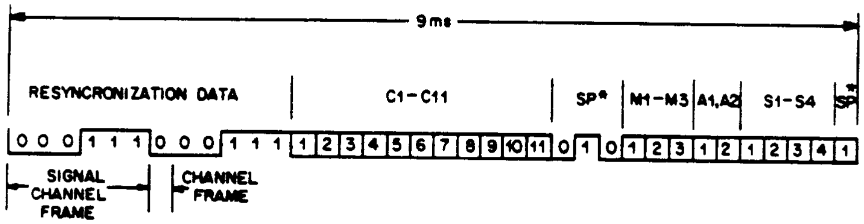


Figure 4 Signaling Frame Format



DATA LINK A

NOTES:

1. THIS FIGURE DEPICTS F_s BITS AS SEEN ON THE DSI LINK, WITH TIME INCREASING LEFT TO RIGHT.
2. C1-C11 ARE CONCENTRATOR FIELD BITS.
3. M1-M3 ARE MAINTENANCE FIELD BITS.
4. A1,A2 ARE ALARM FIELD BITS.
5. S1-S4 ARE LINE SWITCH FIELD BITS.
6. DATA LINK C IS IDENTICAL IN FORMAT TO DATA LINK A AND IS TRANSMITTED WITH THE PCM FROM SHELF C. ON DATA LINK C. THE MAINTENANCE, ALARM, AND LINE SWITCH DATA FIELDS ARE NOT USED.

* SPOILER BITS.

Figure 5 Data Link Frame

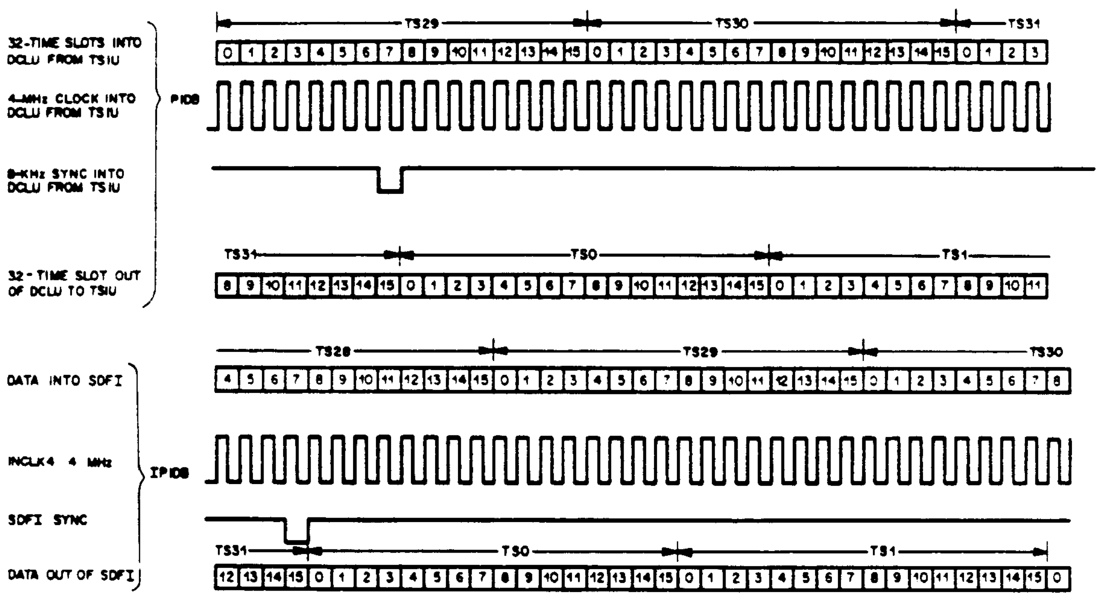


Figure 6 PIDB and IPIDB Timing

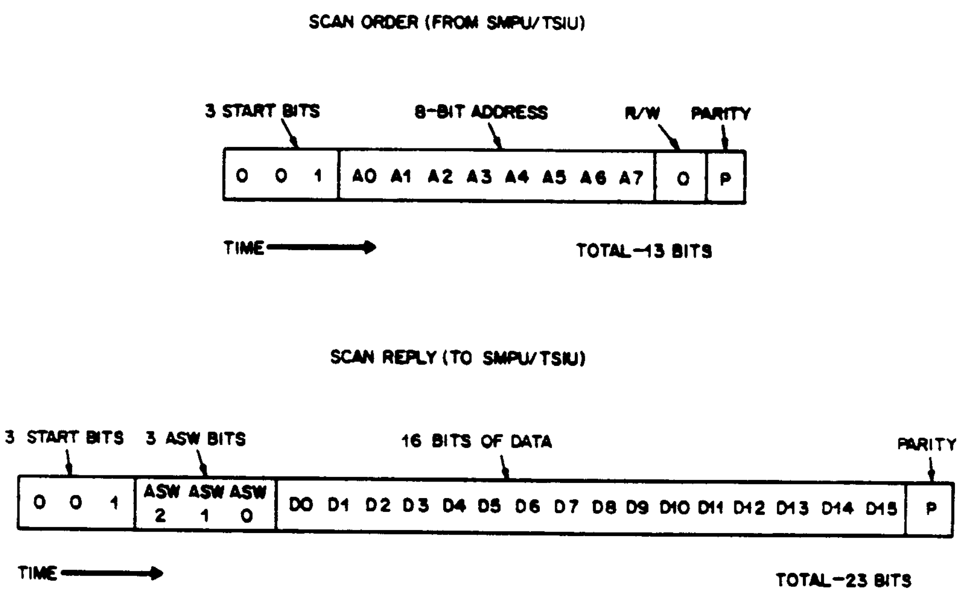


Figure 7 Scan Message Formats

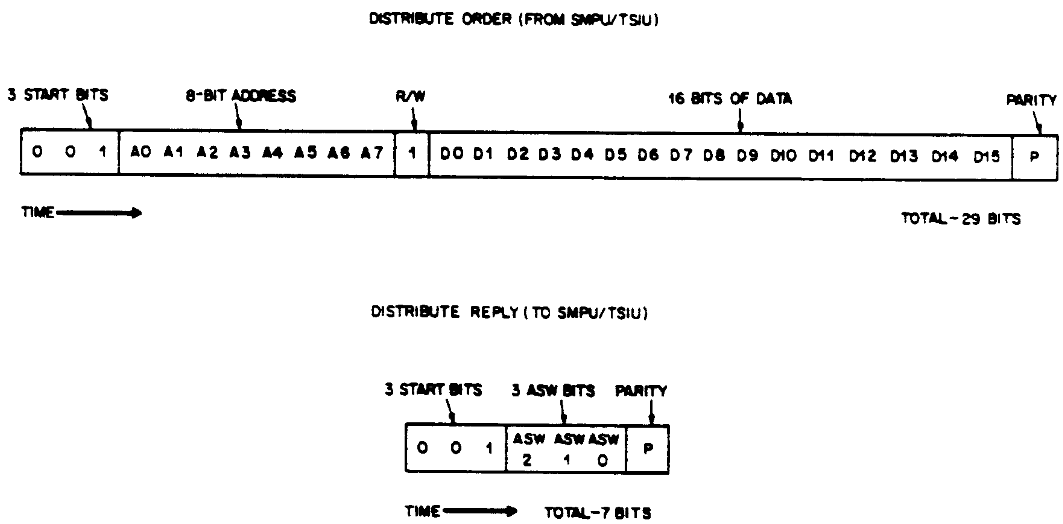
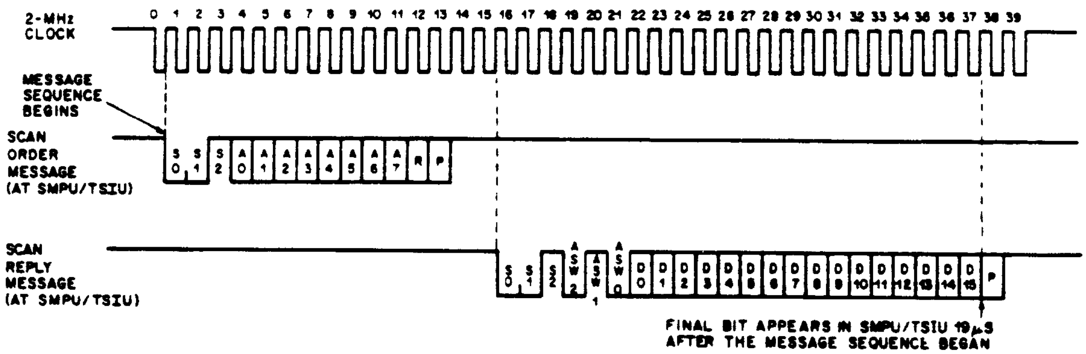
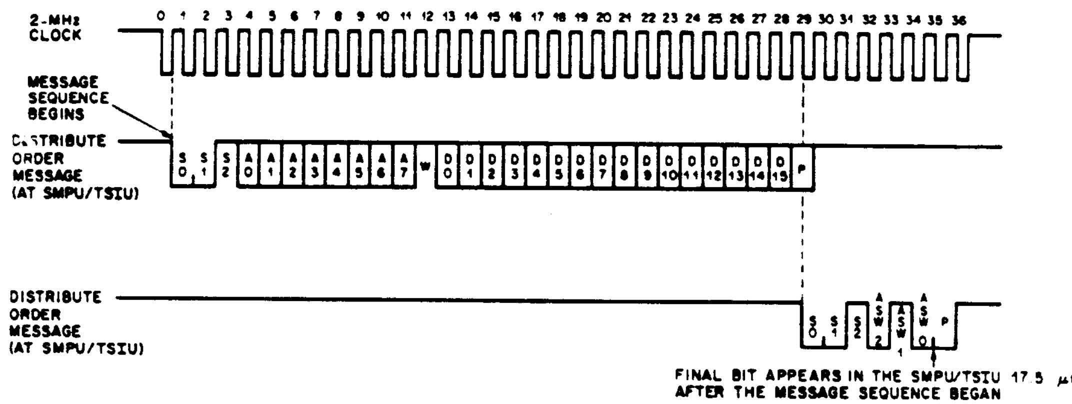


Figure 6 Distribute Message Formats



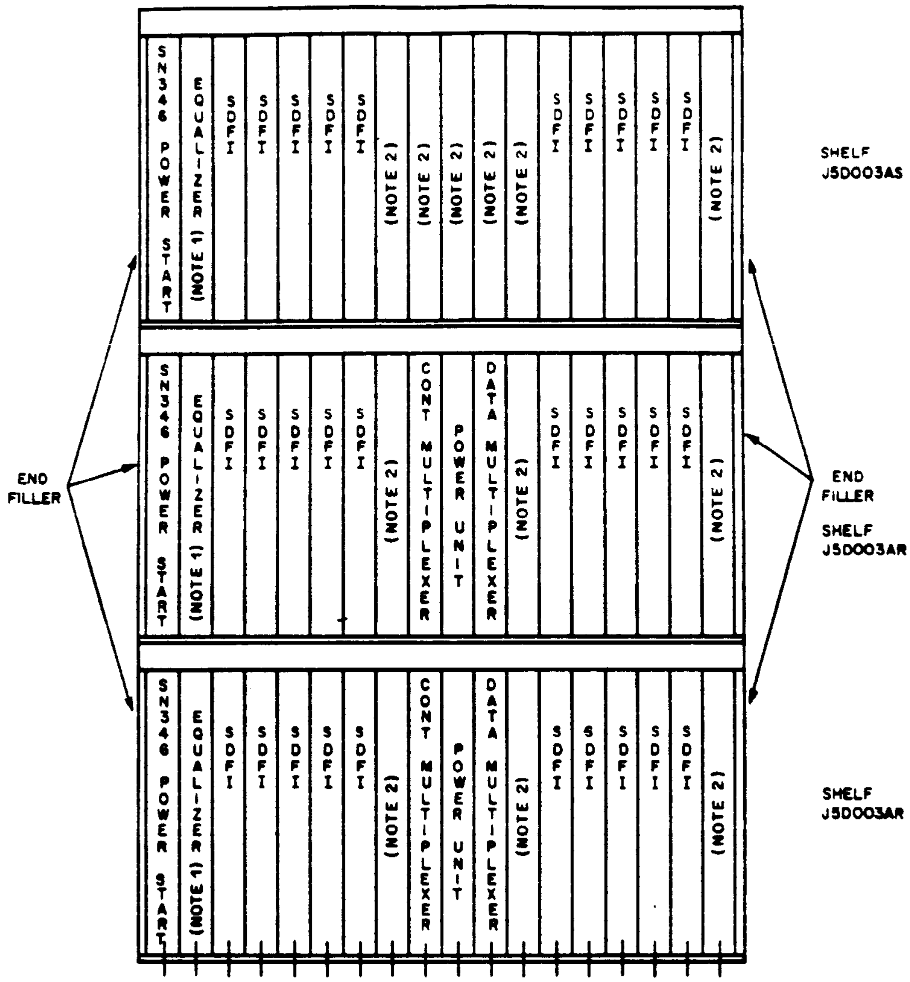
NOTE: ASW SHOWN FOR "NO ERRORS"

Figure 9 PICB/IPICB Scan Messages Timing



NOTE: ASW AND P SHOWN FOR "NO ERRORS"

Figure 10 PICB/IPICB Distribute Messages Timing



EQL	010	018	027	037	047	057	067	-	088	098	108	-	129	139	149	159	169	-
SLOT	3	7	12	17	22	27	32	37	42	47	52	58	63	68	73	78	83	88
963 CONN	G	G	M	M	M	M	M	–	L	G	L	–	M	M	M	M	M	–

NOTES:

1. THE EQUALIZER CIRCUIT PACK CODE IS SELECTED ACCORDING TO THE DISTANCE THE DIGITAL FACILITY INTERFACES MOUNTED IN THE DCLU OF THE LINE TRUNK PERIPHERAL FRAME IS LOCATED FROM THE DIGITAL CROSS-CONNECT BAY. TABLE 10 LISTS THE DISTANCES AND DIFFERENT CIRCUIT PACK NUMBERS.
2. COVER PLATE.

Figure 11 Digital Carrier Line Unit Shelf Layout

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The DCLU has a component operating temperature range of 0 to 70°C.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packs

Designation	Meaning
(none)	Equalizer Pack
(none)	Power Start Pack
(none)	Power Unit
SDFI or DFI	SLC-96 Digital Facility Interface or Digital Facility Interface
Data Mux	Data Multiplexer
Control Mux	Control Multiplexer

2.02 Interface Cables

Designation	Meaning
PIDB	Peripheral Interface Data Bus
PICB	Peripheral Interface Control Bus
IPIDB	Internal Peripheral Interface Data Bus
IPICB	Internal Peripheral Interface Control Bus

2.03 Indicators:

Designation	Meaning
OOS	Out of service lamp

2.04 Circuits:

Designation	Meaning
DCLU Supp	DCLU Supplement Circuit (third shelf option)

3. FUNCTIONS

3.01 The primary DCLU functions are:

(a) To frame on incoming SLC-96, T1 facility and synchronize to 5ESS system timing,

(b) To provide concentration at 5ESS for SLC-96 RTs,

(c) To convert from T1 format to PIDB format,

(d) To generate framing information on outgoing T1 facility,

(e) To monitor T1 facility and report problems to 5ESS SMPU,

(f) To monitor itself and report problems to 5ESS SMPU,

(g) To provide control concentration.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) The T1 facility interfaces with the DSX1 cross connecting bay, SD-99503-01.

(b) The PIDB interfaces to the 5ESS data interface, (DI) circuit pack (CPS 836, CPS 837) which is part of the 5ESS switching module's TSIU (SD5D045-01).

(c) The PICB interfaces to the 5ESS control interface (CI) circuit pack, CPS TN 876 which is part of the 5ESS switching module MP (SD5D040-02).

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are contained in the following X-specifications:

(a) X-19829: Line Equalizer Circuit Pack, CPS SN215-219

(b) X-18928: Power start Pack, CPS SN346

(c) X-19300: SLC-96 Digital Facility Interface for RT application CPS ANN4.

SECTION IV - REASONS FOR REISSUE

A. Changed and Added Functions

A1. Added

Section II - Detailed Description and Section III - Reference Data.

AT&T BELL LABORATORIES

DEPT 54313-JK-JCB