5ESS® SWITCHING EQUIPMENT
IDCU
INTEGRATED DIGITAL CARRIER UNIT CIRCUIT

D. Description of Changes

The following changes are documentation corrections or clarification of the existing design.

MNEMONICS INDEX updated to include the following designation and definition:

[0:1]T1[I:O][T:R][0:19]	ELI 0 OR 1, T1, IN OR OUT, TIP OR RING, FOR LINES 0 TO 19

FS 3, added note under title "ELI_0 IS NOT ASSOCIATED WITH SIDE 0". Functional Designations on Symbol No. 4, 5 and 6, changed to "0LSI_0", "0LSI_1" and "ELI_0" respectively.

FS 6, added note under title "ELI_1 IS NOT ASSOCIATED WITH SIDE 1". Functional Designations on Symbol No. 8, 9 and 7, changed to "1LSI_0", "1LSI_1" and "ELI_1" respectively.

Circuit Note 102 changed ELI_A and ELI_B to ELI_0 and ELI_1, respectively.

Circuit Note 103 added:

"ELI_0 is not associated with Side 0.
ELI_1 is not associated with Side 1."

Circuit Note 105 deleted. Information did not pertain to production hardware.

Equipment Note 207 changed to correct description information and documentation error of cabling for the IDCU. The correct information is as follows:

BACKPLANE WIRING SIDE CONNECTORS ON IDCU SHELF					
FUNCTION	TO/FROM	DESCRIPTION	EQL/TERM	SIZE	ID
DS1 CABLE "IN - A"	DSX-1 "IN"	T1IT,R[10,19] T1IT,R[0,9]	04-085-145 04-085-132	2X12 2X12	DS DT
DS1 CABLE "OUT - A"	DSX-1 "OUT"	T1OT,R[10,19] T1OT,R[0,9]	04-085-113 04-085-100	2X12 2X12	DU DV
DS1 CABLE "IN - B"	DSX-1 "IN"	T1IT,R[10,19] T1IT,R[0,9]	04-097-145 04-097-132	2X12 2X12	DW DX
DS1 CABLE "OUT - B"	DSX-1 "OUT"	T1OT,R[10,19] T1OT,R[0,9]	04-097-113 04-097-100	2X12 2X12	DY DZ

Information Note 307 reworded to the following:

"AT&T 1249C TYPE CABLE IS RECOMMENDED FOR T1 OFFICE CABLING, EXCEPT WHEN THE LENGTH EXCEEDS 450 FEET, WHEN THE 600 TYPE CABLE MUST BE USED."

AT&T BELL LABORATORIES

DEPT NA5340100-SMW-CHS

5ESS® SWITCHING EQUIPMENT
IDCU
INTEGRATED DIGITAL
CARRIER UNIT
CIRCUIT

CONTENTS

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The Integrated Digital Carrier Unit (IDCU) feature of the 5ESS® Switch digitally connects to the Subscriber Loop Carrier (SLC) system without the need for associated Central Office Terminals (COT). This new circuit maintains low Plain Old Telephone Service (POTS) cost, supports an Integrated Services Digital Network (ISDN) interface through a remote terminal, and implements a new generic interface to remote digital terminals.

The IDCU interfaces to the same types of remote terminals as the Digital Carrier Line Unit (DCLU). This interface is specified in Bellcore TR008[1] , and is implemented by SLC® Series 5 and SLC® 96 remote terminals. Both nonconcentrated and concentrated modes are supported. The IDCU performs all the applications of the DCLU it replaces.

The IDCU fulfills the requirements explained in a new Bellcore publication, TR303[2] , that specifies a generic interface between remote digital terminals and local digital switches. This generic interface enables operating companies to mix equipment from different vendors. AT&T has produced an interface specification[3] that explains in detail how the IDCU and the generic software conform to the specifications of the Bellcore TR303 document.

The IDCU also supports general DS1 interfaces, as described in PUB43801[4] which are associated with DS1 facilities terminating on D4 and D5 channel banks, and on Digital Access and Cross connect System (DACS) frames.

1.2 GENERAL DESCRIPTION OF OPERATION

HARDWARE CONFIGURATION

See the block diagram BD1 in the companion SD-5D301-01, sheet H1. The IDCU is a one-shelf system that accepts up to forty DS1s and converts them to Peripheral Interface Data Buses (PIDBs) when connecting to a Switching Module (SM), or converts them to Directly-connected Peripheral Interface Data Buses (DPIDBs) when connecting to a Packet Switch Unit (PSU).

Depending on the engineered traffic load and application, two switch-side interface configurations are possible:

- A voice-traffic application can have up to sixteen PIDBs and seven DPIDBs.
- An ISDN-heavy application can have up to eleven DPIDBs with eight PIDBs.

Note: present SMs can have only sixteen PIDBs. Next generation SMs may accept more.

Two PICBs, one to each active side, are required for the IDCU. Two power feeds of office -48 volt battery are required, one from each bus.

The shelf consists of a duplicated architecture of two sides ("0" and "1"). One side is active and the other is standby, with a non-duplicated set of two common packs. Each side is a distinct service group and consists of:

- one or two Loop Side Interface (LSI) (TN1670) circuit packs,
- a PIDB Termination Interface (PTI) (KBN6) pack,

- a Common Control Processor (CCP) (UN359) pack, and
- a Power Converter with Display and Control (PCDC) (429AA) pack.

In addition, there are one or two Electrical Line Interface (ELI) (KBN7) packs, which are common to both service groups, are not duplicated, and are always active.

EQUIPAGE

The IDCU can have three circuit pack configurations, one for each of the following applications:

- a forty-DS1 equipage,
- a twenty DS1 equipage with typical PIDB use, or
- a twenty-DS1 equipage with high PIDB use.

The forty-DS1 equipage has all slots filled with circuit packs, and both the active and standby side are equipped. The two LSI packs in each side, 0 and 1, are logically arranged as two groups of 20 DS1s each: group A and group B. One ELI pack in the A group connects to one A-group LSI in side 0 and one A-group LSI in side 1. The other ELI pack, in the B group, connects to one B-group LSI in side 0 and one B-group LSI in side 1.

The typical twenty-DS1 equipage eliminates the two B-group LSI packs, one from side 0 and one from side 1. The ELI pack associated with the B-group is also deleted. The PIDB ports used in this configuration are numbered from Port 0 up to the maximum of Port 8.

The twenty-DS1 equipage with high PIDB use also eliminates the two B-group LSI packs, one each from side 0 and 1, but the ELI pack associated with the B-group remains. Under unusual engineering applications, where the IDCU is used for many trunking applications of PUB43801 and few remote terminals are connected, the traffic from the DS1s is not concentrated and passes directly onto the PIDBs. In particular, the second ELI is always required when PIDB Port 9 or higher is used.

The signal flow within the IDCU consists of "data" (voice traffic, ISDN signals, and DS1 related information) and "control" (IDCU administration commands from the Switch).

GENERAL DATA SIGNAL FLOW

The "data" signal flow comprises the handling of voice and data traffic from the DS1 facilities into the Switching Module (SM). The functions of traffic flowing in the reverse direction are similar and will be explained in the "Detailed Description" section.

All circuit packs are duplicated (active/standby) except for the ELI. A DS1 signal (1.544 Mbits/sec) enters the ELI and is passively split into two signals, one sent to the LSI on side 0 and the other sent to the LSI on side 1. One LSI will be in the active service group, the other in the standby service group.

The LSI pack terminates up to twenty DS1 signals, recovers the 1.544 MHz line clock, checks for proper framing format, and extracts calling information from the embedded data link in the DS1 format. The calling information is gathered by circuitry within the LSI and made available to the CCP. Continuous voice and ISDN traffic is bundled and sent on to the PTI pack.

The PTI pack receives the traffic from the LSI, looks for particular signaling patterns, and uses an internal Time Slot Interchange (TSI) to bundle the traffic into PIDBs and DPIDBs to the SM, or back out to the LSI in a hairpin arrangement. The PTI pack also generates timing and synchronization signals for its side.

GENERAL CONTROL SIGNAL FLOW

The control for the IDCU originates in the SM and enters the IDCU over a standard PICB interface through a pin field to the CCP pack.

The CCP contains a microprocessor, RAM, and EPROM that locally run software to control the IDCU. Each CCP can communicate over an internal update bus to the companion CCP in the opposite side, which allows rapid maintenance switching between the active and standby side. The CCP has a parallel bus interface to the PTI pack for control and monitoring of PTI and LSI functions.

The PTI has an internal EPROM to load in configuration data autonomously at power up. This control program sets up the logic in several Field Programmable Gate Arrays (FPGAs) to form functions such as parity generators and detectors, timing controls, and error/control registers. The PTI also formats control information from the CCP to the LSI.

Each LSI pack in a service group receives control information from the CCP through the PTI over a PICB-like path. One main processor does general housekeeping for all of the LSI, twenty-DS1 facilities, while two slave processors each handle data link traffic for ten DSIs. Commands are received from the CCP and results are sent back to the CCP through the PTI.

GENERAL POWER DISTRIBUTION

Each PCDC accepts standard office battery -48 volt power and converts it to 5 volts for distribution to the PTI, CCP, and LSI packs on its side. The ELI packs are purely passive, containing only resistors, transformers, and choke filters, so no supply voltages are used on that pack.

FRONT ACCESS OPERATIONS

There are only a few controls and indicators accessed from the front of the IDCU shelf, all of which are contained on the PCDC's faceplate. These show the power state and service status of each side. For more information, see the PCDC detailed description below.

There are no option switches or manual settings on any of the IDCU packs. Except for the few power controls on the PCDC faceplate, all control is accessed through software at the regular Switch maintenance console.

2. DETAILED DESCRIPTION

2.1 ELI CIRCUIT PACK

Each ELI splits the received DS1 signals, dual-feeds the Side 0 and Side 1 LSI packs of its A or B group, and combines the signals from the active side LSI. The mate side LSI of its group does not generate any DS1 signals until it switches roles and becomes the active side. The ELI packs are not duplicated because they contain only passive components, and therefore have a sufficiently-low failure rate. A single fault affects only one DS1 out of a service group of twenty DS1s.

The ELI provides the interface between the IDCU and the facility, and, because of PTI pack pin limitations, terminates the PIDBs' 8 kHz Clock and Sync differential signals from the SM. Since all PIDBs from the SM are synchronous, the PTI only needs the Clock and Sync signals for PIDB Port 0. The clock and sync signals for PIDB Ports 1 through 8 are terminated on the A-group ELI, and the clock and sync signals for PIDB Ports 9 through 15 are terminated on the B-group ELI. These clock and sync terminations minimize spurious radiating noise, which can contribute to Electro-Magnetic Compatibility (EMC) generation, as defined in FCC Rules Part 15.

All DPIDB signals are terminated within the PTI pack. Choke filters in the ELI on the DS1 signal paths also reduce spurious, conducted noise emission.

2.2 LSI CIRCUIT PACK

The Loop Side Interface (LSI) performs framing on each of the DS1s and converts the data to an Internal Data Base (IDB) format on the internal bus to the PTI pack. This IDB format is modeled on the standard SM's PIDB format, except that the IDB is at twice the speed and is single-ended-driven instead of differential-driven.

The main features of the LSI pack are:

- Provides DS1 framing and formatting for twenty DS1s.
- Provides Derived Data Link handling of the embedded data links within the framing format of the DS1 signal: either F_S bits for the TR8 interfaces, or bit oriented Extended Superframe/new data link (ESF/ndl) bits for the TR303 interfaces.
- Detects DS1 failure, DS1 alarm, and call origination in TR8 mode 2.
- Provides optional Binary code, 8 Zero Substitution (B8ZS) coding on the DS1s.
- Equalizes transmit cable for its entire length from the IDCU to the DSX cross connect field - quantized into five ranges. (See Notes 302 and 306 in the SD.)
- Collects performance monitoring data, including slips, out-of-frames, bipolar violations, and errored seconds based on incoming DS1 frame information and on the cyclic-redundancy-code, 6 bit (CRC-6) of the ESF format.
- Bundles DS1 signals into compact Internal Data Busses (IDBs) to the PTI.

The pack contains three microprocessors, one acting as master and two as slaves. The master handles general DS1 tasks for the twenty DS1s, while each slave, referred to as a Data Link Processor (DLP), handles the derived data link for ten DS1s.

2.3 PTI CIRCUIT PACK

The PIDB Termination Interface (PTI) contains a Time Slot Interchange (TSI) fabric that can connect any DS1 time slot to any time slot on the PIDBs to the SM Time Slot Interchanger Unit (TSIU), or on the DPIDBs to the Packet Switch Unit (PSU), connects the Time slot Management Channel (TMC) and the Embedded Operations Channel (EOC) of TR303 to the PSU via DPIDBs, and connects multiple DS0 time slots from one DS1 to another DS1 to make internal "hairpin" connections within the IDCU without using any SM resources.

The PTI also performs signal processing, monitoring incoming signaling to detect call originations and transmission of idle signaling. After a call connection is set up, signaling is handled by the PTI's signal processor for all non-ISDN lines. This signaling is contained in the robbed-bit time slots of the DS0 channels of the DS1s.

The PTI distributes timing to both the A and B group LSI packs within its side, and cross-couples timing signals with the mate side PTI, to frequency- and phase-align the DS1 outputs. This aligns the bit occurrence in the LSI's DS1 outputs so that a hitless maintenance switch between active and standby side can be done.

The main features of the PTI are:

- clock generation and timing signals to the LSI packs,
- parity generation and detection for bus to the CCP,
- time-slot-interchange,
- robbed-bit signaling detection,
- idle-code generation in any DS0 time slot,
- interface for up to sixteen PIDBs or eleven DPIDBs,
- terminations for all DPIDBs, and
- phase-locked-loop for timing alignment with the SM.

2.4 CCP CIRCUIT PACK

The Common Control Processor (CCP) is a general-purpose microprocessor board that is the main control of the IDCU. It downloads code from the SM to the PTI and LSI, controls the PTI, and through it, the LSI, and, via the PICB, is the control communications interface to the SM. The CCP pack is also used in the Integrated Services Line Unit 2 (ISLU2) application of the 5ESS® Switch (SD-5D192-01).

The main features of the CCP are:

- 16 MHz, 32-bit, 68020 Microprocessor,
- 2M Static RAM,
- 32K EPROM,
- sanity timer,
- RAM write protection,
- Input/Output (I/O) write protection,
- bus timer,
- interrupt controller,

- mate access, and
- SM PICB interface based on the Unified Control Interface (UCI) device.

2.5 INTERFACES

This section describes the pack interfaces in detail. "0" and "1" designate service groups. "A" and "B" designate twenty-DS1 groups in a maximal configuration. For pin designations and descriptions, refer to the "Designation Mnemonics Index," Sheet A2 of the SD. Detailed descriptions are contained in the circuit description section of each pack schematic, [the "E" sheets of the Circuit Pack Schematics for Manufacture (CPSMs)]. Notes 308 to 322 of the SD list each pack-to-pack or pin field connection, arranged by functional grouping. Sheets BC1 to BC28 list the connections of each circuit path to the pin number on the pack.

2.5.1 INTERFACES of the ELI CIRCUIT

DS1/ELI Interface

The Electrical Line Interface (ELI) card interfaces with twenty 1.544 Mbits/sec DS1 lines from the office Digital signal cross-connect (DSX) bay at a nominal characteristic impedance of 100 ohms.

Facility I/O Pins

A total of eighty I/O pins connect the ELI to the facilities, forty for the T and R output signals to the DSX and forty for the input T1 and R1 signals from the DSX, via AT&T 1249C or 600-type ABAM cabling. See Note 307 of the SD.

LSI/ELI Interface

The ELI packs connect the DS1 facilities to the LSI packs. In the receive direction from the DSX cross-connect bay, the twenty dual-rail DS1 signals (forty signals total) are split into two groups of forty signals each. In the transmit direction to the DSX, the twenty DS1 dual-rail transmit DS1 signals (forty signals total) are connected in parallel from the two LSI packs.

2.5.2 INTERFACES of the LSI CIRCUIT

LSI/LSI Interface

There are twenty bidirectional signal leads that cross-connect an A-group LSI pack to its mate A-group LSI pack on the other service group side of the unit. These signals control hitless DS1 switching between the two sides of the duplicated hardware, and are repeated for the B-group LSI packs.

LSI/PTI Data and Sync Interface (IDB)

An Internal Data Bus (IDB) is used between the PTI and the LSI for the transfer of data. It is similar to a PIDB except that it uses TTL-level signals and does not run all synchronization signals for all busses across the backplane. The IDB is a 8.192 Mbits/sec signals derived from multiplexing/demultiplexing two 4.096 Mbits/sec PIDB formatted signals. The data path carries the PCM and signaling data of the DS1 facilities. The signals necessary for IDB synchronization are a 4.096 MHz clock, a 8.192 MHz clock, a 8 kHz frame sync, and a 111 Hz (9 millisecond period) superframe sync signal.

The LSIs are connected to twenty DS1s each, and the following occurs:

1. The twenty-four-time-slot DS1s are bundled in groups of four.
2. Each DS1 channel is converted to a thirty-two-time-slot, sixteen-bit format and stepped up to a 4.096 Mbits/sec rate.
3. A four-channel bundle is then compressed down to three channels and stuffed time slots are removed.
4. Channel pairs are then bit multiplexed and stepped up to 8.192 Mbits/sec for transmission to the PTI.

This procedure is reversed for the LSI DS1 transmit direction.

LSI/PTI PICB Control Interface

A PICB interface is used by the PTI for pump and control of the LSI. This interface differs from the standard PICB interface in that it uses TTL level signals instead of balanced differential and does not use Select signal, since the PICB is not duplicated per LSI. In all other respects, such as speed and formats, this PICB interface conforms to that of standard Switch PICBs.

2.5.3 INTERFACES of the PTI

PTI/CCP Common Bus Interface

The Common Bus is the interface with which the CCP microprocessor controls the PTI and sends messages to the LSI. It consists of sixteen-bit Address and Data Buses, parity, read and write control signals, interrupts, and memory protection control.

PTI/PSU Interface

The connection to the PSU consists of a maximum of eleven DPIDB interfaces. All signals are balanced differential, and each interface is self-contained and operates at 4.096 Mbits/sec. This interface carries ISDN information to and from the PSU, for LAPD processing, as well as the TMC and EOC channels of the TR303 specification.

DPIDBs are not completely synchronous, like PIDBs, and go through skew compensators within the PTI to adjust for the allowed timing difference of ±3 bits with respect to the master PIDB Port 0. This keeps the DPIDBs aligned with each other as well as with the master PIDB.

PTI/SM PIDB Interface

The PTI-to-SM PIDB interface contains a maximum of sixteen PIDB interfaces, one set from each SM side (active and standby), which are numbered from Port 0 to 15. Only the active or standby set is selected at any one time. PIDB0 is the master PIDB, which implies that all signals (data, clock, and sync) of the PIDB0 interface are terminated on the PTI. For all other PIDBs, the clock and sync signals are not needed and are instead routed to the ELI pack for proper termination, as all signals from the SM are bit and frame synchronous and the PTI is pin limited. The interface signals are differentially driven and operate at 4.096 Mbits/sec.

PTI Synchronization Interface

The PTI to PTI sync interface consists of four signals:

1. a master superframe sync output (SFSYNCO),
2. a master superframe sync input (SFSYNCI),
3. a 4.096 MHz output (4MMCKO), and
4. a 4.096 MHz mate clock input (4MMCKI).

(See FS2.) The superframe sync signals have a period of 9 milliseconds and align the transmit DS1 facility to a common superframe, which ensures that the transmit DS1 facility maintains the same superframe alignment during a switch of the hardware from active to standby.

ELI Control Interface

There are two pull-down resistors on each ELI pack. One resistor is connected to the Side 0 PTI pack and the other to the Side 1 PTI pack, which allows either side PTI to detect the presence of the ELI pack.

2.5.4 INTERFACES of the CCP

CCP/SM PICB Interface

The control interface between the SM and the CCP consists of one standard PICB interface from each side of the SM. All signals are differential and clocked in at 2.048 Mbits/sec.

CCP Mate Update Bus

The CCP Mate Update Bus is used by the active CCP to update the standby CCP so it is ready to switch whenever necessary. The update bus consists of full address and data busses, parity, read and write signals, and BREQ and DORMANT signals. All signals are TTL level. Although the active processor will have control over the standby side, the standby side will have a "concurrent" mode that allows the standby side simultaneous processing of its own on a limited basis. The active side also can read standby side peripherals.

FDI Interface

The Fault Detection and Isolation (FDI) interface allows access to status and control of the LSI circuit packs. It is used to lock and unlock LSIs and to scan the LSI to verify that it is in the correct state (Active/Standby). If the LSI is Active and not responding to signals to go Standby, an Override signal will force the LSI into Standby. This direct interface does not require the ICB interface through the standby side PTI to be functional.

2.6 SYSTEM SYNCHRONIZATION

A 4.096 MHz clock cross couple ensures that the active and mate side DS1 Line ClocKs (LCKs) have a minimum phase difference, by making the transmit Phase-Lock-Loop (PLL) of the mate side use the same 4.096 MHz clock reference as the active side.

To ensure a hitless maintenance switch of the IDCU sides, the transmit line facility data must have no more than 100 nanoseconds of phase difference (jitter) introduced by the side switch. There are three components to this possible phase difference:

1. the DS1 device on the LSI (DSI-S T5292),
2. the PLL, and
3. the SM's phase difference in its Side 0 and Side 1.

The DS1 device on the LSI has a maximum phase error of 20 nanoseconds, which is a DSI-S device specification. The design objective for the transmit PLL is to be less than 20 nanoseconds, though the PIDB clock difference, between active and mate SM sides, may be as much as 60 nanoseconds. Together, these add up to 100 nanoseconds, leaving no phase error margin. However, using the 4MMCKO cross couple ensures that the active and mate transmit line clock PLLs have the same SM reference, which removes the SM's possible 60 nanoseconds phase difference. This, in turn, increases the margin for the unit, giving a total phase difference for the transmit line facility of less than 40 nanoseconds.

The IDCU echo path delay is 0.25 milliseconds + RAND, where RAND is a uniformly distributed random variable with a range of 0 to 0.25 milliseconds.

2.7 IDCU POWER

2.7.1 DESIGN OBJECTIVES

The IDCU power consists of two independent -48 volt power systems, one per service group side. The fusing apparatus is a J5D003BT-1 or J5D003AU-1, using Slow Blow (70-type) frame fuses to a combined Power Converter with Display and Control (PCDC) circuit pack. Each PCDC generates +5 Vdc power and distributes it through the backplane to its service group. Both sides will be powered under normal conditions.

The PCDC can deliver 5 volts at 30 amps maximum, and has the following features:

- current limiting and inrush current limiting,
- low voltage alarm indication,
- low voltage shutdown capability,
- high voltage shutdown capability,
- 0 - 70°C operating temperature range,
- not more than 25 mV output ripple or 100 mV spikes,
- Out-Of-Service (OOS) LED,
- alarm LED,
- scan points to monitor converter state and OOS LED state,
- distribute points to change the OOS state,
- output voltage test jacks, and
- SN connector configuration

The fusing is sized greater than the maximum current for the PCDC. The PCDC, when producing the maximum of 150 watts (30 amps at 5 volts) from a lowest office battery of -39.5 volts and at a converter efficiency of 80%, draws 4.7 amps. The fuse for the IDCU is 5 amps. (See Note 101 of the SD.) Typical measured current draw is 2.0 amps.

Separate grounds are used for signal and frame ground, and are separated on the backplane as well. On the edge of the backplane, all grounds are brought together at a common point before leaving the shelf.

2.7.2 PIN SEQUENCING

Pin sequencing of the packs is done for extra reliability. The normal procedure for pack replacement or insertion is to first transfer service to the opposite side and to then power down the side. With pin sequencing, ground, signals, and power are applied in a controlled sequence to prevent power-up problems such as Complimentary Metal Oxide Semiconductor (CMOS) device latch-up.

2.8 SERVICE GROUPS

2.8.1 SERVICE GROUP SWITCH

The following is an example of a service group switch (from Side 0 to Side 1). Service group equipage was described earlier in this document. Both the active and mate side accept the same traffic from the ELI pack. It is the transmit traffic to the ELI and the DSX that must be switched.

1. Service group 0 is active and carrying traffic.
2. When the decision is made to switch to side 1, the SM begins by unlocking LSI0 by writing to it through PTI0 and CCP0.
3. The standby side LSI1 is updated with LSI information (LSI0 to LSI1) under software control, which is either done across the Update Bus or through the SM.
4. The SM checks that the standby CCP0 is up to date with current traffic information for DS1 states, TSI map, etc.
5. The SM sends the "switch to active" message to LSI1.
6. The SM sends the "switch to standby" message to LSI0.
7. LSI0 switches to standby and acknowledges.

   Each of the twenty DS1s in the LSIs makes a transfer on a logic 0 bit transmission of the DS1 signal. Eventually, all the DS1s will have made the transfer.
8. LSI1 switches to active and acknowledges. If LSI1 is unable to switch to active, the switch is not made and is reversed back to the original state. This operation is done under SM software control.
9. After a successful LSI switch, the data reception path to the SM is then switched, at the PTI-SMP interface, to come from PTI1.
10. Reception from PTI0 and LSI0 stops.

The switch of service groups is completed. Switching of SM sides is an SM procedure and is not covered by IDCU.

2.8.2 FAULT DETECTION and ISOLATION CIRCUIT

The fault detection and isolation circuit detects faulty IDCU areas and isolates them from the rest of the system. Hardware-aided detection capabilities include:

- ELI, LSI, PTI, and CCP pack detection,
- sanity timers,
- loss of clock detectors,
- missing and mis-aligned synchronization detectors,
- parity generation and detection on control and data paths,
- hash checksums for memory,
- background processor audits, and
- LSI "switch to active/standby" verification.

Additional fault detection features are implemented in software.

Once a faulty circuit has been identified, the fault isolation circuit can be used by software to immediately disable the faulty area until further action can be taken. The active fault isolating capabilities include:

- isolating a bad standby LSI from the rest of the system,
- protecting the active CCP from a bad mate CCP by inhibiting the Update Bus, and
- verifying that the mate CCP was really disabled.

2.9 PHYSICAL DESIGN

2.9.1 UNIT LAYOUT

Two general duplex service group layouts are encountered in 5ESS® Switch equipment:

1. symmetrical (mirror image), and
2. replicated.

While replicated layouts are easier to use and are more visually aesthetic, symmetrical layouts have better design characteristics. The IDCU has a symmetrical, duplicated layout, which minimizes the path distance between the circuit packs while allowing the power converter packs to be located at both extreme ends of the shelf.

2.9.2 THERMAL REQUIREMENTS

Maximum power dissipation of the IDCU circuit packs is as listed in Table 1.

TABLE 1. Power Distribution

Board	Power Max	Power Typical
P(CCP)	57W	45W
P(PTI)	30W	21W
P(LSI)	15W	8W
P(ELI)	5W	1W
P(PCDC)	22W	18W

The IDCU shelf has been designed so that these heat loads can be accommodated without undue thermal stress on pack components.

The overall worst-case power dissipation of the IDCU is less than 288 watts, below the maximum shelf power limit of 290 watts. Typical measurements are 210 watts.

2.9.3 CABLING

<u>SM interface bus termination field</u>

The physical layout of the PICB, PIDB, and DPIDB cable terminations on the IDCU backplane is contained in one central pin field on Side 0 and another pin field on Side 1. (See Note 207 and 208 in the SD.) Although sixteen PIDB and eleven DPIDB ports are allocated pin field locations, not all positions can be populated simultaneously. (See "Interconnect Restrictions" below.)

<u>DS1 cable terminating field</u>

The DS1 lines (1249C-type cable and 600-type ABAM) are terminated directly on the ELI pin field. The transmit and receive lines are bundled in separate cables to minimize cross-talk and interference. (See Note 208 of the SD.)

<u>Power and ground termination</u>

The IDCU backplane has a power and ground bus (-48V and -48V RTN) connected to Side 0 and to Side 1.

2.9.4 HARDWARE

The IDCU hardware packaging is the standard Fastech® System. The shelf relies on the 132G apparatus mounting. The circuit packs and their associated hardware are described in Table 2.

TABLE 2. Circuit Pack Physical Features

Circuit Packs	Type	Faceplate	Width
CCP	UN	12	1 inch
PTI	KBN	6014	1-1/2 inches
LSI	TN	12	1-1/4 inches
ELI	KBN	6014	1-1/2 inches
PCDC	SN	12	1-1/4 inch

2.9.5 CABINET TYPE

The IDCU shelf fits into the existing 5ESS® Switch Line Trunk Peripheral (LTP) cabinet, equipped with a six-fan unit. Furthermore, because no constraints exists on the type of fuse/filter panel and the thermal dissipation, the IDCU can use space available in existing LTP cabinets.

2.9.6 INTERCONNECT RESTRICTIONS

Because of PTI pin limitations, certain pins on the circuit pack are programmed as either PIDB or DPIDB pins. The pin field on the backplane has space allocated for sixteen PIDBs and eleven DPIDBs, but not all positions can be used simultaneously. A range of PTI interface configurations is possible: a maximum of sixteen PIDBs with up to seven DPIDBs, or a maximum of eleven DPIDBs with up to eight PIDBs. The rule that sets the limits for PIDBs and DPIDBs is that the number of PIDBs plus two times the number of DPIDBs must be less than or equal to thirty:

PIDBs + (2 x DPIDBs) ≤ 30

The configuration is not dynamic and is set at installation.

2.9.7 EMI/EMC/ESD DESIGN FEATURES

(Standard 5ESS® Switch procedures should always be followed regarding ESD practice.) The IDCU packs have been designed to have low ElectroMagnetic Interference (EMI) emissions and high resistance to ElectroStatic Discharge (ESD). Some of these features are:

- Circuit pack I/Os are designed so that the highest frequency signals are adjacent to a signal ground.
- Low EMI emission integrated circuit drivers are used for (D)PIDBs and PICBs.
- The PICB differential drivers have a ground reference at the IDCU.
- Effective grounding:
  - All circuit packs and backplanes have both a signal and a frame ground, with the signal ground being a ground plane.
  - The circuit jacks connect to the backplane using a multipoint ground.
- To prevent propagation of common mode noise on the DS1 facility cables, the ELI has a center shield on the transformers for the transmit path and a choke filter for the receive path.
- An ESD path ring on the perimeter of the circuit pack is connected to frame ground.

3. REFERENCE DATA

3.1 WORKING LIMITS

Office battery voltage at the unit is from -39.5 volts to -60.0 volts.

The IDCU has an operating component temperature range of 0°C to 70°C. Unit level heat loads fall within internal 5ESS® Switch guidelines for central office compatibility.

3.2 FUNCTIONAL DESIGNATIONS

CIRCUIT PACK:

Designation	Meaning
ELI	Electrical Line Interface
LSI	Loop Side Interface
PTI	PIDB Termination Interface
CCP	Common Control Processor
PCDC	Power Converter with Display and Control

INTERFACE CABLES:

Designation	Meaning
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
DPIDB	Direct PIDB
DS1	Digital Signal 1 (1.544 Mbits/sec)
-48V/RTN	Nominal -48 volt central office battery plant and Return

3.3 INDICATORS

Designation	Meaning
ALM	PCDC has entered an alarm state
OFF	PCDC is not generating +5 volt power to an IDCU side
OOS	Indicated side of the IDCU is Out-Of-Service

3.4 CONTROLS and TEST POINTS

Designation	Meaning
±5V	PCDC's output voltage test points
ON	Cause PCDC to generate +5 volt power to an IDCU side
OFF	Stop PCDC +5 volt generation, if IDCU side is OOS
MOR	If pushed while OFF is also pushed, stops +5 volt power generation, regardless of OOS state

3.5 FUNCTIONS

The IDCU has the following functions:

- TR008 interface for remote terminals,
- TR303 interface for remote terminals, and
- PUB43801 interface for general DS1 trunking.

3.6 CONNECTING CIRCUITS

The IDCU connects to the following circuits:

- The PICB interfaces to the 5ESS® Switch Control Interface (CI) circuit pack, which is part of the Switching Module Processor Unit (SMPU) (SD-5D040-02) or SMPU2 (SD-5D192-01).
- The PIDB interfaces to the 5ESS® Switch Data Interface (DI) circuit pack, which is part of the SM TSIU (SD-5D041-01) or TSIU2 (SD-5D045-01).
- The DPIDB interfaces to the 5ESS® Switch Packet Switch Unit (SD-5D074-01).
- The DS1 signals connect to the office DS1 facility interfaces at the DSX1 bay (SD-99503-01).
- The -48 volt power inputs connect to various 5ESS® Switch Fuse and Filter Units (SD-5D053-01 or SD-5D087-01).

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DEPT 55534-CHS-DEH

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4. AT&T, Technical Reference: Digital Channel Bank Requirements and Objectives, PUB43801, November, 1982.