

**5ESS® SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT  
MODEL 2  
CIRCUIT**

**4. REASONS FOR REISSUE**

*B. Changes in Apparatus*

Added option N, which provides the TN1802 circuit pack.

Added option M, which uses a 982TRC lightwave data transceiver (LDT).

*D. Description of Changes*

Option N was added to the block diagram, FS1 and FS2 symbols 3 and 16, and to apparatus figures.

Option M, which provides the LDT which meets the international cisper 22 EMC requirement, was added to FS1 and FS2 symbols 1, 2, 4, 15, 23, and 24, to apparatus figures, and to CAD1 element identifiers AA, AB, AC, and AD.

Note 102 was added to provide fusing information.

Note 103 was added to provide programming plug position information for circuit packs TN619, TN1802, and TN1039.

Note 302, 303, and 304 were changed, and note 305 was added to show option N.

Note 302 and 303 were changed, and note 306 was added to show option M.

The symbol table was changed to show the DLI C/D interface cabling alternative.

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DEPT NA5380700-WFG-SDS

CIRCUIT DESCRIPTION

CD-5D401-01  
ISSUE 1  
APPENDIX 6M  
DWG ISSUE 7M  
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT,  
MODEL 2  
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added option "P" which specifies the new ODL50 type fiber optic connectors. Option "Q" specifies the old ODL40 type fiber optic connectors.

D. Description of Changes

D.1 The new ODL50 type fiber optic connectors are a cost reduction.

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CIRCUIT DESCRIPTION

CD-5D401-01  
ISSUE 1  
APPENDIX 5A  
DWG ISSUE 6A  
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT

FACILITIES INTERFACE UNIT,  
MODEL 2  
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added option R which provides a TN618D for 24-channel and 30-channel units.

D. Description of Changes

D.1 Options R and T must be used for 30-channel operation. Option R or V may be used for 24-channel operation with option S. Option R is now standard.

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5ESS™ SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT  
MODEL  
CIRCUIT

CHANGES

A. Changed and Added Functions

A.1 None.

B. Change in Apparatus

B.1 Added Option V, which uses a TN618C in 24 (domestic) channel or 30 (international) channel units. Option Y uses a TN618B in 24 channel units only. Option Z uses a TN618 when the clock unit is not used in a remote switching module (RSM).

D. Description of Changes

D.1 Canceled circuit pack TN1364 for use in international units. International unit require 30 channel units, compared to 24 channel units for domestic units. Changing the TN618 or TN618B to TN618C will work for both domestic and international service. Option T wiring will be required for international use.

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CIRCUIT DESCRIPTION

CD-5D401-01  
ISSUE 1  
APPENDIX 3A  
DWG ISSUE 4A  
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT,  
MODEL 2  
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added Option X, which uses circuit packs TN1039 and TN1364 for international use instead of circuit packs TN619 (Option W) and TN618B (Option Y), respectively, used in domestic applications. See FS 1 and App Fig. 2.

D. Description of Changes

D.1 International units require 30 channel units as compared to 24 channel units used on domestic units. Changing the TN619 to a TN1039 and the TN618B to a TN1364 accomplishes this requirement.

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CIRCUIT DESCRIPTION

CD-5D401-01  
ISSUE 1  
APPENDIX 2AC  
DWG ISSUE 3AC  
DISTN CODE 7T13

5ESS™ SWITCHING EQUIPMENT

FACILITIES INTERFACE UNIT,  
MODEL 2  
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Some nets were tied together in error. This was corrected by changing the net names and removing wires on FS 1 (Symbols 3, 6, 10, and 13) and CAD 1.
- D.2 Incorrect terminals were specified in wiring to the control and display circuit. This was rectified by removing and adding wires on CAD 002.

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SESS™ SWITCHING EQUIPMENT  
 FACILITIES INTERFACE UNIT,  
 MODEL 2  
 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The facilities interface unit (FIU) connects the module control unit (MCU) and the time slot interchange unit (TSIU) of a remoted interface module (IM) to trunk facilities provided from the SESS™ host office of a T1 carrier.

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## 2. GENERAL

2.01 The FIU circuit is divided into FS 1 and FS 2. FS 1 is group/side 0 and FS 2 is group/side 1. The terms "both sides" or "each side" means FS 1 and FS 2.

2.02 The combination of a facilities interface unit (FIU) and a remoted interface module (IM) is called a remoted switching module (RSM). The remote digital lines originate from one or two digital line trunk units (DLTUs) of an IM at the host office, which is referred to as the host interface module (HIM). The DLTUs are equipped with a digital facility interface (DFI) for each T1 carrier line.

2.03 The DFIs recover data, and control designated data channels and timing from the T1 lines. The FIU formats this information into a pair of network control and timing (NCT) link signals. These signals are routed to the time slot interchange unit (TSIU) over optical fiber pairs.

2.04 The DFIs also decode messages that can be used to establish communication on the initial control link, or to force a restart of the module processors (MP) of the RSM. These messages are sent over a derived data link (DDL) on each T1 line from the host interface module.

2.05 The subunits of the FIU and the associated DFIs are controlled by peripheral control channels (PCCs) from the MPs. A peripheral control channel is realized through a peripheral interface control bus (PICB) composed of five wire-pairs that are driven by a control interface (CI) from one side of the module control unit (MCU). A maximum of 22 peripheral control channels are required from each side of the module control unit to support up to 20 digital facility interfaces and the duplex FIU hardware.

2.06 Through the peripheral control channels, the RSM maintenance software forces each subunit to be initialized, receives reports of hardware failures, and initiates diagnostic testing.

## INTERFACES

### A. Trunk Facilities

2.07 The FIU interfaces with the trunk facility through one or two digital line trunk units (DLTUs) that are equipped with a digital facility interface (DFI) for each T1 line. A minimum of 4 to a maximum of 20 T1 lines can be used.

2.08 Each T1 line terminates on a DFI that is controlled by the active module processor (MP) through one of its peripheral control channels (PCC).

2.09 Each DFI interfaces to the FIU via a facilities interface data bus (FIDB) and must be configured to operate in the RSM mode, whereby the DFIs provide 23 clear data channels (no signaling bits or zero suppression imposed upon the data words) and use the remaining time slot of the T1 line to send signaling information for the 23 data channels. In this mode, the DFIs also provide T1 clock signals to the FIU. These signals are used to lock a local crystal oscillator within the FIU to the network clock provided by the host office. This oscillator in turn determines the data rate on the network control and timing (NCT) links, assuring synchronization of the RSM to its host. This same oscillator provides accurate timing for the RSM during stand-alone operation.

### B. Module Control Unit (MCU)

2.10 The FIU interface with the module control unit (MCU) has two components, the peripheral control channels (PCCs) and the module

processor (MP) reset leads. A PCC must be provided by each side of the MCU for accessing each side of the FIU and each DFI.

2.11 The pair of PCCs used by each side of the FIU provides for initialization and maintenance of the circuit packs in this unit. The PCCs terminate in several control registers and error registers. Another pair of PCCs is required for each equipped DFI slot of the digital line trunk units (DLTUs). These PCCs are used to initialize and maintain the DFIs and to pass messages between the MP and the DFI for transmission over the derived data link (DDL) to the host interface module (HIM). Similarly, a message received over the DDL can be passed to the MP from the DFI by its PCC.

2.12 Central processor intervention (CPI) has the capability to reset both processor halves of the RSM from the central processor (CP). It is used in case software errors prevent the standby MP from gaining control of the module control unit (MCU)/time slot interchange unit (TSIU). The existing CPI circuitry that removes CPI messages from bit 7 of the control time slot at the duplex link interface (DLI) can operate incorrectly at a RSM during software failure. In that event, a "last resort" capability has been added which utilizes a derived data link (DDL) message that has been reserved for local decoding at each DFI. Upon receiving this message, the DFI can output a signal to a majority voting circuit in the FIU.

2.13 The voting circuit, which is not under module processor (MP) control, examines all of its inputs from the DFIs and determines when and whether to cause a reset. The majority vote feature prevents an inadvertent

reset of the MPs by requiring the reset-message produced signal from a majority of those DFIs whose digital line status is known to be good.

2.14 To force RSM reset, the central processor (CP) sends a message to the host interface module (HIM), requesting it to send the reset message to the RSM over each DFIs derived data link. The HIM outputs this message only to those DFIs whose T1 line is operational. This prevents a reset of a RSM that is in stand-alone and has no way of completing the boot process because of facility failures.

### C. Time Slot Interchange Unit (TSIU)

2.15 The FIU interfaces to the TSIU through two service groups of two network control and timing (NCT) links. Each provides up to 229 data time slots and one control time slot. The remaining time slots, which are distributed throughout the NCT frame are stuffed with idle code. The control time slot can be provided on any of the incoming T1 lines (time slot 1 is proposed for this purpose), and can appear at any of ten locations within the NCT frame. During the initialization of the RSM, the RSM and the HIM, communicate with each other over the derived data links.

2.16 The purpose of these communications is to obtain an agreement upon the use of a particular T1 line to carry the initial control channel.

### 3. FACILITY INTERFACE CIRCUIT (FS 1, FS 2)

#### GENERAL

3.01 The hardware used to implement the FIU is functionally divided into three circuit pack types: multiplexer (MUX); link interface (LI); and clock-control (CLK-CNT).

#### LINK INTERFACE

3.02 The link interface (LI) is a TN834 circuit pack. Two of these circuit packs are controlled by the TN618 CLK-CNT circuit.

3.03 The LI takes data from the multiplexer (TN619) output bus and forms a network control and timing link signal, which is transmitted over a fiber guide to the TSIU.

3.04 The LI also receives the network control and timing (NCT) link signal output from the TSIU, recovers data, and performs frame synchronization. The resultant data is written into a variable length "first in first out" (FIFO) buffer that is used to synchronize the time slot of the data output to the multiplexer (TN619) subunit.

#### CLOCK-CONTROL

3.05 The clock-control (CLK-CNT) (TN618) circuit pack provides timing, control distribution, and an interface through two peripheral control channels to both module processor sides for all circuit packs. Timing is also transmitted to the TSIU of the RSM via the 32 MHz fiber optic links and then recovered from the fiber link data stream by the LIs in the TSIU. The T1 remote switching module reset function is also provided in the TN618.

#### MULTIPLEXER

3.06 The multiplexer (MUX) circuit pack (TN619) provides a fixed time slot mapping of data carried over ten facility interface data buses (FIDBs) into a 256 time slot format that is then converted to a NCT link signal by a LI subunit.

3.07 Two MUX and LI pairs are utilized to provide the A and B NCT links

which interface to the TSIU. Synchronization and clock signals for these conversions are provided by the CLK-CNT circuit pack. The MUX can also be directed to loop data from the LI or a particular FIDB back towards the TSIU for use in diagnostic testing of the MUX and LI circuit packs.

#### POWER UNIT

3.08 The 495LA power unit supplies the necessary +5 volts for proper operation of the circuit packs. Each group (FS 1, FS 2) has its own power unit.

#### POWER CONTROL AND DISPLAY

3.09 The power control and display circuit pack (SN516) conveys the status of a FIU group. It contains switches to power up and power down a FIU group. It also has a switch to request a group out-of-service. These switches and associated LED indicators provide a craft interface for that service group, located in the DLI unit.

#### SECTION II - DETAILED DESCRIPTION

##### 1. FACILITY INTERFACE CIRCUIT (FS 1, FS 2)

###### GENERAL

1.01 Since FS 1 and FS 2 are similar, only one FS is described. FS 1 is group/side 0 and FS 2 is group/side 1. The term "both sides" means FS 1 (group/side 0) and FS 2 (group/side 1).

###### LINK INTERFACE

1.02 The link interface (LI) is a TN834 circuit pack. Two of these circuit packs are controlled by the TN618 CLK-CNT circuit. The LI takes data from the MUX output bus and forms a network control and timing (NCT) link

signal, which is transmitted over a fiber guide to TSIU.

1.03 The LI also receives the NCT link signal output from the TSIU, recovers data, and performs frame synchronization. The resultant data is written into a variable length "first in-first out" (FIFO) buffer that is used to synchronize the time slot of the data output to the MUX.

1.04 To form the NCT link signal, the LI takes data word nibbles from the MUX output bus, and after checking for odd parity across each word, forms the NCT link signal by inserting a framing pattern, scrambling the resulting data, and then outputting it serially at 32.768 MHz to the DLI in the TSIU.

1.05 The LI receives the NCT link signal output from the DLI and recovers a receive clock from transitions in the data stream. It then descrambles the data and performs frame synchronization. The resultant data is written into a variable length FIFO buffer that is used to synchronize the time slot of the data output to the MUX so that it is the same as the time slot of the data input from the MUX. The receive data word parity is checked and then regenerated by the LI before it is outputted in nibbles to the MUX. This parity check and generation can be used to provide a known data pattern for testing a LI when the mu has been set into the LI data loopback mode of operation.

1.06 Timing signals are required for the LI to transmit data to the TSIU and also to align the transmit and receive data time slots at the MUX interface. These signals are generated from a 32 MHz clock, a 2 MHz synchronization pulse stream, and a

time slot count that are produced by the CLK-CNT circuit pack. These signals are phase locked to the receive T1 clock frequency of one of the DFIs so that the derived timing within the TSIU is identical to that of the host office, thereby eliminating facility framing slips. The CLK-CNT subunit also provides each LI with a CONTROL REGISTER and shares an ERROR REGISTER between them. Both registers can be accessed by the MP through the active PCC.

1.07 The LIs provide several features for diagnostic purposes. By writing to the LI CONTROL REGISTER, a specific LI can be configured to send idle code, disable framing sequence, invert transmit parity, invert receiver parity, loop, and place the associated error register into a test mode.

1.08 The NCT link data stream of each LI can be looped back to its own receiver to isolate a framing or data parity error to either the LI in the T1 FIU, the NCT link, or the LI of the DLI. When this loopback occurs, the LOOP bit is set (one) in the ERROR REGISTER for the appropriate LI. Thus the MP cannot "forget" that it has placed the LI into this test state.

1.09 While the LI is looped back, the associated MUX must also be placed into the LI data loopback mode while the LI forces idle code to be sent towards the MUX. This sends the LI a known signal for use during the data loop test. Note that the MUX loops the idle code back towards the LI without checking or regenerating the parity of the data words. A further test of the data processing capabilities of the LI is obtained by having the MP insert a test pattern at the TSI while the MUX loops this data back through the LI, and then testing that data at the TSI.

CLOCK-CONTROL

1.10 The CLOCK-CONTROL (CLK-CNT) circuit pack (TN618) provides timing, control distribution, and an interface through two PCCs to both MP sides for all circuit packs of the FIU. Timing is also transmitted to the TSIU of the T1 RSM via the 32 MHz fiber optic links and then recovered from the fiber link data stream by the LI subunits in the TSIU. The T1 RSM reset function is also provided by the CLK-CNT subunit.

A. Timing

1.11 Clock signals are derived from the output of a 128B crystal oscillator used in a phase locked loop (PLL). Operating at the NCT link rate of 32,768 MHz, the oscillator output is used to generate various clocks, sync pulses, the time slot count for the NCT link frame, and the frame bit sequence.

1.12 The PLL can be set to operate in either the master mode or the slave mode. When in the master mode, a CLK-CNT circuit pack can be set either to select a digital facility interface (DFI) as the timing reference source or to free-run at the internal crystal oscillator frequency. In the slave mode, a CLK-CNT circuit pack is locked to the 8 MHz output of its mate. An interlock is provided so that at least one CLK-CNT circuit pack side is in the master mode.

B. Control Interface

1.13 Circuitry of the CLK-CNT circuit pack provides the interfaces to both module processor (MP) sides through peripheral control channels (PCCs). PCCs from the MPs terminate in fourteen control and error registers. One MUX CONTROL REGISTER and one MUX ERROR REGISTER reside on each MUX subunit, while ten other registers reside on the CLK-CNT subunit.

1.14 The control registers are both readable and writable. The error registers are latching and are cleared by a read operation, thereby removing the interrupt from that error register for transient errors. If a hard fault exists, then the error interrupt remains. Any specific bit of an error register can be masked from causing an interrupt by writing a "1" to that bit. This action does not change the error register contents but does prevent the possible error condition from causing an interrupt.

1.15 The logical sense of an error register input can be reversed by writing a one to the INT TEST bit of the appropriate control register. This input reversal, when used in conjunction with individual bit interrupt masking, enables testing of the error registers.

C. DFI Interface

1.16 Each DFI subunit sends four signals via a bus to the CLK-CNT subunit. These are T1 CLOCK, T1 STATUS, DFI STATUS, and RSM RESET. The T1 CLOCK signal is a 1.544 MHz clock signal which the DFI has recovered from its incoming T1 line and can be used for synchronization to the network. The T1 STATUS signal is an indication of whether the T1 CLOCK signal is acceptable for use as the reference for synchronization. The DFI STATUS signal indicates the state of the DFI microcomputer and is used in conjunction with the RSM RESET signal to determine a possible reset for the T1 RSM.

D. Reset Function

1.17 An office interface module can be reset via central processor intervention (CPI), a process which is capable of handling multilevel resets. Due to the complex control-link path of the RSM, an additional reset has been

implemented. The path of this additional reset is independent of MP control and therefore cannot be disrupted by an uncooperating MP.

1.18 The usage of a RSM reset requires that the host interface module send reset messages over all derived data links of the DFIs associated with the target RSM.

1.19 The RSM reset path from the host to the CLK-CNT reset circuit can be tested by sending a reset message through only one DFI to the RSM. This single reset is detected by the DFI and passed to the CLK-CNT subunit, where it fails the majority vote but sets an error bit to cause an interrupt.

#### MULTIPLEXER

1.20 The MULTIPLEXER (MUX) circuit (TN619) provides a fixed time slot mapping of data carried over ten FIDBs (facilities interface data buses) into a 256 time slot format that is then converted to a NCI link signal by a LI subunit. Two MUX and LI pairs are utilized to provide the A and B NCI links required for the proper operation of each side of the TSIU. Synchronization and clock signals for these conversions are provided by the CLK-CNT circuit pack.

1.21 The MUX also provides data parity test capabilities required to maintain portions of both the DFI and the LI interfaces. Errors in data parity are automatically detected and reported through the CLK-CNT circuit pack to the CI of the MCU. The MUX can also be directed to loop data from the LI or a particular FIDB back towards the TSIU for use in a diagnostic testing of the MUX and LI circuit packs.

1.22 The MUX is logically divided into five main sections: transmit data processing; peripheral interface;

receive data processing; timing generation; and control distribution with error reporting.

#### POWER UNIT

1.23 The 495LA power unit is capable of delivering about 18 amperes at +5.0 volts. It has programmable current limiting via programming resistors located on each subunit. The value of each resistor is determined by the current requirements of the particular subunit. The power unit output can never supply current to a fault in excess of 5 amperes. A second output voltage at +12.0 volts can supply 0.4 amperes and is regulated separately from the +5.0 volt output.

1.24 The power unit operates at about 50% of its load capacity with an expected efficiency of greater than 75%, supplying power to one side. This power unit requires craft interaction to start the unit once it has entered the off state. It can enter the off state by craft intervention or by detection of voltage and/or current excursions which exceed preset limits. The unit must be started using its remote start feature via the power control and display (SN516) unit that is in the adjacent slot in the shelf assembly.

#### POWER CONTROL AND DISPLAY

1.25 The power control and display circuit pack (SN516) conveys the status of a FIU group. It contains switches to power up and power down a FIU group. It also has a switch to request a group out-of-service. These switches and the associated LED indicators provide a craft interface for that service group.

1.26 The SN516 performs its functions via scan and distribute points that are read and written from the MP. It is powered directly by office

battery and provides isolated interfaces to the scan and distribute unit through optical isolators.

The SN516 pack has a face plate with four switches and five LEDs whose functions are as follows:

- (1) ON - A momentary pushbutton used to power up the FIU's side.
- (2) OFF - A momentary pushbutton used to power up the FIU side only if that side is out-of-service.
- (3) RST-ROS - A slide switch used to request a side either in service or out-of-service.
- (4) MOR - A momentary pushbutton manual override switch. Whenever it is simultaneously depressed with the OFF switch, power is turned off.
- (5) OFF - A red LED that lights whenever logic power is off.
- (6) ALM - A red LED that lights whenever there is a power fault on the side (fuse or converter alarm). Once the craft powers down the side for repairs, the OFF LED lights, and the ALM LED extinguishes.
- (7) OOS - A yellow LED controlled by the MF and is lit whenever the side is out-of-service.
- (8) RGIP - A green LED controlled by the MP. It lights whenever a request to restore or remove a

unit has been received by the MP. If this request is denied, this LED flashes for 5 to 10 seconds.

- (9) ROS - A green LED that lights whenever the ROS/RST switch is in the ROS (request out-of-service) position.

### SECTION III - REFERENCE DATA

#### 1. WORKING LIMITS

1.01 Working limits for the individual circuits are in their respective schematic drawing circuit descriptions.

#### 2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for the individual circuits are in their respective schematic drawing circuit descriptions.

#### 3. FUNCTIONS

3.01 Function information for individual circuits are in their respective schematic drawing circuit descriptions.

#### 4. CONNECTING CIRCUITS

4.01 Connecting circuit information is provided in Issue 2.

#### 5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are provided in Issue 2.

AT&T BELL LABORATORIES

DEPT 55614-EAM-DPS

5ESS<sup>TM</sup> SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT,  
MODEL 2  
CIRCUITSECTION I - GENERAL DESCRIPTION1. PURPOSE

1.01 The Facility Interface Unit (FIU) is the transmission hardware which enables a 5ESS Interface Module (IM) to be remoted from the Central Office over T1 lines. The remoted IM and its peripherals are known as a 5ESS Remote Switching Module (RSM). Digital Facility Interfaces (DFI) in conjunction with the FIU convert the T1 data to Network, Control, and Timing (NCT) Link Data which then interface directly to the IM.

SECTION II - DETAILED DESCRIPTION1. GENERAL

The RSM traffic requirements determine whether 4 or up to 20 T1 lines will be utilized. Each T1 line terminates on a RSM Digital Facility Interface (R-DFI) which converts the T1 format to the Facility Interface Data Bus (FIDB) format. The FIDB's then terminate on a Facility Interface Unit (FIU) which converts the data to two Network Control and Timing (NCT) Links.

1.01 The FIDB data which terminate on two MUXs contained in the FIU (TN619) combines the data from up to 10 R-DLIs and maps the timeslots into a nibble data stream suitable for the Link Interface (LI). The LI then converts this nibble data stream into an NCT link signal which enters the Duplex Link Interface (DLI) of the IM. Since there is no cross-coupling between sides of the FIU and DLI, the two units are in the same service group and are thus switched as a single entity.

1.02 The interface between the R-DFI and FIU consists of FIDBs and control signals which terminate on the CNTLR (TN618B) circuit pack. Each R-DFI sends the CNTLR board the following signals:

T1Clock - A 1.544 MHz clock is provided to the FIU for synchronizing the 32.768 MHz oscillator on the TN835 circuit pack to the network clock. The CNTLR circuit divides the T1CLOCK signals from the 20 R-DFI's into two groups, A and B. The T1 select register of the CNTLR circuit is used to select a single clock source from each group. The CNTLR control register then selects either group A or B as the active timing reference, and the other as the backup reference.

T1STATUS - This signal is used to indicate the status of the T1 line which R-DFI terminates. The T1STATUS lead will show bad status if the T1 clock cannot be recovered.

SECTION III - REFERENCES

None.

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