

**5ESS® SWITCHING EQUIPMENT  
FACILITIES INTERFACE UNIT  
MODEL 3  
UNIT**

**4. REASONS FOR REISSUE**

*B. Changes in Apparatus*

Added option T, which uses a 982TRC or 982TSC light wave data transceiver (LDT).

*D. Description of Changes*

Option T, which provides the LDT which meets the international CISPR 22 EMC requirement, was added to FS1 and FS2 symbols 4, 21, and, 22, to apparatus figures, and to CAD 1 element identifiers DV, DW, DX, and DY.

Note 102 was added to provide programming plug position information for circuit packs TN619, TN1802, and TN1039.

Notes 302, and 303 were changed, and note 307 was added to show option T.

The symbol table was changed to show the DLI C/D interface cabling alternative.

AT&T BELL LABORATORIES

DEPT NA5380700-WFG-SDS

CIRCUIT DESCRIPTION

CD-5D401-02  
ISSUE 1  
APPENDIX 3A  
DWG ISSUE 4A  
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT  
FACILITY INTERFACE CIRCUIT  
MODEL 3  
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added option U which uses circuit pack TN1802 in place of option Y, which uses circuit pack TN619.

D. Description of Changes

D.1 FS1, 2 and apparatus figures have been revised to add option U TN1802 circuit pack.

D.2 Notes 302 and 304 have been revised to add option U TN1802 circuit pack, which will be used in place of circuit pack TN619 in the FIU unit for the 24 channel application whenever the DLTU2 is used with the FIU.

F. Changes In CD Sections

F.1 None.

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5ESS® SWITCHING EQUIPMENT  
 FACILITY INTERFACE UNIT,  
 MODEL 3  
 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The facilities interface unit (FIU) connects the module control unit (MCU) and the time-slot interchange unit (TSIU) of a remoted switch module (SM) to trunk facilities provided from the 5ESS® host office of a T1 carrier.

2. GENERAL

2.01 The FIU circuit is divided into FS 1 and FS 2. FS 1 is group/side 0, and FS 2 is group/side 1. The term "both sides" or "each side" means FS 1 and FS 2.

2.02 The combination of a facilities interface unit (FIU) and a remoted switch module (SM) is called a remoted switching module (RSM). The remote digital lines originate from one or two digital line trunk units (DLTUs) of an SM at the host office, which is referred to as the host switch module (HSM). The DLTUs are equipped with a digital facility interface (DFI) for each T1 carrier line.

2.03 The DFIs recover data and control designated data channels and timing from the T1 lines. The FIU formats this information into a pair of network control and timing (NCT) link signals. These signals are routed to the time slot interchange unit (TSIU) over optical fiber pairs.

2.04 The DFIs also decode messages that can be used to establish communication on the initial control link.

2.05 The subunits of the FIU and the associated DFIs are controlled by peripheral control channels (PCCs) from the module processors (MPs). A peripheral control channel is realized

through a peripheral interface control bus (PICB) composed of five wire-pairs that are driven by a control interface (CI) from one side of the module control unit (MCU). A maximum of 22 PCCs are required from each side of the MCU to support up to 20 digital facility interfaces and the duplex FIU hardware.

2.06 Through the PCCs, the RSM maintenance software forces each subunit to be initialized, receives reports of hardware failures, and initiates diagnostic testing.

INTERFACES

A. Trunk Facilities

2.07 The FIU interfaces with the trunk facility through one or two digital line trunk units (DLTUs), equipped with a digital facility interface (DFI) for each T1 line. A minimum of 2 to a maximum of 20 T1 lines can be used for 24 channel applications. A minimum of 2 to a maximum of 16 T1 lines can be used for 30 channel applications.

2.08 Each T1 line terminates on a DFI that is controlled by the active module processor through one of its peripheral control channels (PCCs).

2.09 Each DFI interfaces to the FIU via a facilities interface data bus (FIDB) and must be configured to operate in the RSM mode, whereby the DFIs provide either 23 or 30 (for 24 or 30 channel respectively) clear data channels (no signaling bits or zero suppression imposed upon the data words. For the 24 channel application, the remaining time-slot of the T1 line is used to send signaling information for the 23 data channels. In the 30 channel application, a 2 msec multiframe (16 frames, each having time-slots 0-31) is structured so that

TS-0 contains frame alignment and control bit information while TS-16 is the signaling channel. In this mode, the DFIs also provide T1 clock signals to the FIU. These signals are used to lock a local crystal oscillator within the FIU to the network clock provided by the host office. This oscillator, in turn, determines the data rate on the NCT links, assuring synchronization of the RSM to its host. This same oscillator provides accurate timing for the RSM during stand-alone operation.

### B. Module Control Unit (MCU)

2.10 The FIU interface with the module control unit has only one component: the peripheral control channel (PCC). A PCC must be provided by each side of the MCU for accessing each side of the FIU and each DFI.

2.11 The pair of PCCs used by each side of the FIU provides for initialization and maintenance of the circuit packs in this unit. The PCCs terminate in several control registers and error registers. Another pair of PCCs is required for each equipped DFI slot of the digital line trunk units. These PCCs are used to initialize and maintain the DFIs and to pass messages between the MP and the DFI for transmission over the derived data link (DDL) to the host switch module (HSM). Similarly, a message received over the DDL can be passed to the MP from the DFI by its PCC.

2.12 Central processor intervention (CPI) has the capability to reset both processor halves of the RSM from the central processor (CP). It is used in case software errors prevent the standby MP from gaining control of the module control unit time-slot interchange unit (TSIU).

### C. Time Slot Interchange Unit (TSIU)

2.13 The FIU interfaces to the TSIU through two service groups of two network control and timing links. Each provides up to either 229 data time-slots and one control time-slot (24 channel) or 239 data time-slots and one control time-slot (30 channel). The remaining time slots, which are distributed throughout the NCT frame, are stuffed with idle code. The control time slot can be provided on any of the incoming T1 lines (time slot 1 is proposed for this purpose), and can appear at any of 10 locations within the NCT frame. During the initialization of the RSM, the RSM and the host switching module (HSM), communicate with each other over the derived data links.

2.14 The purpose of these communications is to obtain an agreement on the use of a particular T1 line to carry the initial control channel.

### 3. FACILITY INTERFACE CIRCUIT (FS 1, FS 2)

#### GENERAL

3.01 The hardware used to implement the FIU is functionally divided into three circuit pack types: multiplexer (MUX) TN619 (24 channel) or TN1039 (30 channel); dual link MUX interface (DLMI); and clock-control (CLK-CNT).

#### DUAL LINK MUX INTERFACE

3.02 The dual link MUX interface (DLMI) TN1510 circuit pack has two link interfaces on board. Both are controlled by the TN618 CLK-CNT circuit via interfaces on the TN1510 pack.

3.03 The DLMI/LI takes data from the multiplexer (TN619/TN1039) output

bus and forms a network control and timing link signal, which is transmitted over a fiber guide to the TSIU.

3.04 The DLMI/LI also receives the network control and timing (NCT) link signal output from the TSIU, recovers data, and performs frame synchronization. The resultant data is written into a variable length "first in first out" (FIFO) buffer that is used to synchronize the time-slot of the data output to the multiplexer (TN619/TN1039) subunit.

#### CLOCK-CONTROL

3.05 The clock-control (CLK-CNT) (TN618) circuit pack provides timing, control distribution, and an interface through two peripheral control channels to both module processor sides for all circuit packs. Timing is also transmitted to the TSIU of the RSM via the 32 MHz fiber optic links and then recovered from the fiber link data stream by the LIs in the TSIU.

#### MULTIPLEXER

3.06 The multiplexer (MUX) circuit pack (TN619/TN1039) provides a fixed time-slot mapping of data carried over ten facility interface data buses (FIDBs) into a 256 time-slot format that is then converted to a NCT link signal by a DLMI subunit.

3.07 Two MUX and LI pairs (in a DLMI) provide the A and B NCT links that interface to the TSIU. Synchronization and clock signals for these conversions are provided by the CLK-CNT circuit pack. The MUX can also be directed to loop data from the DLMI or a particular FIDB back towards the TSIU for use in diagnostic testing of the MUX and DLMI circuit packs.

#### POWER UNIT

3.08 The 494LA power unit supplies the necessary +5 and +12 volts for proper operation of the circuit packs. Each group (FS 1, FS 2) has its own power unit.

#### REMOTE POWER CONTROL AND DISPLAY

3.09 The power control and display circuit (SN516, TN1077, or TN1077B), located in the associated host switch module, conveys the status of an FIU/DLI group. It contains switches to power up and power down an FIU/DLI group. It also has a switch to request a group out-of-service. These switches and associated LED indicators provide craft interface for that service group located in the DLI unit.

### SECTION II - DETAILED DESCRIPTION

#### 1. FACILITY INTERFACE CIRCUIT (FS 1, FS 2)

##### GENERAL

1.01 Because FS 1 and FS 2 are similar, only one FS is described. FS 1 is group/side 0 and FS 2 is group/side 1. The term "both sides" means FS 1 (group/side 0) and FS 2 (group/side 1).

##### DUAL LINK MUX INTERFACE

1.02 A TN1510 circuit pack has two link interfaces (LI) on board. The CLK-CNT circuit on the TN618 pack control the TN1510 pack. The LI takes data from the MUX output bus and forms a network control and timing (NCT) link.

1.03 The LI in a DLMI also receives the NCT link signal output from the TSIU, recovers data, and performs

frame synchronization. The resultant data are written into a variable-length "first in-first out" (FIFO) buffer that is used to synchronize the timeslot of the data output to the MUX.

1.04 To form the NCT link signal, the LI in a DLMI takes data word nibbles from the MUX output bus, and after checking for odd parity across each word, forms the NCT link signal by inserting a framing pattern, scrambling the resulting data, and then outputting it serially at 32.768 MHz to the DLI in the TSIU.

1.05 The DLMI receives the NCT link signal output from the DLI and recovers a receive clock from transitions in the data stream. It then descrambles the data and performs frame synchronization. The resultant data is written into a variable length FIFO buffer that is used to synchronize the time-slot of the data output to the MUX, so that it is the same as the time-slot of the data input from the MUX. The receive data word parity is checked and then regenerated by the DLMI before it is outputted in nibbles to the MUX. This parity check and generation can be used to provide a known data pattern for testing a DLMI when the MUX has been set into the DLMI data loopback mode of operation.

1.06 Timing signals are required for the DLMI to transmit data to the TSIU and also to align the transmit and receive data timeslots at the MUX interface. These signals are generated from a 32-MHz clock, a 2-MHz synchronization pulse stream, and a time-slot count, produced by the CLK-CNT circuit pack. These signals are phase-locked to the receive T1 clock frequency of one of the DFIs so that the derived timing within the TSIU is identical to that of the host office, thereby eliminating facility framing slips. The CLK-CNT subunit

also provides each DLMI with a CONTROL REGISTER and shares an ERROR REGISTER between them. Both registers can be accessed by the MP through the active PCC.

1.07 The DLMIs provide several features for diagnostic purposes. By writing to the DLMI CONTROL REGISTER, a specific DLMI can be configured to send idle code, disable framing sequence, invert transmit parity, invert receiver parity, loop, and place the associated error register into a test mode.

1.08 The NCT link data stream of each DLMI can be looped back to its own receiver to isolate a framing or data parity error to either the DLMI in the T1 FIU, the NCT link, or the DLMI of the DLMI. When this loopback occurs, the LOOP bit is set (one) in the ERROR REGISTER for the appropriate DLMI. Thus the MP cannot "forget" that it has placed the DLMI into this test state.

1.09 While the DLMI is looped back, the associated MUX must also be placed into the DLMI data loopback mode while the DLMI forces idle code to be sent towards the MUX. This sends the DLMI a known signal for use during the data loop test. Note that the MUX loops the idle code back towards the DLMI without checking or regenerating the parity of the data words. A further test of the data processing capabilities of the DLMI is obtained by having the MP insert a test pattern at the TSI while the MUX loops this data back through the DLMI, and then testing that data at the TSI.

#### CLOCK-CONTROL

1.10 The CLOCK-CONTROL (CLK-CNT) circuit pack (TN618) provides timing, control distribution, and an interface through two PCCs to both MP

sides for all circuit packs of the FIU. Timing is also transmitted to the TSIU of the T1 RSM via the 32 MHz fiber optic links and then recovered from the fiber link data stream by the LI subunits in the TSIU.

#### A. Timing

1.11 Clock signals are derived from the output of a crystal oscillator used in a phase locked loop (PLL). Operating at the NCT link rate of 32,768 MHz, the oscillator output is used to generate various clocks, sync pulses, the time-slot count for the NCT link frame, and the frame bit sequence.

1.12 The PLL can be set to operate in either the master mode or the slave mode. In the master mode, a CLK-CNT circuit pack can be set either to select a digital facility interface (DFI) as the timing reference source or to free-run at the internal crystal oscillator frequency. In the slave mode, a CLK-CNT circuit pack is locked to the 8 MHz output of its mate. An interlock is provided so that at least one CLK-CNT circuit pack side is in the master mode.

#### B. Control Interface

1.13 Circuitry of the CLK-CNT circuit pack provides the interfaces to both module processor (MP) sides through peripheral control channels (PCCs). PCCs from the MPs terminate in fourteen control and error registers. One MUX CONTROL REGISTER and one MUX ERROR REGISTER reside on each MUX subunit, three registers reside on the CLK-CNT subunit, and nine registers reside on the DLMI subunit.

1.14 The control registers are both readable and writable. The error registers are latching and are cleared by a read operation, thereby removing the interrupt from that error register

for transient errors. If a hard fault exists, then the error interrupt remains. Any specific bit of an error register can be masked from causing an interrupt by writing a "1" to that bit. This action does not change the error register contents but does prevent the possible error condition from causing an interrupt.

1.15 The logical sense of an error register input can be reversed by writing a one to the INT TEST bit of the appropriate control register. This input reversal, when used in conjunction with individual bit interrupt masking, enables testing of the error registers.

#### C. DFI Interface

1.16 Each DFI subunit sends two signals via a bus to the CLK-CNT subunit. These are T1 CLOCK and T1 STATUS. The T1 clock signal is a 1.544 MHz (24 channel) or 2.048 MHz (30 channel) clock signal recovered by the DFI from its incoming T1 line; it can be used for synchronization to the network. The T1 STATUS signal is an indication of whether the T1 CLOCK signal is acceptable for use as the reference for synchronization.

#### D. Reset Function

1.17 An office switch module can be reset via central processor intervention (CPI), a process that is capable of handling multilevel resets.

#### MULTIPLEXER

1.18 The MULTIPLEXER (MUX) circuit (TN619/TN1039) provides a fixed time-slot mapping of data carried over ten facilities interface data buses (FIDBs) into a 256 time-slot format that is then converted to a NCT link signal by a DLMI subunit. Two MUX and LI pairs in a DLMI are used to provide

the A and B NCT links required for the proper operation of each side of the TSIU. Synchronization and clock signals for these conversions are provided by the CLK-CNT circuit pack.

1.19 The MUX also provides data parity test capabilities required to maintain portions of both the DFI and the DLMI interfaces. Errors in data parity are detected automatically and reported through the CLK-CNT circuit pack to the CI of the MCU. The MUX can also be directed to loop data from the DLMI or a particular FIDB back towards the TSIU for use in a diagnostic testing of the MUX and DLMI circuit packs.

1.20 The MUX is divided logically into five main sections: transmit data processing, peripheral interface, receive data processing, timing generation, and control distribution with error reporting.

#### POWER UNIT

1.21 The 494LA power unit is capable of delivering about 13 amperes at +5.0 volts. It has programmable current limiting via programming resistors located on each subunit. The value of each resistor is determined by the current requirements of the particular subunit. A second output voltage at +12.0 volts can supply 1 ampere and is regulated separately from the +5.0-volt output.

1.22 The power unit operates at about 50% of its load capacity with an expected efficiency of greater than 75%, supplying power to one side. This power unit requires operator interaction to start the unit once it has entered the off state. It can enter the off state by operator intervention or by detection of voltage and/or current excursions that exceed

preset limits. The unit must be started using its remote start feature via the power control and display (SN516, TN1077, or TN1077B) unit that is in the associated SM.

#### REMOTE POWER CONTROL AND DISPLAY

1.23 The power control and display circuit pack listed above conveys the status of a FIU/DLI group through the DLI in the SM. It contains switches to power up and power down a FIU/DLI group. It also has a switch to request a group out-of-service. These switches and the associated LED indicators provide a craft interface for that service group.

1.24 The CD circuit performs its functions via scan and distribute points that are read and written from the MP. It is powered directly by office battery and provides isolated interfaces to the scan and distribute unit through optical isolators.

The SN516, TN1077, and TN1077B packs have a face plate with four switches and five LEDs whose functions are as follows:

- (1) ON - A momentary pushbutton used to power up the FIU/DLI's side.
- (2) OFF - A momentary pushbutton used to power up the FIU/DLI side only if that side is out-of-service.
- (3) RST-ROS - A slide switch used to request a side either in service or out-of-service.
- (4) MOR - A momentary pushbutton manual override switch. Whenever it is simultaneously depressed with the OFF switch, power is turned off.
- (5) OFF - A red LED that lights whenever logic power is off.

- (6) ALM - A red LED that lights whenever a power fault occurs on the side (fuse or converter alarm). Once the side is powered down for repairs, the OFF LED lights, and the ALM LED extinguishes.
- (7) OOS - A yellow LED controlled by the MP; it is lit whenever the side is out of service.
- (8) RGIP - A green LED controlled by the MP; it lights whenever a request to restore or remove a unit has been received by the MP. If this request is denied, this LED flashes for 5 to 10 seconds.
- (9) ROS - A green LED that lights whenever the ROS/RST switch is in the ROS (request out-of-service) position.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Working limits for the individual circuits are in their respective schematic drawing circuit descriptions.

2. FUNCTIONAL DESIGNATIONS

2.01 Functional designations for the individual circuits are in their respective schematic drawing circuit descriptions.

3. FUNCTIONS

3.01 Function information for individual circuits are in their

respective schematic drawing circuit descriptions.

4. CONNECTING CIRCUITS

4.01 Connecting circuit information is provided in SD-5D401-02.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are provided in X-79970.

SECTION IV - REASONS FOR REISSUE

B. CHANGES IN APPARATUS

B.1 ADDED

OPTION 4 - ODL50 FIBER  
OPTIC CONNECTOR

D. DESCRIPTION OF CHANGES

D.1 The new ODL50 type fiber optic connectors are a cost reduction.

D.2 In CAD 1, element identifiers BR, BG, DB, DC reflect the addition of ground connections.

D.3 In the unit symbol table of contents, corrections were made to have the respective element with the corresponding NCT link.

D.4 In the information notes section, note 305 was added reflecting option x and y which list the appropriate circuit pack and generic.

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