5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH CONTROL UNIT
MODEL 3
CIRCUIT

Description of Changes

SD5D508-01 issue 3M corrects drawing errors introduced during issue 2B. 42 ground nets that did not exist in the circuit were removed. The text in the CD is not affected by this issue.

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4. REASONS FOR REISSUE

B. Changes in Apparatus

None.

D. Description of Changes

Dual serial channel (DSCH) identification (ID) codes were added to support the connection of the message switch control unit 3 (MSCU3) to the 3B21D.

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**5ESS® SWITCHING EQUIPMENT
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CONTENTS

LIST OF FIGURES

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The Message Switch Control Unit, model 3 (MSCU3) controls the message transfers between the Administration Module (AM), and as many as 14 peripheral control communities, each consisting of one to four peripheral controls. A Peripheral Controller (PC) can be a Module Message Processor (MMP), a Foundation Peripheral Control (FPC), a Pump Peripheral Controller (PPC), or a Communication Module Processor (CMP). The community with the FPC and PPC is limited to two PCs and is contained within the MSCU3. Message transfers are accomplished under control of a bit-slice processor on the Input/Output Processor 2 (IOP2)/Message Switch Control 3 (MSC3) circuit pack. The functions of the MSCU3 are as follows:

a. Perform the serial-to-parallel conversation of data received from the AM, and the parallel-to-serial conversation of data transmitted to the AM.

b. Provide one to four Input/Output Microprocessor Interfaces (IOMIs) to interface the IOP2/MSC3 with the MMPs, FPC, and PPC.

c. Provide control to transfer data between MMPs or between the AM and MMPs.

d. Provide control to transfer data between the AM and the FPC or PPC.

e. Perform self diagnostics resident in IOP2/MSC3 firmware.

f. Provide control and diagnostic access for the Dual Message Interface (DMI), the Network Clock (NCLK), and the Time Multiplexed Switch, model 2 (TMS2) via the FPC.

g. Provide a PPC for loading the Switch Module (SM) with data at a high rate (192k bytes/sec).

h. Provide both manual and AM control of the MSCU3 from an in-service/out-of-service point of view.

2. DETAILED DESCRIPTION

A description of each circuit pack in the MSCU3 (as seen in Fig. 1) can be found in this section.

2.1 INPUT OUTPUT PROCESSOR/MESSAGE SWITCH CONTROLLER (IOP2/MSC3)

The IOP2/MSC3 circuit pack combines functions that were contained on separate circuit packs in the MSCU2. The IOP2/MSC3 has the following functions:

- a. A Dual Serial Channel (DSCH) interface to the AM.

- b. A Duplex Dual Serial Bus Selector (DDSBS) interfaces the DSCH and Bit Sliced Processor (PIC) controller.

- c. PIC controls MSCU3 message transfer and diagnostic functions.

- d. Provides pumpable microcontrol store.

- e. Provides an on-board IOMI.

- f. Clock generation circuitry.

Three custom gate arrays provide a DDSBS, PIC, and IOMI functionality.

The DDSBS serves to interface the MSCU3 with the AM DSCH. All signaling is compatible with EIA standard RS422. Each DDSBS interfaces with the DSCH via connectorized cables, each of which consists of two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The data rate between the DDSBS and DSCH is at 10 MHz. The DDSBS also interfaces with the PIC which can read or write messages into DDSBS FIFO memory.

To specify the operation type, 4-bit start codes are transmitted to the DDSBS over the two bidirectional data leads. The DSCH issues one of the following seven different start codes to the DDSBS:

Start Codes	
33	Write data in the word mode.
35	Send device command.
39	Write data in the block mode.
53	Read data in the work mode.
55	Sense DDSBS status
59	Read data in the block mode.
93	End Of Transfer (EOT).

Similarly, the DDSBS issues one of the following four completion codes to the DSCH to specify the success or failure of the operation:

Completion Codes	
33	All seems well.
35	Device reported an error.
53	Invalid DDSBS command.
55	Illegal start code received.

The DDSBS receives and decodes the incoming serial message, executes the specified operation, and transmits the serial reply message back to the DSCH.

The DDSBS acts as a buffer between the 32-bit DSCH messages and the 16-bit PIC. Included in the DDSBS are a 16-word by 32-bit data FIFO, a 32-bit command register, a 32-bit status register, and a 16-bit sanity timer. The PIC can access each of these registers 16 bits at a time. The DDSBS buffers data and commands to the PIC, buffers data and status from the PIC, and performs the necessary hand shaking to communicate with the DSCH.

The FIFO can be accessed by both the PIC and DSCH but not at the same time. Parity checks over the transfers between the DSCH and DDSBS are always performed. Parity checks over transfers between the PIC and DDSBS may or may not be performed, depending on the state of an internal flag controlled by the PIC.

The command register records commands from the AM destined for the PIC. The PIC may read and, for maintenance purposes, may write this register.

The timer provided on the DDSBS is used to maintain the sanity of the MSCU3. The PIC has read/write access to the timer, which is incremented once every 5 microseconds. A timer interrupt is issued to the PIC at an interval specified in the initialization block from the maintenance software. The PIC has 30 mS to reset the timer, otherwise a sanity error bit will be set to report the detection of an error to the AM.

The DDSBS status register is segmented into 16 bits of status and 16 bits of error. Flags are used to request interrupt and Direct Memory Access (DMA) service from the AM, to alert the IOP2/MSC3 of the presence of an AM command or data requests, and to record the detection of error conditions.

The processor used on the IOP2/MSC3 consists of a custom gate array and bit-slice technology. The gate array PIC provides a microprogram sequencer, interrupt address generator, source and destination decoders, execution ram address counter, data bus control, Programmable Read-Only Memory (PROM) control and execution Random Access Memory (RAM) control.

A microprogram register provides a data latch for the microinstruction. This register contains all control information required to execute a single microinstruction.

The source and destination register decoders are used to decode 10 bits of microprogram register into the appropriate register input and output enable signals.

The Arithmetic Logic Unit (ALU) consists of four 4-bit sliced microprocessors. In addition, the ALU can perform two forms of subtraction and five logical operations.

A 16k by 16+2 parity bit RAM is equipped on the IOP2/MSC3 to be used as temporary data storage. Associated with the RAM is a 14-bit address sequencer that also provides auto increment function of memory addresses.

Fifteen vectored interrupt levels are incorporated by priority on the IOP2/MSC3. A 16-bit mask register is included to individually inhibit or enable selected levels. The MSCU3 interrupt assignments are shown below:

LEVEL 0   Unused - highest priority; unmaskable

LEVEL 1   Microword parity error

LEVEL 2   PIC instruction timer

LEVEL 3   DDSBS command flag, used to alert the PIC of the presence of a command from the AM awaiting execution.

LEVEL 4   IOMI-A PC Interrupt Request (PCIR) summary

LEVEL 5   IOMI-B PCIR summary

LEVEL 6   IOMI-C PCIR summary

LEVEL 7   IOMI-D PCIR summary

LEVEL 8   Unused

LEVEL 9   Unused

LEVEL 10   Unused

LEVEL 11   Unused

LEVEL 12   DDSBS sanity timer

LEVEL 13   IOMI parity error

LEVEL 14   Stop The World (STW)

The microprogram address sequencer provides full control capability to perform normal sequential execution of up to 64k words of microcontrol store. The sequencer also performs conditional and unconditional jumps for the following seven conditions:

    a. Carry.

    b. Overflow.

    c. Negative.

    d. Zero.

    e. DDSBS data flag.

    f. DDSBS error summary.

    g. PIC data ready.

The IOP2/MSC3 contains 16K by 48 bits of high speed Execution RAM (E-RAM) used by the PIC as microcontrol store, and 2K by 48 bits of boot PROM which contains MSCU3 firmware used to pump the E-RAM from the AM disk and to diagnose the MSCU3 hardware. The function of each bit, or series of bits within each 48-bit word, follows:

- Bits 0-35 form the instruction to be executed by the PIC.

- Bits 36-43 are used by the clock generator to determine the instruction execution speed of the microinstruction (instruction speeds cay vary from 100 ns to 300 ns in increments of 25 ns).

- Bits 44-47 are used by the PIC to check parity over the 48-bit word.

The on-board IOMI serves to interface the 16-bit PIC with up to four communities of 8-bit peripheral processors. The second community provides dedicated access to the FPC and PPC processors contained in the MSCU3 unit.

The interface between the PIC and on-board IOMIs consists of a 16+2 parity bit data bus, five source signals, and five destination signals for control of the IOMI.

All signals between the on-board IOMI and the Message Switch Peripheral (MSPU) processors are at TTL levels. Each community consists of a 16-bit DMA address bus, and 8+1 parity bit bidirectional data bus, eight control signals, and one out-of-level signal. Each of the four peripheral processors in each community has an individual Service Request (SR), Interrupt Request (IR), Error Request (ER), and Control Signal Acknowledge (CSA) signal.

2.2 INPUT OUTPUT MESSAGE INTERFACE

The MSCU3 can be equipped with up to three additional external IOMIs to provide 10 additional communities.

The interface between the PIC and external IOMIs consists of a 16+2 parity bit data bus, five source signals, and five destination signals for control of the IOMI.

All signals between the external IOMIs and the MSPUs are at TTL levels. Each community consists of a 16-bit DMA address bus, and 8+1 parity bit bidirectional data bus, eight control signals, and one out-of-level signal. Each of the four peripheral processors in each community has an individual SR, IR, ER, and CSA signal.

2.3 MESSAGE SWITCH PERIPHERAL PROCESSOR

The Message Switch Peripheral Processor (MSPP) is the controlling circuit pack of all message switch peripheral controller applications. The MSPP is a single-board processor with an interface through an IOMI bus to the IOP2/MSC3 as well as an interface to application boards needed for each particular function. Contained on the MSPP is a 16-bit microprocessor, 128K bytes of Dynamic Random Access Memory (DRAM), 8K bytes of static RAM, 16K bytes of Erasable Programmable Read Only Memory (EPROM), and clock circuits to ensure its own sanity and to provide needed timing to application boards.

The interface to the application boards supports either 8- or 16-bit peripherals. Through this interface, the MSPP performs parity generation and checking functions for both the data bus and address bus. DMA operations are also supported, allowing efficient data transfers without direct processor involvement.

2.4 FOUNDATION PERIPHERAL CONTROLLER

The FPC contains circuitry that peripherals the following functions:

a. Provides serial interface to the three subdevices over the Control and Diagnostic Access Link (CDAL). This interface is accomplished through a fixed hardware protocol provided by the Control and Diagnostic Access Circuit (CDAC). A PROM sequencer is used to provide the necessary control signals associated with the protocol.

b. Generates maskable interrupt control vectors to the MSPP upon reception of error or service requests from one of the three subdevices.

c. Selects the active CDAL (0 or 1).

d. Checks parity of address and data received from the MSPP, and generates parity over the data bus during data transfers to the MSPP.

On the MSPP microprocessor bus interface, the FPC receives address, address parity, data, data parity, various control signals. The FPC sends data, data parity, and control signals to the MSPP on this bus.

On the CDAL interface, the FPC sends and receives serial data and control signals.

2.5 PUMP PERIPHERAL CONTROLLER

The PPC provides the interface for rapid pumping on the SM. Data is pumped from the disk in the AM, through the IOP2/MSC3, to the PPC through the on-board IOMI bus. The PPC then sends the data to the Communication Module Control Unit (CMCU) through a Message Interface Bus (MIB). The CMCU sends it to the TMS2, where it is distributed to the destination SM through a Network Control and Timing (NCT) link.

PPC contains circuitry which performs the following functions:

   a. A pair of 4k byte RAM buffers temporarily store blocks of data written by the MSPP.

   b. An 11-bit word counter generates the RAM buffer address during reads (transmissions to the switch module). An address multiplexer switches the source of the RAM buffer's address from the address counter to the processor's address bus.

   c. A data formatting circuit converts the 16-bit words read from the RAM buffer to 8-bit time slots. Each time slot contains six data bits, a framing bit, and a parity bit.

   d. An 8-bit time slot counter has two functions: it counts the eight bits per time slot and the 32 time slots per frame.

   e. The output data circuit contains a multiplexer that switches idle code or data to the output. A shift register converts the parallel data to serial data, which is outputted on the MIB at a 2 MHz rate.

   f. A 32-by-1 bit RAM performs time-slot selection. Each bit corresponds to one of the 32 time slots and is used to determine which of the time slots will be used for data transmission during SM pump.

   g. Diagnostic circuits check data parity, address parity, data formatting, and the time-slot select RAM.

Data blocks are transferred in parallel format from the MSPP to the PPC. This interface contains a 16-bit address bus, 16-bit data bus, and various control signals.

Data blocks are transferred in serial format from the PPC to the DMI on the MIB. This interface contains transmitted data, received data, received data, and 4 MHz clock and sync signals. The maximum data transfer rate is 192k bytes/second.

2.6 CONTROL AND DISPLAY

In service/Out-Of-Service (OOS) control, and alarming of the power converters is performed by Control and Display (C&D) circuit packs. The MSCU3 incorporates two C&D packs (Fig. 1). One provides manual and AM control of the FPC, PPC, and their associated MSPPs; the other provides manual and AM control of the IOP2/MSC3, and the IOMIs. The AM monitors the C&D packs for fuse alarms, power status (alarms, manual off, and power on), and request for OOS.

2.7 495FB POWER CONVERTER

The purpose of the converter is to change a nominal -48 volt input to a well regulated +5 volt output for applications in the MSCU3 circuits. The power unit is pulse-width controlled for regulation, is self-oscillating, and operates at a fixed frequency. The 495FB provides +5 volts at 250 watts. The MSCU3 incorporates two converters (Fig. 1). One provides power for the FPC, PPC, and their associated MSPPs; the other provides power for the IOP2/MSC3, and the IOMIs.

3. REFERENCE DATA

3.1 CIRCUIT PACKS

Circuit pack CDs reside within the following Circuit Pack Schematics (CPSs).

    a. IOP2/MSC3 - CPS KBN10.

    b. Input Output Microprocessor Interface (IOMI) - CPS UN25B.

    c. Power Converter - CPS 495FB.

    d. Control and Display (C&D) - CPS SN516B.

    e. Foundation Peripheral Controller (FPC) - CPS UN173.

    f. Pump Peripheral Controller (PPC) - CPS TN886.

    g. Message Switch Peripheral Processor (MSPP) - CPS TN856C.

3.2 CONNECTING CIRCUITS

    1.   Message Switch Peripheral Unit, Model 3 (MSPU3) - SD-5D078-01.

    2.   CMCU - SD-5D060-01.

    3.   Fuse/filter panel - SD-5D084-01.

    4.   Input Output Processor (IOP) - SD-4C101-01.

    5.   DSCH - SD-4C099-01.

3.3 WORKING LIMITS

Voltages		
Nominal	Minimum	Maximum
-48 volts	-42.75 volts	-52.5 volts

Ambient Temperature	
Maximum air temperature at frame outlet	2 to 70 degrees Celsius
Aisle ambient at fan inlet	2 to 50 degrees Celsius

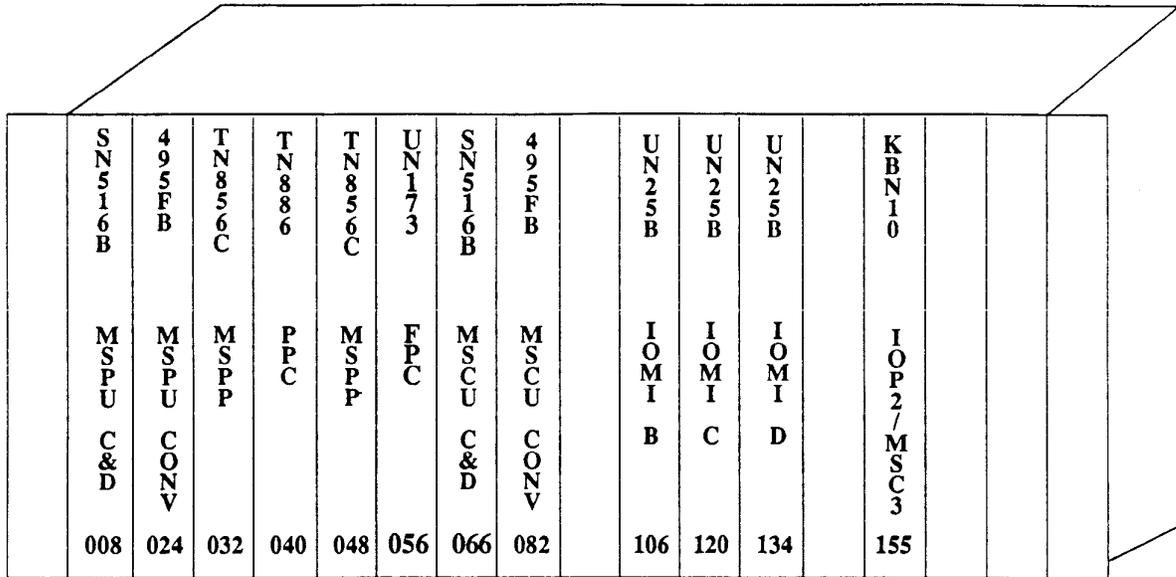| S N 5 1 6 B	4 9 5 F B	T N 8 5 6 C	T N 8 8 6	T N 8 5 6 C	U N 1 7 3	S N 5 1 6 B	4 9 5 F B		U N 2 5 B	U N 2 5 B	U N 2 5 B		K B N 1 0			
M S P U C & D	M S P U C O N V	M S P P	P P C	M S P P	F P C	M S C U C & D	M S C U C O N V		I O M I B	I O M I C	I O M I D		I O P 2 / M S C 3			
008	024	032	040	048	056	066	082		106	120	134		155			

Figure 1. Message Switch Control Unit, Model 3, Layout of Circuit Packs

4. ACRONYMS

ALU   - Arithmetic Logic Unit
AM   - Administration Module
C&D   - Control and Display
CD   - Circuit Description
CDAC   - Control and Diagnostic Access Circuit
CDAL   - Control and Diagnostic Access Link
CMCU   - Communication Module Control Unit
CMP   - Communication Module Processor
CPS   - Circuit Pack Schematics
CSA   - Control Signal Acknowledge
DDSBS - Duplex Dual Serial Bus Selector
DMA   - Direct Memory Access
DMI   - Dual Message Interface
DRAM   - Dynamic Random Access Memory
DSCH   - Dual Serial CHannel
E-RAM - Execution-RAM
EOT   - End Of Transfer
EPROM - Erasable Programmable Read-Only Memory
ER   - Error Request
FIFO   - First In First Out
FPC   - Foundation Peripheral Control
IOMI   - Input/Output Microprocessor Interfaces
IOP2   - Input/Output Processor 2
IOP   - Input/Output Processor
IR   - Interrupt Request
MIB   - Message Interface Bus
MMP   - Module Message Processor
MSC3   - Message Switch Control 3
MSCU3 - Message Switch Control Unit model 3
MSPP   - Message Switch Peripheral Processor
MSPU   - Message Switch Peripheral Unit
NCLK   - Network CLocK
NCT   - Network Control and Timing
OOS   - Out of Service
PC   - Peripheral Controller
PCIR   - PC Interrupt Request
PIC   - Bit Sliced Processor
PPC   - Pump Peripheral Controller
PROM   - Programmable Read-Only Memory

RAM - Random Access Memory
SD - Schematic Drawing
SM - Switching Module
SR - Service Request
STW - Stop The World
TMS2 - Time Multiplexed Switch, model 2

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