5ESS® SWITCHING SYSTEMS
COMMUNICATIONS MODULE UNIT
CIRCUIT

Description of Changes

Two new NCLK2 packs were added to the CMU for 64Kb/s applications. The TN1850 reference interface pack and the TN1851 NCLK2 controller. Sections 2.7.1, 2.7.3, and 2.7.4 were updated to include details on the new packs.

2.7.1 GENERAL HARDWARE DESCRIPTION

The NCLK2 consists of three fundamental circuit pack types: a controller (TN1276 or TN1851 for 64Kb/s applications), an oscillator (TN1283B, TN1284B, TN1285B, or TN1286B), and a reference interface (TN1274B, TN1275B, or TN1850 for 64Kb/s applications).

One NCLK2 oscillator circuit pack is required in each CMU shelf, as follows:

(a) TN1283B - 30-channel, high-stability, for international gateway and toll switches.

(b) TN1284B - 24-channel, high-stability, stratum 2, for toll switches in the United States (U.S.) and compatible countries.

(c) TN1285B - 30-channel, medium-stability. for international local switches.

(d) TN1286B - 24-channel, medium-stability, stratum 3, for local switches in the U.S. and compatible countries.

The reference interface circuit pack (TN1274B) is required for 24-channel digital carrier (DS-1) synchronization. This provides a maximum of one analog input and two digital inputs in any combination. A maximum of one TN1274B may be used in each CMU.

The reference interface circuit pack (TN1275B) is required for 30-channel digital carrier export synchronization. One TN1275B provides one analog input and four digital inputs with the restriction that a maximum of four of the five inputs be used simultaneously. A maximum of one TN1275B may be used in each CMU.

The reference interface circuit pack (TN1850) is required for 64Kb/s composite digital reference. One TN1850 provides two 64Kb/s digital references. A maximum of one TN1850 may be used in each CMU.

Analog references are restricted as follows:

(a) TN1274B - Basic Synchronization Reference Frequency (BSRF) of 2.048MHz* with an input level of -27 dbm* to +10 dbm* into 75 ohms.

(b) TN1275B - Frequency of 2.048 MHz* with an input level of -13 dbm* to +10 dbm* into 75 ohms.

2.7.3 NCLK2 CONTROLLER (TN1276 or TN1851)

The TN1276 circuit pack used for 30-channel and 24-channel reference applications or the TN1851 circuit pack used for 64Kb/s reference applications perform several NCLK2 functions. Being the controller for the NCLK2, the TN1276 or TN1851 handles communication with the FPC. It also contains a DELL and performs calculations to vary the output frequency of the clock. The controller also diagnoses NCLK2 functions under control of the FPC.

The TN1276 or TN1851 compares one external reference to the signal from the NCLK2 oscillator. The controller then calculates a frequency difference. This difference information is then used to control the DPLL. By keeping the DPLL locked to the very stable NCLK2 oscillator and not directly to the external reference, high degrees of NCLK2 stability are possible.

The DPLL provides the clock signal from which all TMS timing pulses are derived. It also provides a cross-coupled output to the NCLK2 on the opposite side. Normal operation is for one NCLK2 to be active-major providing timing signals to the TMS fabric and its associated link interfaces. The other NCLK2 is active-minor and is synchronized to the active-major side through cross-coupling, preventing errors in the 5ESS® Switch network when active-major and active-minor clocks are switched.

The DPLL can be operated in four different modes: normal, fast, holdover, and free run. In the normal mode, the DPLL attempts to track the external references using the normal time constants for that particular application. In the fast mode, time constants are reduced to achieve a fast lock condition in the NCLK2. The holdover mode is entered whenever problems with the external references are detected. Here, the DPLL is no longer locked to the external references; instead, its signal is based on the last known good reference. In the free mode, DPLL is instructed to free run in the center of its range. This is normally used only when the NCLK2 is initialized with no external references, or for stand-alone operation.

2.7.4 NCLK2 REFERENCE INTERFACE (TN1274B, TN1275B, or TN1850)

As previously stated, the NCLK2 locks to external reference signals connected to the TN1274B, TN1275B, or TN1850 circuit packs. Timing information is extracted from the reference signal and is sent to the DPLL on the controller circuit pack.

The DPLL then generates the required 8KHz timing signal (locked to the reference) for use by the TMS. For a master/slave network, where several references are used, the DPLL will lock to one of the external references. If that reference fails, the DPLL will be told to use the backup reference. If all external references are corrupted or lost, the DPLL will continue to provide the 8KHz to the TMS. In this holdover mode, the phase of the output signal is based on the last known good state of the reference. The stability of the clock during holdover will depend on the stability of the local NCLK2 oscillator.

5ESS® SWITCHING SYSTEMS
COMMUNICATIONS MODULE UNIT
CIRCUIT

Description of Changes

SD5D513-01 was changed to correct documentation errors in the notes. CD section DETAILED DESCRIPTION 2.10 is updated to include information on auto power recovery (APR). CD section REFERENCE DATA 3.4 is updated to include APR.

2.10 CONTROL AND DISPLAY (SN516B)

In service/out-of-service control, and alarming of the power converters are performed by the SN516 control and display (C&D) circuit pack. The pack provides manual and AM control of everything in the CMU except the NCLK2 oscillator pack. The AM monitors the C&D pack for fuse alarms, power status (alarms, manual off, and power on), and request for out of service (OOS). The C&D pack is wired through the CMU backplane for unit auto power recovery (APR). This allows the C&D pack to automatically power up the power converter if -48 volts to the unit is lost and then restored.

3.4 FUNCTIONAL DESIGNATIONS

APR	Auto Power Recovery

AT&T BELL LABORATORIES

DEPT NA5360100-RMW-JBC

CIRCUIT DESCRIPTION

CD-5D513-01
ISSUE 1
APPENDIX 2M
DWG ISSUE 3M
DISTN CODE BT13

5ESS® SWITCHING SYSTEMS COMMUNICATIONS MODULE UNIT CIRCUIT

Description of Changes

SD5D513-01 was changed to correct documentation errors in the DSCH backplane wiring and apparatus figures. Apparatus figures 14 and 15 providing NCT link optics were added, and apparatus figures 3, 4, 12 and 13 were corrected. Information notes 302 and 305 were changed to incorporate the apparatus figure and DSCH corrections. The text in the CD was not affected by this issue.

AT&T BELL LABORATORIES

DEPT NA5360100-RMW-JBC

5ESS® SWITCHING SYSTEMS COMMUNICATIONS MODULE UNIT CIRCUIT

Description of Changes

SD5D513-01 was changed to provide the correct DSCH backplane wiring for channels 12 and 14 to allow connection to the 3B21D. Notes 302 and 305 in the SD were changed. The text in the CD is not affected by this issue.

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DEPT NA5360100-RMW-JBC

5ESS® SWITCHING SYSTEMS
COMMUNICATIONS MODULE UNIT
CIRCUIT

CONTENTS

LIST OF FIGURES

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The communication module unit, or CMU, is a key component of the small office 5ESS® switch. The CMU can be used in offices having no more than two switching modules (SMs), one of which can be an SM-2000. The CMU has the following purposes:

- Supplying a clock to the office that is synchronized to external references.
- Providing central processor intervention (CPI), to force SMs into a known state.
- Pumping the SMs.
- Routing of BX.25 messages to the administrative module (AM) from an SM, or from the AM to an SM, or between SMs.
- Routing data or (PCM) voice between SMs.
- Providing an interface from the message switch controller (MSC) to a communication module processor (CMP).

To provide these functions, the CMU consists of eight main components: the message switch controller, the foundation peripheral controller (FPC), the pump peripheral controller (PPC), the message module processor (MMP), the message interface, the network clock model 2 (NCLK2), the time multiplexed switch controller (TMSC), and the time multiplexed switch (TMS).

1.2 GENERAL DESCRIPTION OF OPERATION

1.2.1 MESSAGE SWITCH CONTROLLER

The message switch controller is the heart of the message switch. It resides functionally between the AM, and the message switch peripherals, which can be MMPs, FPCs or PPCs, located in the CMU, or CMPs, located in another unit. The message switch controller communicates through the dual serial channel to the AM, and through the input-output microprocessor interface (IOMI) bus to the peripherals.

1.2.2 FOUNDATION PERIPHERAL CONTROLLER

The FPC provides control and diagnostic access to those function blocks in the CMU that are not directly controlled by the message switch controller: the network clock, the message interface, and the TMS.

1.2.3 PUMP PERIPHERAL CONTROLLER

The PPC is used to pump the SMs. Pump data is received by the PPC from the message switch controller and is temporarily stored in buffer memories in the PPC. Under software control, the PPC transmits the data, on as many as 32 time slots to the Message Interface.

1.2.4 MESSAGE MODULE PROCESSOR

The MMP contains eight X.25 protocol controller (XPC-8) chips that implement the level 2 data link control functions specified in the BX.25 packet switching communications standard. Each of the eight XPC-8 chips services one time slot. These time slots carry control information between SMs or between the AM and the SM.

1.2.5 MESSAGE INTERFACE

The message interface provides the interface between the time multiplexed switch and the MMPs and PPCs of the message switch. Every time slot, the message interface sets up a connection between the TMS and the appropriate message switch peripheral. The message interface can also insert the CPI code on one time slot or all time slots, to force an SM into a known state. The message interface also provides the FPC with control access, through the control and diagnostic access link (CDAL) to the network clock and TMS controller, as well as the message interface itself.

1.2.6 NETWORK CLOCK, MODEL 2

The NCLK2 provides timing and synchronization signals to the 5ESS® Switch network. This allows the 5ESS® Switch to be synchronized with the digital network that it connects to. In synchronized mode, the NCLK2 derives this timing signal from designated external reference facilities, thereby locking the 5ESS® Switch network to these reference facilities. NCLK2 provides high-stability or medium-stability operation, and interfaces to multiple 24-channel and 30-channel digital references, as well as to analog references. The network clock is a duplex circuit; that is, it is fully duplicated in each CMU shelf with some signals cross-coupled between the two sides.

1.2.7 TIME MULTIPLEXED SWITCH CONTROLLER

The TMSC consists of two circuit packs: TN1813 (controller), and TN1812 (clock and control interface).

TN1813 and TN1812 provide the control interface and environment necessary for the TMS firmware to execute call processing. These boards also handle maintenance orders from the AM and perform TMS internal operations (error reporting, initialization, reinitialization, etc.).

The TN1812 contains a high-frequency phase-locked loop that is locked to the network clock reference. It provides the clock signal and sync pulse to the switching module link interface pack (TN1830) and a clock signal to the TN1813 controller.

1.2.8 TIME MULTIPLEXED SWITCH

The CMU is connected to the SMs through 32Mbps network control and timing (NCT) links which terminate on the TN1830 boards.

Data received from the NCT links is switched through the TMS fabric multiplexers and either routed back to the appropriate SM through an outgoing NCT link, or to the message switch through the message interface.

2. DETAILED DESCRIPTION

A description of each circuit pack in the CMU can be found in this section. Refer to Figure 1 for a view of the unit layout.

2.1 MESSAGE SWITCH CONTROLLER (KBN10)

The KBN10 interfaces the CMU with the AM dual serial channel (DSCH). Each DSCH link consists of five RS-422 compatible cables, carrying two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The data is sent across the link as either a single 32-bit word or in a block of 16 32-bit words. The high order 16 bits of the 32-bit word are sent over one of the data leads and the low order 16 bits are sent over the other, least significant bit first, in parallel. The data rate between the KBN10 and DSCH is at 10 MHz.

To specify the operation type, 4-bit start codes are transmitted to the KBN10 over the two bidirectional data leads.

The KBN10 receives and decodes the incoming serial message, executes the specified operation, and transmits a serial reply message back to the AM.

Communication between the AM and the KBN10's on-board 16-bit processor takes place through a 16-word by 32-bit data first-in first-out (FIFO), a 32-bit command register, a 32-bit status register, and a 16-bit sanity timer.

The FIFO can be accessed by both the processor and the AM, but not at the same time. A single word or a block of 16 words can be stored in the FIFO.

The command register records commands from the AM destined for the KBN10. The processor may read and, for maintenance purposes, may write this register.

The timer is used to maintain the sanity of the KBN10. The processor has read/write access to the timer, which is incremented once every five microseconds. A timer interrupt is issued to the processor at an interval specified in the initialization block from the maintenance software. The processor has 81.92 ms to reset the timer; otherwise, a sanity error bit will be set to report the detection of an error to the AM.

The status register is segmented into 16 status flags and 16 error flags. These flags are used to request interrupt and direct memory access (DMA) service from the AM, to alert the processor to the presence of an AM command or data requests, and to record the detection of error conditions.

The processor used on the KBN10 consists of four 4-bit sliced microprocessors. These bit-slices work together to form a 16-bit microprocessor.

A 48-bit microcode word stored in the on-board microcontrol store controls the operation of the processor. This microword instructs the processor to move and operate on data. When reset, the KBN10 begins executing out of the on-board 1K-deep boot programmable read only memory (PROM) which instructs the KBN10 to download the 15K-deep execution random access memory (RAM) from the AM through the DSCH. Helper code used by diagnostics is also contained in the boot PROM. This same microword also controls the operation of the KBN10's microprogram sequencer. This sequencer controls all microprogram jumps, returns, and loops.

Interrupt vectoring circuitry on the KBN10 allows branching to interrupt handling routines. This circuitry automatically forces the program to branch to an interrupt vector table stored in the microcontrol store and to push the correct return address onto its stack.

On-board RAM allows for temporary storage of data passing through the KBN10. On-board registers allow the KBN10 to interface with the AM and with message switch peripheral processors (MSPPs)

The IOMI bus between the KBN10 and the MSPPs is at transistor-transistor logic (TTL) levels. Each community has a 16-bit DMA address bus, an 8+1 parity bit bidirectional data bus, eight control signals, and one out-of-level signal. Each of the peripheral processors in each community has an individual service request (SR), interrupt request (IR), error request (ER), and control signal acknowledge (CSA) signals.

2.2 MESSAGE SWITCH PERIPHERAL PROCESSOR (TN856C)

The MSPP is the controlling circuit pack of all message switch peripheral controller applications in the CMU. The MSPP is a single-board processor with an interface through an IOMI bus to the KBN10, and with an interface to application boards needed for each particular function. Contained on the MSPP is a 16-bit microprocessor, 128k bytes of dynamic random access memory (DRAM), 8k bytes of static RAM, 16k bytes of erasable programmable read only memory (EPROM), and clock circuits to ensure its own sanity as well as to provide needed timing to application boards.

The interface to the application boards supports either 8-bit or 16-bit peripherals. Through this interface, the MSPP performs parity generation and checking functions for both the data bus and address bus. DMA operations are also supported, allowing efficient data transfers without direct processor involvement.

2.3 FOUNDATION PERIPHERAL CONTROLLER (UN173)

The FPC contains circuitry that performs the following functions:

(a) Provides a serial interface to the three subdevices (network clock, message interface, and time multiplexed switch) over the CDAL. This interface is accomplished through a fixed hardware protocol provided by the control and diagnostic access circuit. A PROM sequencer is used to provide the necessary control signals associated with the protocol.

(b) Generates maskable interrupt control vectors to the MSPP upon reception of error or service requests from one of the three subdevices.

(c) Selects the active CDAL (0 or 1).

(d) Checks parity of address and data received from the MSPP, and generates parity over the data bus during data transfers to the MSPP.

On the MSPP microprocessor bus interface, the FPC receives address, address parity, data, data parity, and various control signals. The FPC sends data, data parity, and control signals to the MSPP on this bus.

On the CDAL interface, the FPC sends and receives serial data and control signals.

2.4 PUMP PERIPHERAL CONTROLLER (TN886)

The PPC provides the interface for rapidly pumping an SM. Data is pumped from the disk in the AM, through the KBN10, by way of the IOMI bus to the PPC. The PPC then sends the data to the message interface device (MI device) through a message interface bus (MIB). The message interface device sends it to the TMS, where it is distributed to the destination SM through an NCT link.

The PPC contains circuitry which performs the following functions:

(a) A pair of 4k byte RAM buffers temporarily store blocks of data written by the MSPP.

(b) An 11-bit word counter generates the RAM buffer address during reads (transmissions to the switch module). An address multiplexer switches the source of the RAM buffer's address from the address counter to the processor's address bus.

(c) A data formatting circuit converts the 16-bit words read from the RAM buffer to 8-bit time slots. Each time slot contains six data bits, a framing bit, and a parity bit.

(d) An 8-bit time slot counter has two functions: it counts the eight bits per time slot and the 32 time slots per frame.

(e) The output data circuit contains a multiplexer that switches idle code or data to the output. A shift register converts the parallel data to serial data, which is output on the MIB at a 2 MHz rate.

(f) A 32x1 bit RAM performs time-slot selection. Each bit corresponds to one of the 32 time slots and is used to determine which of the time slots will be used for data transmission during SM pump.

(g) Diagnostic circuits check data parity, address parity, data formatting, and the time-slot select RAM.

Data blocks are transferred in parallel format from the MSPP to the PPC. This interface contains a 16-bit address bus, 16-bit data bus, and various control signals.

Data blocks are transferred in serial format from the PPC to the MI device through the MIB. This interface contains transmitted data, received data, and 4 MHz clock and sync signals. The maximum data transfer rate is 192K bytes per second.

2.5 MESSAGE MODULE PROCESSOR (TN870)

The MMP contains the custom protocol chips (XPC8s) and the complementary metal oxide semiconductor (CMOS) MIB controller (CMC) chip for selecting eight transmit and eight receive time slots on the MIB. This board provide multiplexing between the 2Mb/s MIB serial rate and the 48Kb/s XPC serial rate, with parity insertion and checking on the MIB. It is controlled through the MSPP's microprocessor address, data, and control buses.

Through multiplexers here, and in the SM, dedicated links are supported by this board between the MMP and the SMs. The XPC chips process messages according to strict interpretation of level 2 BX.25 protocol. The XPC chip's interfaces to the system are through a duplex 48KB/s serial port to the MIB multiplexing circuitry, and an internal dual channel DMA controller which accesses memory on the MSPP board. The dual access memory (DAM) of the TN856C acts as the interface buffer between the processor on the KBN10 and the MSPP.

The MSPP receives messages destined for the SM in DAM, transfers it to dynamic RAM, and writes an XPC lookup table (also in dynamic RAM). The XPC chip makes use of pointer and message length information in the lookup table to program its internal DMA controller. The XPC chip then transfers the message into dynamic RAM. Messages traveling in the reverse direction are handled similarly.

The CMC chip provides the interface from the MIBs to the XPCs. This interfacing function consists of multiplexing and demultiplexing between the 2.048Mb/s MIB serial data rate and the 48 Kb/s XPC serial data rate, with parity checking and generation over both the transmit and receive portions of the interface. It provides access to eight transmit and eight receive time slots to and from the MIB.

In the single MMP configuration, there is only one MMP (and its associated MSPP) per side. The even-numbered control time slots are processed by the MMP on side 0 and the odd-numbered control time slots are processed by the MMP on side 1. In the dual MMP configuration, there are two MMPs per side, and both the odd- and even-numbered time slots are processed by both sides.

2.6 MESSAGE INTERFACE

2.6.1 GENERAL DESCRIPTION

The message interface consists of the control pack UN187 and the MI device and supporting circuitry on the TN1830. A maximum of 128 control time slots are transferred through the MI device. The UN187 controls the operation of the MI device.

2.6.2 MESSAGE INTERFACE DEVICE (PART OF TN1830)

In the transmit direction, the MI device sends clock, synchronization, and data from the TMS fabric to the message switch. The MI device demultiplexes a 32MHz data stream to four 4MHz data streams (half of the incoming data stream is discarded) for the peripheral controllers (PCs) in the message switch.

The MI device also supplies the TMS with data from four cross-coupled communities of PCs in the message switch. The MI device receives balanced serial data from the PCs through the MIB.

The MI device has eight serial input buses. Two buses are associated with each MIB. Four of these buses are associated with PCs on the same message switch side and four are associated with PCs on the cross-coupled message switch side.

The MI device has the capability to detect input parity errors from the PCs and the TMS and can force incorrect parity to the PCs and the TMS. The MI device can also force errors through control registers and detect them through (ESRs). This allows the MI device to verify its error detection circuitry.

2.6.3 MESSAGE INTERFACE CONTROLLER (UN187)

The UN187 is the control interface for the message interface complex. It provides the serial interface to the CDAL, which supplies a communication channel with either side of the FPC in the message switch. The UN187 uses its time slot switching memory to configure the data paths received from the PCs. It also can insert CPI in one or all time slots.

2.7 NETWORK CLOCK MODEL 2 HARDWARE DESCRIPTION

2.7.1 GENERAL HARDWARE DESCRIPTION

The NCLK2 consists of three fundamental circuit pack types: a controller (TN1276), an oscillator (TN1283B, TN1284B, TN1285B, or TN1286B), and a synchronizer (TN1274B or TN1275B).

One NCLK2 oscillator circuit pack is required in each CMU shelf, as follows:

(a) TN1283B - 30-channel, high-stability, for international gateway switches.

(b) TN1284B - 24-channel, high-stability, stratum 2, for toll switches in the United States (U.S.) and compatible countries.

(c) TN1285B - 30-channel, medium-stability, for international local switches.

(d) TN1286B - 24-channel, medium-stability, stratum 3, for local switches in the U.S. and compatible countries.

The synchronizer circuit pack (TN1274B) is required for 24-channel digital carrier (DS-1) synchronization.

This provides a maximum of one analog input and two digital inputs in any combination. A maximum of one TN1274B may be used in each CMU.

The synchronizer circuit pack (TN1275B) is required for 30-channel digital carrier export synchronization. One TN1275B provides one analog input and four digital inputs with the restriction that a maximum of four of the five inputs be used simultaneously. A maximum of one TN1275B may be used in each CMU.

Analog references are restricted as follows:

(a) TN1274B - Basic Synchronization Reference Frequency (BSRF) of 2.048MHz* with an input level of -27 dbm* to +10 dbm* into 75 ohms.

(b) TN1275B - Frequency of 2.048MHz* with an input level of -13 dbm* to +10 dbm* into 75 ohms.

2.7.2 NCLK2 OSCILLATOR (TN1283B, TN1284B, TN1285B, OR TN1286B)

The NCLK2 architecture uses a fixed frequency time base to perform its function of locking to the external references. The oscillator is oven-enclosed to provide high stability. Four different codes of oscillator circuit packs are provided for various combinations of domestic, export, high-stability, and medium-stability as described in section 2.7.1. Each NCLK2 oscillator is a unique failure group with independent power and alarms separate from other components in the CMU, including the NCLK2 reference and controller packs.

Each NCLK2 oscillator output (one in each CMU shelf) connects to both NCLK2 controllers (one in each CMU shelf). The digital phase locked loop (DPLL), on the controller circuit pack, is instructed through the maintenance software as to which clock to use as its time base.

For stand-alone applications, the NCLK2 will not be synchronized to any external reference facilities. Instead, the NCLK2 will serve as the master timing reference for the 5ESS® Switch. The stand-alone options are provided only for medium-stability applications.

2.7.3 NCLK2 CONTROLLER (TN1276)

The TN1276 circuit pack performs several NCLK2 functions. Being the controller for the NCLK2, TN1276 handles communication with the FPC. It also contains a DPLL and performs calculations to vary the output frequency of the clock. The controller also diagnoses NCLK2 functions under control of the FPC.

The TN1276 compares one external reference to the signal from the NCLK2 oscillator. The controller then calculates a frequency difference. This difference information is then used to control the DPLL. By keeping the DPLL locked to the very stable NCLK2 oscillator and not directly to the external reference, high degrees of NCLK2 stability are possible.

The DPLL provides the clock signal from which all TMS timing pulses are derived. It also provides a cross-coupled output to the NCLK2 on the opposite side. Normal operation is for one NCLK2 to be active-major providing timing signals to the TMS fabric and its associated link interfaces. The other NCLK2 is active-minor and is synchronized to the active-major side through cross-coupling, preventing

* Input frequency is determined by both hardware and firmware. Input level is dependent only on the hardware and is independent of firmware.

errors in the 5ESS® Switch network when active-major and active-minor clocks are switched.

The DPLL can be operated in four different modes: normal, fast, holdover, and free run. In the normal mode, the DPLL attempts to track the external references using the normal time constants for that particular application. In the fast mode, time constants are reduced to achieve a fast lock condition in the NCLK2. The holdover mode is entered whenever problems with the external references are detected. Here, the DPLL is no longer locked to the external references; instead, its signal is based on the last known good reference. In the free run mode, DPLL is instructed to free run in the center of its range. This is normally used only when the NCLK2 is initialized with no external references, or for stand-alone operation.

2.7.4 NCLK2 SYNCHRONIZER (TN1274B OR TN1275B)

As previously stated, the NCLK2 locks to external reference signals connected to the TN1274B or TN1275B circuit packs. Timing information is extracted from the reference signal and is sent to the DPLL on the controller circuit pack.

The DPLL then generates the required 8KHz timing signal (locked to the reference) for use by the TMS. For a master/slave network, where several references are used, the DPLL will lock to one of the external references. If that reference fails, the DPLL will be told to use the backup reference. If all external references are corrupted or lost, the DPLL will continue to provide the 8KHz to the TMS. In this holdover mode, the phase of the output signal is based on the last known good state of the reference. The stability of the clock during holdover will depend on the stability of the local NCLK2 oscillator.

2.8 TMS CONTROLLER

2.8.1 GENERAL DESCRIPTION

The TMS controller consists of two circuit packs: the TN1813 controller, and the TN1812 clock and control interface.

2.8.2 CONTROLLER (TN1813)

The TN1813 controller operates as a microprocessor-based core to maintain and set up the TMSC (TMS controller) and TMS.

The TN1813 consists of a 68000 microprocessor supported by 48 kbytes of static RAM, 64 kbytes of EPROM, a D71054 programmable timer, a 9519A programmable interrupt controller, maintenance and error source registers, and other circuitry for address decoding, data flow, and other, lower level functions.

The EPROM stores TMS firmware, including a bootstrap program that initializes the TMSC in response to a reset. The RAM stores these TMS firmware program variables and the TMS diagnostic program and its variables. Part of the RAM is dedicated to other diagnostic programs delivered from the message switch.

The D71054 programmable timer provides timing for regular interrupts to the 68000 processor and serves as its sanity timer.

The 9519A programmable interrupt controller provides a way to prioritize and allow or disallow TMS internal interrupt sources.

The error source registers provide maintenance and control functions on- and off-board.

The TN1813 connects to the TN1812 over a common parallel address, data and control bus. The TN1813 connects to the TN1830 through the TN1812.

2.8.3 CONTROL INTERFACE PART OF (TN1812)

The TN1812 control interface provides one end of the serial link that allows the TMSC to communicate with the TMS. The key component of the TN1812 control interface is the control interface (CI) device. This chip provides a transparent extension of the Motorola 68000 bus by converting the parallel address, data, and control leads of the microprocessor into two serial streams and sending them to the TN1830. In a similar way, the serial stream from the TN1830 is converted back into parallel and put on the microprocessor's own bus.

The CI device also interfaces to the CDAL, allowing the FPC to communicate with the TMS controller, through the UN187. This 1Mbps serial interface is used by the FPC to send initialization, maintenance, fault recovery, and call processing messages to the TMS.

Parity and other control interface errors detected by the TN1812 are reported to the TN1813.

2.8.4 CLOCK INTERFACE (PART OF TN1812)

The TN1812 provides system timing for the TMS through the generation of the various clocks and synchronization pulses, which are used by the TN1812, TN1813, and TN1830. System synchronization is accomplished by phase locking the oscillator on the TN1812 to an 8KHz reference signal from the network clock or from the cross-connected TN1812. Clock loss and clock frequency errors detected by the TN1812 are reported to the TN1813.

2.9 TIME MULTIPLEXED SWITCH (PART OF TN1830)

The TMS is implemented on the TN1830, which interfaces with the NCT links and consists of the following function blocks:

(a) Clock recoveries,

(b) Link interface receivers (LIRs),

(c) Test function,

(d) Fabric and fabric controllers,

(e) Quad link transmitters (QLTs),

(f) Common interface and control (CIC) circuitry,

The LIRs and QLTs are implemented in two QLI chips on the circuit pack. The test function controller, fabric and fabric controller, and most of the CIC circuitry is implemented in the on-board TMS device.

Since the TN1830 does not receive clock along with data over the NCT links, each of the four incoming links has a clock recovery to extract the 32MHz clock from the incoming 32Mbps data.

The incoming data from each link is loaded into that link's LIR, which searches the incoming data for a framing pattern, which it locks on to. Once the LIR is in frame, it transfers the incoming data into the link's 256 x 16 bit RAM. While the data from the various links will not be aligned with each other when they enter the LIRs, the RAM allows for enough buffering that the data from the different links can be aligned when they are read from the RAM. The LIR back end, which reads the RAMs, also checks for framing and parity errors.

The test function is used to generate idle code during normal operation, and to generate test patterns for diagnostics. The test function consists of an 8Kx9 RAM and a RAM controller. The 8K RAM is large enough to hold 16 frames of 256 time slots of 16-bit data. The RAM controller reads consecutive locations in the RAM, converts the data to a serial bit stream and presents the data to input port 0 of the fabric. A sync address register determines the time during the frame when each location is read.

The data that has been aligned by the LIR, along with the data from the test function RAM, is made available on input ports to the fabric. Here, the data is routed to whatever output ports are listening to that input. Since the fabric is re-configured during each time slot, each output port on the fabric is controlled by a 256-word-deep RAM containing 3 bits of data telling that output what input it should listen to during the given time slot. The fabric controller arbitrates the reads and writes of these RAMs.

After the data is switched by the fabric, it passes through a quad link transmitter (QLT). The QLT sets the framing bits to the appropriate values, sets the "E-bit", which indicates whether the time slot is idle or in use, and regenerates parity for the 16-bit word, before sending the data off the board over the outgoing NCT link.

If the data is being sent from the TMS to the message switch, it also passes through a link transmitter, before entering the MI device.

The CIC function of this board interfaces with the TMS controller to provide the controller with access to the registers and memories on the board.

2.10 CONTROL AND DISPLAY (SN516B)

In-service/out-of-service control, and alarming of the power converters are performed by the SN516B control and display (C&D) circuit pack. The pack provides manual and AM control of everything in the CMU except the NCLK2 oscillator pack. The AM monitors the C&D pack for fuse alarms, power status (alarms, manual off, and power on), and request for out-of-service (OOS).

2.11 POWER CONVERTER (410AA)

The purpose of the 410AA converter is to change a nominal -48 volt input to a well regulated +5 volt output for applications in the CMU circuits. The power unit is pulse-width controlled for regulation, self-oscillating, and operates at a fixed frequency. The 410AA provides +5 volts at 310 watts for all the packs in the same CMU shelf except the NCLK2 oscillator pack and the SN516B.

3. REFERENCE DATA

3.1 CIRCUIT PACKS

Circuit pack circuit descriptions (CDs) reside within the following circuit pack schematics (CPSs).

(a) Control and Display (C&D) - CPS SN516B.

(b) Power Converter - CPS 410AA.

(c) Message Switch Controller, Model 3 - CPS KBN10.

(d) Foundation Peripheral Controller (FPC) - CPS UN173.

(e) Pump Peripheral Controller (PPC) - CPS TN886.

(f) Message Switch Peripheral Processor (MSPP) - CPS TN856C.

(g) Message Module Processor (MMP) - CPS TN870.

(h) Message Interface Controller - CPS UN187.

(i) Network Clock Model 2 Oscillator - CPS TN1274B, CPS TN1275B.

(j) Network Clock Model 2 Reference Interface - CPS TN1283B, CPS TN1284B, CPS TN1285B, CPS TN1286B.

(k) Network Clock Model 2 DPLL/Controller - CPS TN1276.

(l) Clock and Control Interface (CCI) - CPS TN1812.

(m) TMS Controller (TMSC) - CPS TN1813.

(n) Switching Module Link Interface (SMLI) - CPS TN1830.

3.2 WORKING LIMITS

3.2.1 TEMPERATURE RANGE

- -5 to 55 degrees C office aisle ambient.
- 0 to 65 degrees C at NCLK2 circuit packs.
- 0 to 70 degrees C at all other circuit packs.

3.2.2 HUMIDITY RANGE

- 5 to 95 percent relative humidity.

3.2.3 VOLTAGE LIMITS

- -39.5 to -57.0 volts.

3.2.4 INTERFRAME CABLING REQUIREMENTS

- Maximum distance from 3B21D processor unit to CMU is 100 feet.
- Maximum distance from DSX to NCLK2 is 655 feet.
- Maximum distance from time slot interchange unit (TSIU) to CMU is 2000 feet.

3.3 CONNECTING CIRCUITS

(a) Modular Fuse/Filter Unit - SD-5D190-01.

(b) 3B21D Processor Unit - SD-4T011-1.

(c) Time Slot Interchange Unit, Model 2 - SD-5D045-01.

(d) Time Slot Interchange Unit, Model 4 - SD-5D196-01.

(e) Communication Module Processor Unit - SD-5D178-01.

3.4 FUNCTIONAL DESIGNATIONS

AM	Administrative Module
C&D	Control and Display
CD	Circuit Description
CDAL	Control and Diagnostic Access Link
CI	Control Interface
CIC	Common Interface and Control
CMC	CMOS Message Interface Bus Controller
CMOS	Complementary Metal Oxide Semiconductor
CMP	Communication Module Processor
CMU	Communication Module Unit
CPI	Central Processor Intervention
CPS	Circuit Pack Schematic
CSA	Control Signal Acknowledge
DAM	Dual Access Memory
DMA	Direct Memory Access
DPLL	Digital Phase Locked Loop
DRAM	Dynamic Random Access Memory
DSCH	Dual Serial Channel
EPROM	Erasable Programmable Read Only Memory
EQL	Equipment Location
ER	Error Request
ESR	Error Source Register
FIFO	First-In First-Out
FPC	Foundation Peripheral Controller
IOMI	Input-Output Microprocessor Interface
IR	Interrupt Request
LIR	Link Interface Receiver
MIB	Message Interface Bus
MMP	Message Module Processor
MSC	Message Switch Controller
MSPP	Message Switch Peripheral Processor
NCLK2	Network Clock, Model 2
NCT	Network Control and Timing
ONTCCOM	Office Network Timing Complex, Common
OOS	Out-Of-Service
PC	Peripheral Controller
PCM	Pulse Code Modulation

PPC	Pump Peripheral Controller
PROM	Programmable Read Only Memory
QLI	Quad Link Interface
QLT	Quad Link Transmitter
SM	Switching Module
SR	Service Request
TMS	Time Multiplexed Switch
TMSC	Time Multiplexed Switch Controller
TSIU	Time Slot Interchange Unit
TTL	Transistor-Transistor Logic
XPC	X.25 Protocol Controller

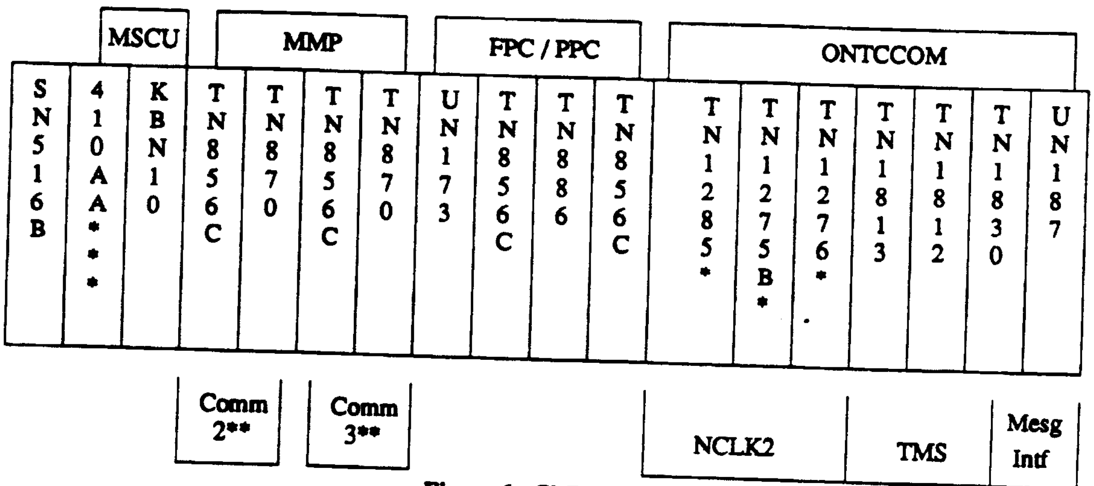

Figure 1. CMU Layout

* Only one possible way of equipping the network clock boards is shown here.

** On side 0, only community 2 will be equipped, and on side 1, only community 3 will be equipped, unless the switch has the dual MMP feature.

*** The power supply in side 0 of the CMU is equipped at a slightly different equipment location (EQL) than the power supply in side 1, to allow for better cooling of the power supplies.

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