5ESS® SWITCHING EQUIPMENT
PACKET SWITCH UNIT
MODEL 2

CONTENTS

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1. GENERAL DESCRIPTION

The Packet Switch Unit model 2 (PSU2) is a Switch Module (SM) peripheral unit, which provides the 5ESS switch the capability to manipulate packetized data, voice, and signaling messages. A PSU2 consists of a minimum of one equipment shelf, and a maximum of four growth shelves may be added to increase capacity.

1.1 PURPOSE OF CIRCUIT

PSU2 provides a generalized platform for processing packetized information of various types within the 5ESS switch. The PSU2 provides an array of processing elements to manipulate packet information. These hardware elements are called Protocol Handlers (PH), and the specific processing a PH performs is dependent on both the application and the specific PH circuit types configured in the unit. A maximum of 16 PHs, of various types, are supported on a single shelf. The addition of growth shelves allows a maximum of 80 PHs to be supported (i.e. 1 base shelf + 4 growth shelves).

In addition to PHs, PSU2 also provides circuits which allow initialization and control by the SM, provides inter PH and PH to SM communication, and provides communication links which support information exchange external to the SM.

Initial PSU2 applications include Code Division Multiple Access (CDMA) mobile telephone and Integrated Services Digital Network (ISDN) functionality for the 5ESS switch. For CDMA, PSU2 processes both voice and call control information required to support calls made by and to CDMA telephone users. In the ISDN application, PSU2 provides a platform for implementing ISDN features by terminating signaling messages and serving as a packet switch for user data.

1.2 GENERAL DESCRIPTION OF OPERATION

1.2.1 CDMA APPLICATION

The following discussion presents a high level application level view of the major functions provided by PSU2 for the CDMA system.

Figure 1 is a high level view of the 5ESS/CDMA system architecture. One or more 5ESS SMs in a Mobile Switch Center (MSC) may be connected to several CDMA cell sites via trunks. The CDMA cell sites contain equipment to implement the "air" interface link between the mobile users and the wired, land based portions of the CDMA system.

Communication channels are established from each cell site via trunks through the SM's Time Slot Interchange (TSI), and the Data Fanout Multiple PIDB (DFMP) circuit to a Protocol Handler General model 4 (PH4/PHG4) in PSU2. The information exchanged between the PH4 and the cell site consist of packetized voice and call control messages. PH4 performs a frame relay function by forwarding packets originating at cell sites to one or more Protocol Handler Voice (PHV) circuits. Likewise, PH4 collects information packets being transmitted by one or more PHV circuits and forwards them to the appropriate cell site. Information transfer between various PHs occurs over a 100 Mbps packet bus within PSU2.

PHV circuits decode QCELP encoded voice packets received from a PH4 and generate a Pulse Code Modulated (PCM) voice representation. The PCM voice format may then be sent on to the Public Switched Telephone Network (PSTN) via the DFMP, TSI, and DLTU. For voice information flowing from the PSTN to the cell site, PHV performs the reciprocal function of encoding PCM samples into QCELP encoded voice packets, which are then forwarded by PH4 circuits to cell sites.

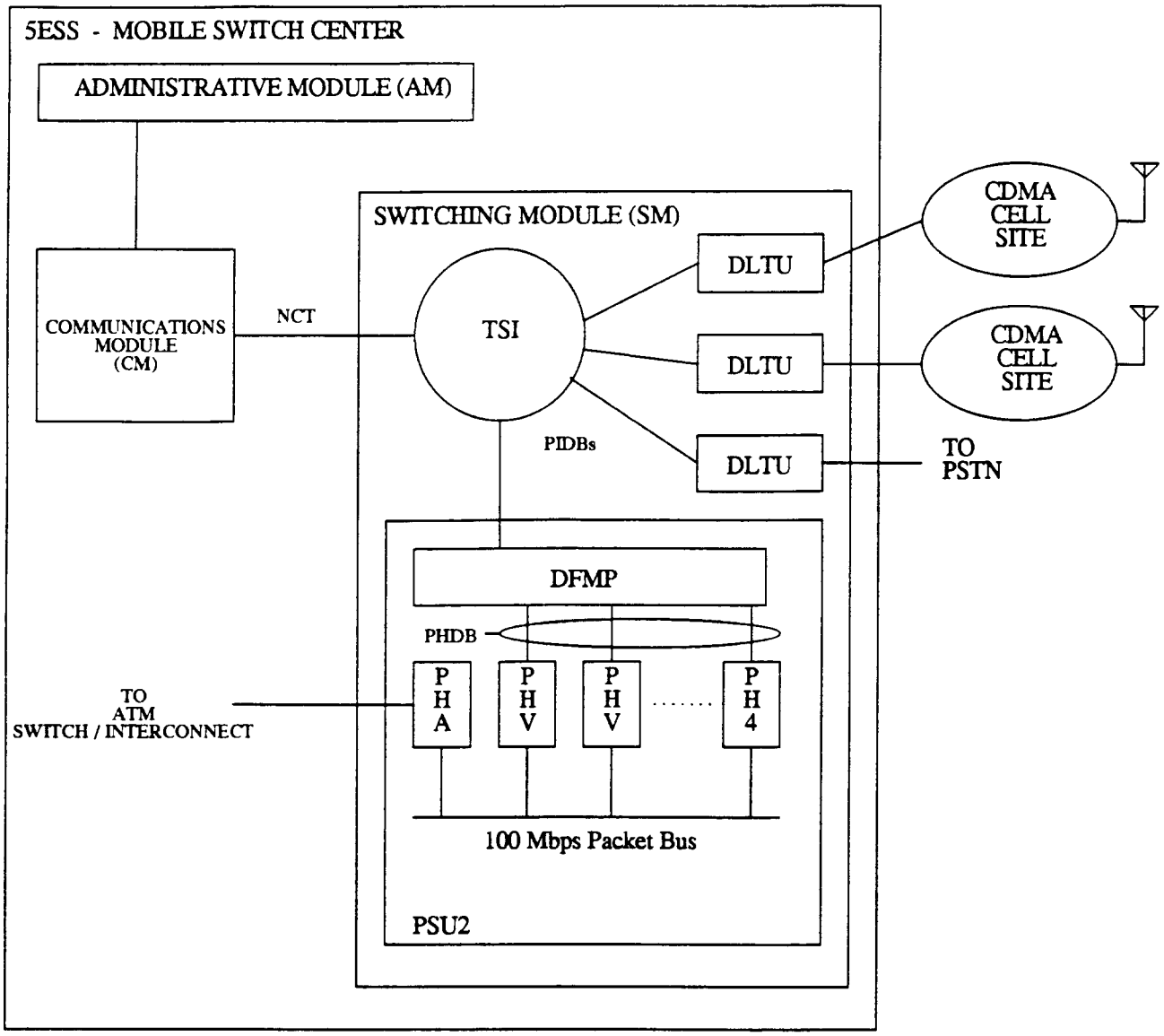


Figure 1. High Level 5ESS/CDMA System Architecture

As mobile units move from one cell site to the next, the PHV, performing the encoding and decoding functions, may not physically reside in the same PSU2 as the PH4 communicating with the cell site. Thus, to meet the end-to-end delay objectives of the system, another protocol handler type is used to efficiently transfer packet information between PSU2 units in different SMs. Protocol Handler ATM (PHA) implements this inter SM transfer capability. The inter SM interface adheres to SONET/SDH and ATM standards. This capability allows either direct connection between PHA circuits in the case where minimal inter SM connectivity is required, or to an ATM switch in the case where connectivity between many SMs is required.

1.2.2 ISDN APPLICATION

Figure 2 is a high level view of a 5ESS central office switch showing one SM equipped with a PSU2 and Integrated Services Line Unit (ISLU) for ISDN service. Additional SMs with similar equippage may also be supported on the switch depending on the total number of Digital Subcriber Line (DSL) terminations

required. The ISLU provides the functionality required to physically and functionally interface to a DSL. Each DSL supports a single 16 Kbps D channel and two 64 Kbps B channels. D channels are used primarily to transmit signaling messages between the subscriber and the switch. Additionally, users may elect to also use the D channel for packet switched data calls. The B channels may be used for transmitting digitized voice or for packet switched data calls.

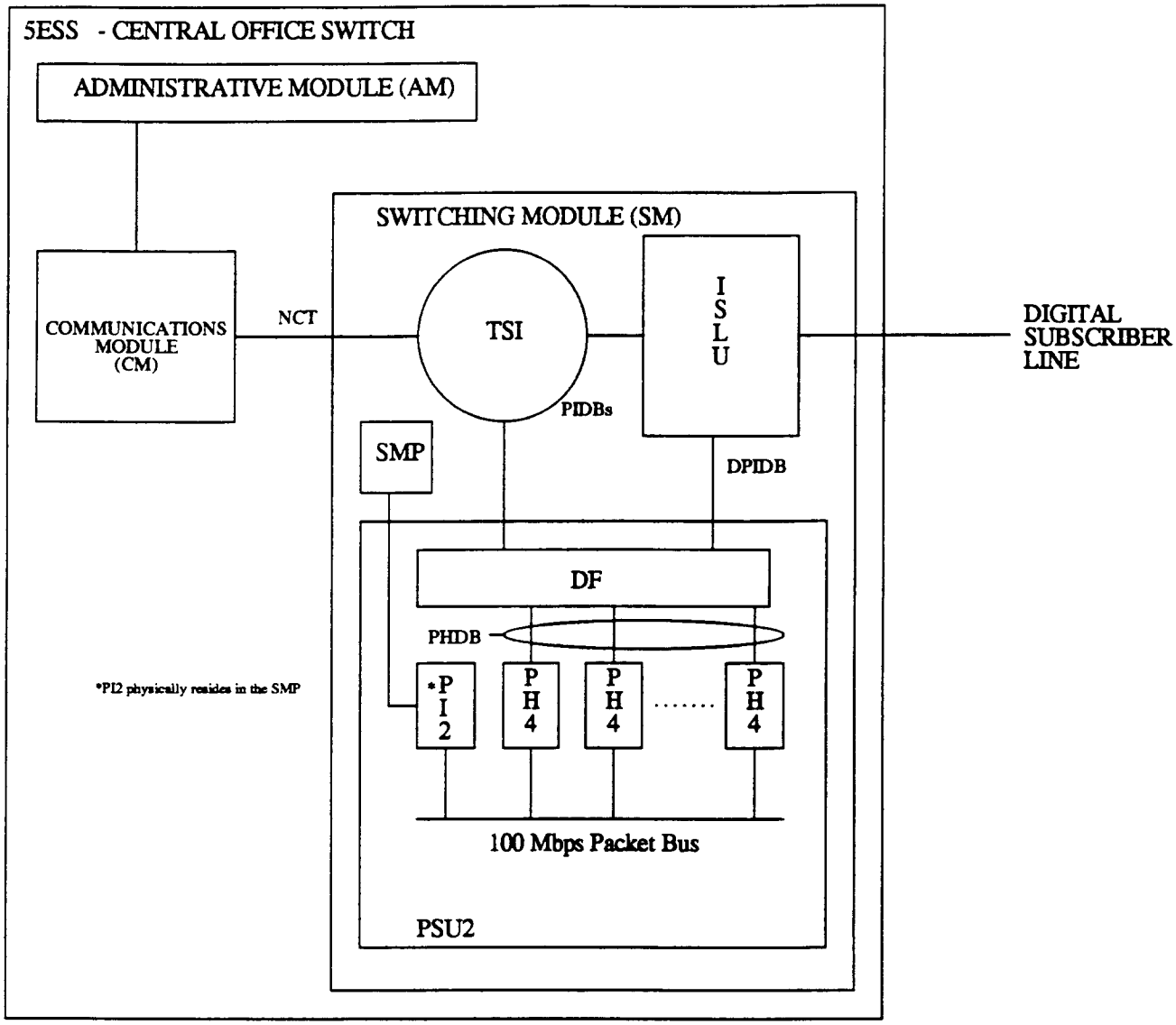


Figure 2. PSU2 ISDN APPLICATION

Circuit switched communication channels are established from the ISLU to Protocol Handler model 4 (PH4) circuits for D channels. The path for this channel is through the Directly connected Peripheral Interface Data Bus (DPIDB), DF circuit, and the Protocol Handler Data Bus (PHDB). As noted above, information transfered over a D channel may be either a call control or signaling message or a user data packet. Signalling messages are routed by PH4 to the SMP for processing, via the 100 Mbps packet bus and the Packet Interface model 2 circuit. The SMP through the same path, in reverse order, has the capability to forward call control messages to the user as well.

When the D channel is also being used for a packet switched data call, packets received by PH4 on the D channel are routed, using the packet bus, to another PH4 having connectivity to the other DSL. Routing information is established for each packet data call during the call setup phase by the SMP. The SMP, via PI2 and the packet bus, communicates that information to the PH4 circuits.

B channels used for circuit switched voice calls are routed directly from the ISLU to the TSI, where connectivity to the PSTN may be established. When a subscriber wants to use a B channel for a packet switched data call, the B channel is connected to a PH4 (usually a different one than the one terminating the D channel for that same DSL) via the DPIDB, DF, and PHDB. From a PSU2 perspective, packet switched calls on the B channel are essentially the same as those on the D channel except for the higher bandwidth (64 vs 16 Kbps) and the need to connect the B channel on a call by call basis to a PH4 providing that service.

2. DETAILED DESCRIPTION

The general description above highlighted the data processing functionality of PSU2. In addition to those functions, PSU2 also incorporates a variety of control functions to support hardware initialization, error reporting, diagnostics, and fault recovery.

The following sections present a more detailed view of both the PSU2 control and data functions in an application independent manner where appropiate. The material is organized around functional boundaries for clarity.

2.1 FUNCTIONAL DESCRIPTION

2.1.1 PSU2 CONTROL CIRCUITS AND INTERFACES

Figure 3 depicts the PSU2 control structure and its relationship to a SM. The PSU2 hardware level control interface is provided by duplexed 5ESS Peripheral Interface Control Busses (PICB) which terminate on Control Fanout model 2 (CF2) circuits on the base shelf. CF2 circuits are equipped in duplexed pairs on the base shelf only, and as its name implies, a major CF2 function is to fan control information out to other circuits in the unit. These circuits include the Packet Fanout model 2 (PF2) and the Data Fanout (DF) circuits. PF2 and DF are equipped in pairs on each PSU2 shelf, including the base and any growth shelves. The collection of CF2, PF2, and DF circuits is generally referred to as PSU Common (PSUCOM) hardware, which is divided into sides 0 and 1. Generally, PSUCOM sides operate electrically and functionally independent of one another. At any given time, only one PSUCOM side is considered active, and the other side is in a standby or out-of-service state. The state (i.e. active, standby, out-of-service) of a PSUCOM side is controlled by the SM. While the SM uses both the active and standby PSUCOM sides to configure and initialize a PSU2 for service, most of the communication occurs between the SM and the active PSUCOM.

Communication between the SM and PSU2 is message based over a PICB. Each PICB contains serial clock, data out, data in, side select, and interrupt signals. Electrically, the clock and data signals employ differential drive techniques over twisted pairs, and the side select and interrupt signals are driven single ended using optical isolators. Of the two PICBs terminating on a CF2, only one is selected for use by the SM. The selection is made by the SM configuring the states of the side select signals in each PICB. For example, if the side select signals are in the same state (i.e. either both high or both low) the CF2 regards the PICB from SM side 0 as active. Likewise, if the side select signals are in different states, CF2 uses the PICB from SM side 1. With the exception of the interrupt signal, communication over the PICB only occurs when the SM wants to either send or retrieve information to/from CF2. The interrupt signal is a

means for CF2 to asynchronously alert the SM to some condition (e.g. error condition) requiring its attention.

Messages transmitted by the SM may be addressed to the CF2 or to any other PF2/DF circuit within the same PSUCOM side. CF2 messages are processed internally to that circuit, while messages destined to a PF2/DF must be forwarded by the CF2. The interface which allows CF2 to PF2/DF communication is the Control Interface Bus (CIB). Each PF2 and DF in a PSUCOM side has an independent CIB link to its CF2 circuit. Every CIB link contains serial clock, data out, and data in signals, supporting a two way, message based communication mechanism. Generally, communication between a CF2 and PF2/DF circuit follows a command/response format. For example, the CF2 will send a command to write or read some register or memory, and the peripheral (i.e. PF2 or DF) will respond back with command status and data if appropriate. The CIB does however support asynchronous message transfer from a PF2/DF to CF2 for reporting events such as error conditions. Via the PICB and CIB communication paths, the SM has access to various registers and memory on CF2, PF2, and DF circuits needed for initialization, configuration, testing, and error recovery.

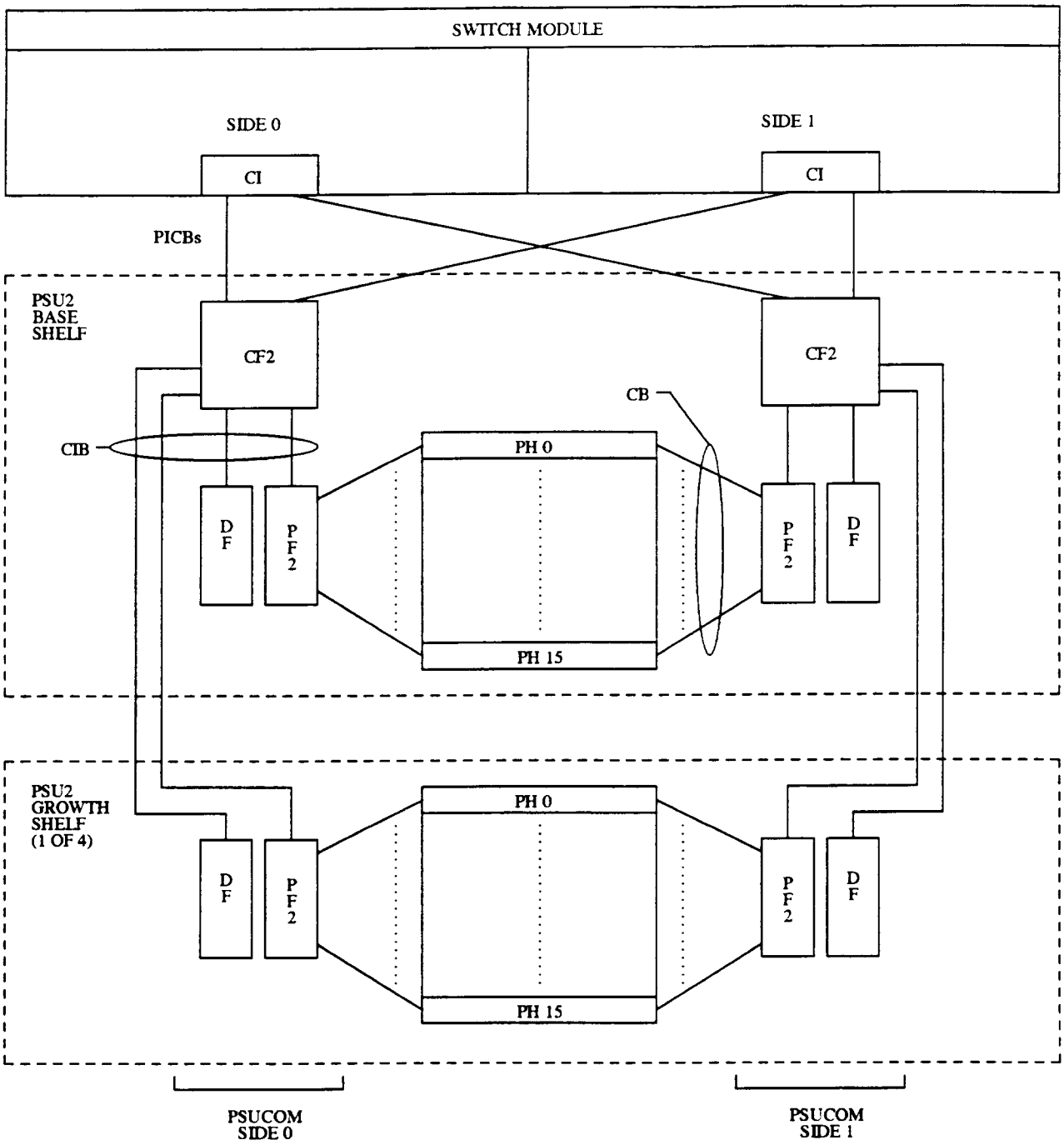


Figure 3. PSU2 Control Architecture

At the lowest level in the control structure, each protocol handler circuit on a shelf has two Control Bus (CB) links, one to each PF2 on the same shelf. The CB links for a PH are electrically independent to all other PHs, with each containing a PH reset, side select, and error signals. The reset and side select signals are sourced by the PF2, while the error signal is driven by the PH. For any PH, the reset and side select signals from PF2 circuits are electrically isolated, but the PH has only one error signal output which is routed to both PF2 circuits.

Similar to the PICB side select functionality, the CB side select signals are used to configure the active PSUCOM for a PH. With the CB side select select signals in the same state, the PH will only allow the reset signal from PSUCOM side 0 to affect the PH. Likewise, when the side select signals are in different states, the PH will only respond to the reset signal from PSUCOM side 1. In addition to this use, the PH uses the side select information to determine the active data bus (see Packet Bus discussion) to be used during initialization. Both the CB reset and side select signal states are determined by commands sent from the SM to the PF2 via the PICB and CIB paths. The PH error signal is the mechanism allowing a PH to report serious hardware problems to the SM, which may not be possible using higher level communcation mechanisms (see Packet Bus discussion). The error signals terminate at registers within PF2 accessible by the SM.

2.1.2 PSU2 PACKET BUS CIRCUITS AND INTERFACES

The PSU2 data functionality is provided by two independent structures - the 100 Mbps packet and time slot data busses. This section will focus on the packet bus architecture and operation, and the following section will cover the time slot busses.

The physical implementation of the packet bus is optimized for efficient bus utilization and fault isolation. As a result, the functional operation of the bus is not clear when studying it from a physical perspective. The following discussion begins with a functional view followed by a presentation of the physical architecture with its various components.

Figure 4 shows a functional view of the dual 100 Mbps Packet Bus (PB) architecture within PSU2. Each of the 80 possible PH circuits and both Packet Interface model 2 circuits in the SM interface to both PBs. Each PB is functionally and electrically independent from the other, and while they are normally configured in active/standby modes, there is no PSUCOM hardware limitation on using both busses simultaneously.

The PB interface consists of data transfer (solid lines in the figure) and arbitration control (dashed lines) elements. As the figure indicates, both data and control functions of the bus are distributed amongst CF2, PF2, backplane, and cable hardware components. The data portion of each PB contains a two bit wide, bidirectional data bus and a 50 MHz clock (i.e 100 Mbps transfer rate). Information transfers are packetized, with each packet containing an address header (destination and source), information field, and a CRC code for error checking purposes. The address and CRC fields are fixed length while the information portion is variable depending on the application and message type. Each PI2 and PH is assigned a PB address dependent on its physical location (i.e. shelf and slot for PHs & SM side for PI2). With this scheme, a packet being transmitted on the bus arrives at the input of all PH and PI2 circuits. Each PH/PI2 must then examine the incoming destination address in the packet header to determine if the remainder of the packet should be processed (destination address match) or ignored (no destination address match).

In addition to exchanging application level messages, the other major use of the PB is to transfer generic software images to PH circuits during PSU2 initialization. This process is commonly referred to as pumping a PH. The SM is the source of PH software images, and thus, controls the entire pump process. The path for an image from the SM is via the PI2 circuit, which is a peripheral circuit to the Switch Module Processor (SMP).

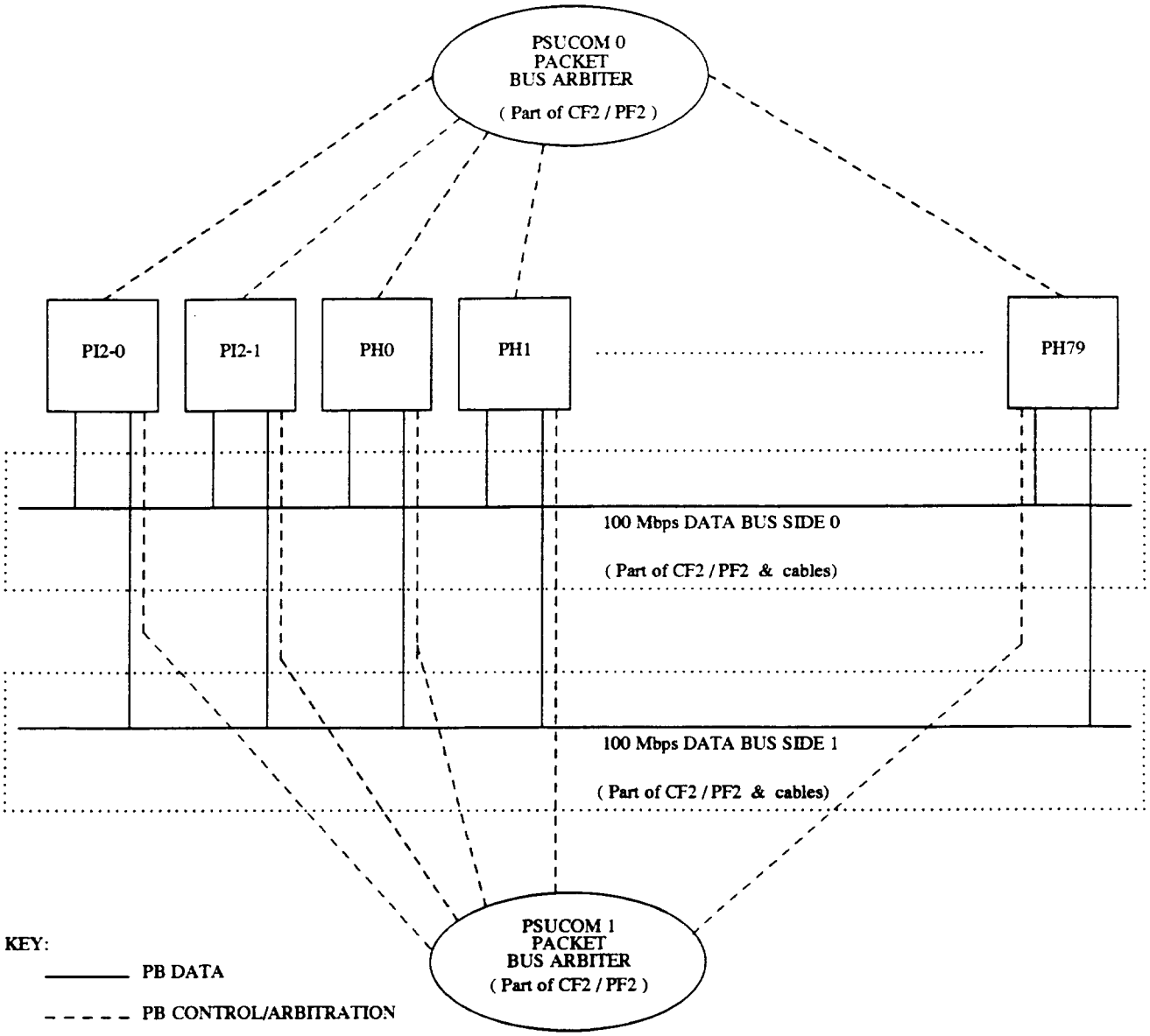


Figure 4. PSU2 - 100 Mbps Packet Bus Functional View

Gaining access to each PB is a function of the control portion of the bus. Only one PH or PI2 may own the bus at any one time for the purpose of transmitting data packets, with PB ownership being controlled by a centralized bus arbiter. For each PB, every PH/PI2 interfaces to two, unique arbitration control signals - request-to-send and clear-to-send. PB ownership is requested when a PH/PI2 asserts its request-to-send signal and is granted when the arbiter asserts the clear-to-send signal to that PH/PI2. The request and clear signals remain asserted for the entire time a PH/PI2 is using the bus. When completed, a PH/PI2 will negate its request followed by the arbiter negating the clear-to-send.

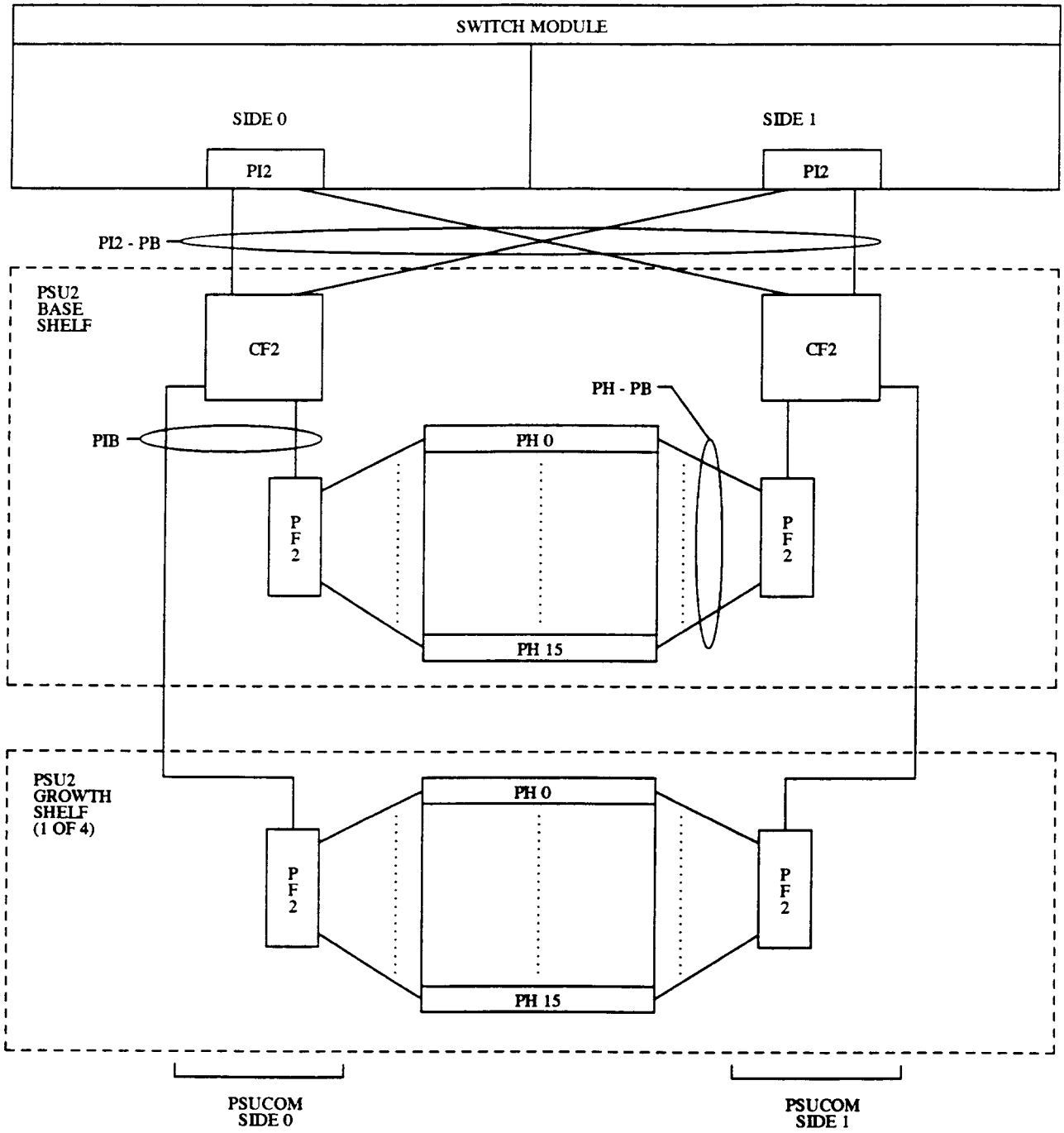


Figure 5. PSU2 100 Mbps Packet Bus Architecture

The physical architecture of the PB is represented in Figure 5 with a base PSU2 shelf and one of four possible growth shelves. Each PH has two Protocol Handler Packet Bus (PH-PB) link interfaces, one to each PF2 circuit on the same shelf. These links are independent from each other and to all other PH-PB links on the shelf. Likewise, each PI2 circuit has two PI2 Packet Bus (PI2-PB) links terminating on a CF2 circuit on each PSUCOM side. Both the PH-PB links and the PI2-PB links are equivalent to the stubs (solid and dashed lines) originating from the PI2 and PH symbols shown on Figure 4. Connectivity

amongst all the PI2-PB and PH-PB links is provided by circuits on CF2, PF2, and the Packet Interconnect Bus (PIB) links between each PF2 and CF2. The CF2 circuit provides up to 5 PIB links (1 base + 4 growth shelves), which are electrically isolated from one another. The isolation of the various packet bus links mentioned above is the primary contributor to providing a structure where a failure on any one link affects only that link (i.e. fault isolation).

Each PH-PB link consists of

- two bidirectional data,
- 50 MHz clock,
- request-to-send, and
- clear-to-send signals.

The data and clock signals employ differential line driver/receiver techniques, while the request-to-send and clear-to-send signals use single ended TTL transmission.

Each PI2-PB link consists of

- two transmit data,
- a 50 MHz transmit clock,
- two receive data,
- a 50 Mhz receive clock,
- request-to-send, and
- clear-to-send signals.

All PI2-PB link signals employ differential transmission techniques. Unlike the PH-PB links, the PI2-PB links employ unidirectional clocks and data. Because the PI2-PB links utilize 20 foot long cables, the transmission delay becomes significant to the point where bidirectional data and a single clock do not provide a reliable transport mechanism.

The PIB links are composed of

- two bidirectional data,
- one 50 Mhz clock,
- four scan address,
- one high summary request,
- one low summary request,
- one scan request-to-send,
- one transmit request-to-send, and
- one clear-to-send signals.

Of these signals, only the data and clock signals employ differential transmission techniques, the remainder are single ended TTL.

2.1.2.1 PF2 Packet Bus Functionality

The PF2 packet bus functionality includes

- Providing data connectivity between the PIB and PH-PB links,
- generating and routing shelf requests to the CF2 circuit, and
- transfering bus ownership to a PH on the shelf.

As noted earlier, all packets being transported on the PB appear at the packet bus interface port of each PH/PI2. This functionality allows any PH/PI2 to communicate with any other PH/PI2. Two scenarios are possible regarding data connectivity within PF2.

1. When the current packet bus owner is not on the same shelf as the PF2, the transmitted packet appears on the PIB (i.e. coming from the CF2) and the PF2 "fans out" or distributes it onto each PH-PB link.
2. If the current packet bus owner is on the same shelf as the PF2, the transmitted packet is being sourced on a PH-PB link on that shelf, and must be distributed by PF2 to the other 15 PH-PB links and the PIB link to the CF2.

PF2 provides information to CF2 to enable it to perform the bus arbitration function. This information includes the high summary request, low summary request, and scan request-to-send signals. The high summary request is asserted whenever any PH in slots 8 - 15 have a request-to-send asserted. Likewise, the same is true for the low summary request except it applies to PHs in slots 0 - 7. The summary requests allow the CF2 based arbiter to save time finding a bus owner. For example, if a summary request is negated, the arbiter will not take the time to scan the individual request-to-send signals for those PHs. In the event a summary request is asserted, the arbiter will then begin to scan or poll the individual request-to-send signals represented by the summary signal. Polling the individual signals involves the scan address and scan request to send signals. The scan address is decoded (4 bits -> one out of 16) and used by PF2 to gate the corresponding PH's request-to-send onto the scan request-to-send signal line to CF2.

The CF2 based arbiter will stop polling when it finds an asserted request-to-send. At that time, the arbiter waits for the current bus owner, if there is one, to complete its transmission and then asserts a clear-to-send on the PIB to the shelf containing the next bus master. The PF2 takes the PIB clear-to-send and generates a clear-to-send to the PH represented by the decoded scan address, and asserts the transmit request-to-send signal to CF2. The transmit request-to-send is used by the arbiter to determine that the bus is being used by the new owner. At the completion of its transmission, the PH will negate its request-to-send, causing the PIB transmit request-to-send to be negated. This action informs the arbiter that the previous bus owner has completed its transmission.

2.1.2.2 CF2 Packet Bus Functionality

The CF2 packet bus functionality includes

- providing data connectivity between the PI2-PB and PIB links, and
- implementing the packet bus arbitration and control mechanism.

The data connectivity functions for CF2 are similar to the ones described for PF2, but at a higher level in the bus structure. From CF2's perspective, packet data may be sourced from any shelf or from either PI2. In the first case where CF2 has granted the bus to a PH, CF2 takes the packet data from the corresponding PIB and "fans out" or distributes it to the remaining PIB and both PI2-PB links. In the second case, one of the PI2 circuits has been granted and is transmitting a packet on the bus. Here, CF2 distributes packet data from the PI2 to all PIB and the other PI2-PB links.

The packet bus arbitration and bus control process has been described in the PF2 disscusion. It is worth noting that the arbitration and control functions are loosely coupled on CF2. For our purposes, arbitration

refers to finding the next bus owner, while control refers to granting ownership and monitoring the current owner's use of the bus. Loose coupling between the arbitration and control processes together with implementing both transmit and scan request-to-send signals allows the arbiter to search out and find the next possible bus owner, while the current owner is transmitting. This capability helps to maximize bus efficiency by eliminating idle bus periods.

A control function, which has not been mentioned to this point, is the bus timeout function. Every time bus ownership is granted (clear-to-send asserted), CF2 starts a timer. If the owner fails to relinquish bus ownership (i.e. negates transmit request-to-send) before the timer expires, the owner is forced from the bus by negating the clear-to-send. The bus timeout condition also results in a CF2 error report to the SM. For PSU2 the bus timeout value established is based on the needs of PHA's packet bus holdoff feature, and is approximately twice the time that would be required for a 4K byte packet to be transmitted.

2.1.3 PSU2 TIME SLOT DATA CIRCUITS AND INTERFACES

The remaining functional area to discuss is the time slot data architecture represented by Figure 6. The figure shows a base and one of four possible growth shelves. Each equipped shelf may be configured with a maximum of two Data Fanout (DF) circuits, one in each PSUCOM service group. Depending on the application there are presently two types of DF circuits used. The ISDN application uses the Data Fanout Flexible Timeslot (DF-FLEX) circuit type, and the CDMA application uses the Data Fanout Multiple PIDB Flexible Timeslot (DFMP-FLEX) circuit type. Both types perform very similar functions, but differ in the number and type of external interfaces supported.

- DF-FLEX provides one duplex Peripheral Interface Data Bus (PIDB) interface to the SM and six (6) Directly connected Peripheral Interface Data Bus (DPIDB) links. The DPIDB links may be terminated on an appropriate peripheral unit such as an ISLU.
- The DFMP-FLEX provides four (4) duplex PIDB interfaces for connection to the SM. No DPIDB interfaces are supported.

The figure shown is generalized to allow a discussion which may be applied to both DF types. Any discussion of DPIDBs does not apply to the DFMP-FLEX case.

The DF shown has two PIDB interface ports to support a duplex, crosscoupled PIDB originating at the Data Interface (DI) circuit function in the SM. Regardless of the equipped DF type, at least one crosscoupled PIDB must always be configured for synchronization purposes. Each PIDB link is electrically independent of any other links and consists of

- data out,
- data in,
- 4 MHz clock, and
- 8 KHz synchronization signals.

All signals employ differential transmission techniques with twisted pair cables. The SM is the PIDB "owner" and thus drives (i.e. DF receives)the data out, clock, and 8 KHz synchronization signals. The DF drives the data in signal back to the SM. Information is formatted on both data signals as a sequence of 32 timeslots. Each timeslot consists of 16 bits with

- 8 bits for user information,
- 7 bits for signaling, and
- parity bit.

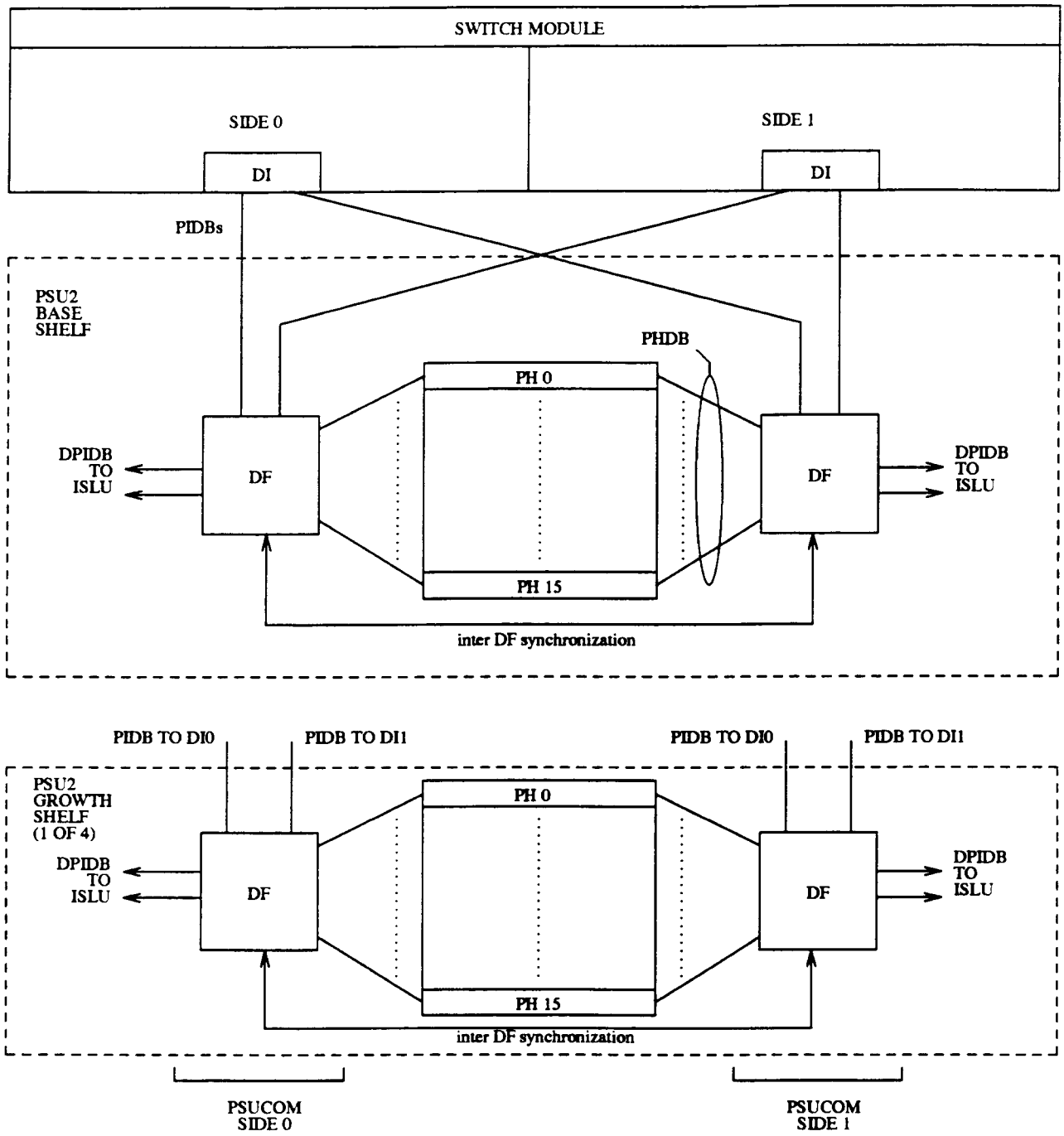


Figure 6. PSU2 TIME SLOT DATA ARCHITECTURE

The data out line is used to transfer information from the DI to the DF, while the data in signal transports timeslot information from the DF to the DI. With a clock frequency of 4.096 MHz, one frame of 32 timeslots occurs every 125 us (i.e. 8 KHz rate). From the PSU2 and DF perspective, only the user information bits are used for data transfer. The signaling bits are useful to the extent required to perform parity related functions only.

DPIDBs, when provided, are sourced by the DF. Each duplexed, cross coupled DPIDB requires two DPIDB ports on each DF as shown in the figure. The signal types, transmission technique, and information format are identical to a PIDB interface. The relationship of the DF circuit to a DPIDB is the same as the DI circuit to a PIDB. Thus, the DF is the DPIDB "owner" and is responsible for driving the data out, clock, and 8 KHz synchronization signals.

Each PH terminates two Protocol Handler Data Bus (PHDB) links, one from each DF circuit on the same shelf. Each link is electrically independent from all others, preventing a fault on any one from affecting any others. PHDBs also provide data out, data in, clock, and 8 KHz synchronization signals with the DF being the "owner". Unlike both PIDB and DPIDB interfaces, the transmission technique used for a PHDB is single ended TTL since the transmission path is relatively short (i.e. within one unit backplane). From a PH perspective, its two PHDBs are normally configured in an active/standby basis. A PH receives information from the active PHDB and outputs identical timeslot data on both PHDBs. The synchronization of signals between two PHDB links at a single PH allows the active/standby state of the PHDBs to be switched without incurring any loss of data.

To support a no error or glitchless PHDB switch at a PH, requires that there be a minimal time skew between the same signals (i.e. clock, sync, data out) on both PHDB links terminating at a PH. The DF circuit can synchronize itself to two sources controlled by the SM and communicated to the DF via the CIB. Normally, the DF in the active PSUCOM side derives synchronization from a PIDB. If the DF on the standby side were to also synchronize to a PIDB, the time skews between the two PHDB inputs at a PH, would not allow a glitchless switch. So to minimize PHDB signal skew, the DF circuit in the standby PSUCOM synchronizes to a mate synchronization signal output by the active DF circuit. Because either DF is required at various times to be active, there are two mate synchronization signals. One is output by the DF on side 0 and and input to the DF on side 1, and vice versa.

The DF provides the functions of a Time Slot Interchange (TSI) amongst the various time slot data links which interface to it. The TSI is a single buffer design, and supports a total of 512 timeslots in two groups of 256 timeslots each. One group of 256 timeslots is permanently associated with PIDB/DPIDB links, and the other group of 256 timeslots is associated with the collection of 16 PHDB links. While the DF physically allows a timeslot to be routed between any two links, normally, timeslots are interchanged between PIDB/DPIDB links and PHDB links. Information which determines how timeslots are exchanged is communicated to the DF by the SM via the CIB. While there is a great deal of flexibility in using and assigning time slots there are a few restrictions listed below.

1. The total number of PIDB/DPIDB timeslots assigned may not exceed 256.
2. The total number of PHDB timeslots assigned may not exceed 256.
3. Across all PHDB links, no more than 8 identically numbered timeslots may be assigned. For example, one could NOT use all the timeslot number 0 on each of 16 PHDB links.
4. The above restriction on 8 timeslots also applies to PIDB/DPIDB links also. For DF-FLEX and DFMP-FLEX, this is not an issue since neither has 8 PIDB/DPIDB links.

2.2 INTERFACES

2.2.1 EXTERNAL

2.2.1.1 PERIPHERAL INTERFACE CONTROL BUS (PICB)

The PICB is a 5 pair cable assembly with a 2x6 connector on each end.

The PICB signal naming convention is:

(*PSU2 Side* **0:1**) **CI** (*SM Side* **0:1**) (*Signal type* **CK:DI:DO:INT:SEL**) **(N:P)**.

PICB SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1]CI[0:1]CK[P:N]	SM	Differential 2.048 MHz PICB clock pair
[0:1]CI[0:1]DI[P:N]	CF2	Differential PICB Data In pair
[0:1]CI[0:1]DO[P:N]	SM	Differential PICB Data Out pair
[0:1]CI[0:1]INTP	CF2	PICB Interrupt
[0:1]CI[0:1]INTN	SM	PICB Interrupt ground return
[0:1]CI[0:1]SELP	SM	PICB Side Select
[0:1]CI[0:1]SELN	CF2	PICB Side Select ground return

2.2.1.2 PERIPHERAL INTERFACE DATA BUS (PIDB)

The PIDB is a 4 pair cable assembly with a 2x4 connector on each end.

The PIDB signal naming convention is:

(*PSU2 Side* **0:1**) (*SM Side* **0:1**) **T** (*PIDB Instance* **P:B:C:D**) (*Signal type* **4MC:8KS:PBI:PBO**) **(N:P)**

PIDB SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1][0:1]T[P:B:C:D]4MC[P:N]	SM	Differential 4.096 MHz PIDB Clock
[0:1][0:1]T[P:B:C:D]8KS{P:N]	SM	Differential 8 KHz PIDB Sync
[0:1][0:1]T[P:B:C:D]PBI[P:N]	DF	Differential PIDB Data In
[0:1][0:1]T[P:B:C:D]PBO[P:N]	SM	Differential PIDB Data Out

2.2.1.3 DIRECTLY connected PERIPHERAL INTERFACE DATA BUS (DPIDB)

The DPIDB signals will be added when the DF-Flex (MC5D124A1D) circuit pack is introduced into the PSU2.

DPIDB SIGNALS		
SIGNAL	SOURCE	DESCRIPTION

2.2.1.4 PACKET BUS (PB) TO PACKET INTERFACE MODEL 2 (PI2)

The PB to PI2 is an 8 pair cable assembly with a 2x12 connector on each end.

The PI2 Packet Bus signal naming convention is:

(*PSU2 Side* **0:1**) **PI** (*SM Side* **0:1**) (*Signal Type* **CTS:DI0:DI1:DO0:DO1:RCK:RTS:TCK**) **(N:P)**

PI2 PACKET BUS SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1]PI[0:1]CTS[P:N]	CF2	PI2 packet bus, differential Clear To Send
[0:1]PI[0:1]DI0[P:N]	PI2	PI2 packet bus, differential Receive Data bit 0
[0:1]PI[0:1]DI1[P:N]	PI2	PI2 packet bus, differential Receive Data bit 1
[0:1]PI[0:1]DO0[P:N]	CF2	PI2 packet bus, differential Transmit Data bit 0
[0:1]PI[0:1]DO1[P:N]	CF2	PI2 packet bus, differential Transmit Data bit 1
[0:1]PI[0:1]RCK[P:N]	PI2	PI2 packet bus, differential Receive Clock
[0:1]PI[0:1]RTS[P:N]	PI2	PI2 packet bus, differential Request To Send
[0:1]PI[0:1]TCK[P:N]	CF2	PI2 packet bus, differential Transmit Clock

2.2.1.5 SONET OC-3 LINKS

The SONET OC-3 link is a 625u fiber optic cable assembly with SC connectors that connects the ATM optical interface circuit packs together. The fiber optic cables originate/terminate on the BKE1 paddle board. The BKE1 implements the PHA Optical Interface Short Span (POISS) which provides the fiber optic to electrical and electrical to fiber optic interface for a respective PHA. The BKE1 paddle-board connects to the non-component side of the PSU2 backplane corresponding to a respective PHA equipped in the component-side of the PSU2 backplane. The electrical signals are not shown in the PSU2 SD.

2.2.1.6 POWER DISTRIBUTION

Unlike the majority of 5ESS units, PSU2 does not employ bulk power converters. Each PSU2 circuit pack is equipped with a circuit board mounted power module, which has 48 volt office battery as an input and generates voltages necessary for that individual circuit. Thus, 48 volt power is provided at the inputs of each circuit pack position.

48 volt power is routed to each PSU2 backplane from the cabinet fuse filter unit using twelve 16 gauge stranded wire cables terminated with a push-on receptacle at the backplane end. Six of the cables supply -48 volts, the other six provide the -48 volt return.

48 VOLT POWER DISTRIBUTION	
Signal	**Description**
-48A	Provides -48 volts to Protocol Handlers 0 through 3
-48ARTN	Provides -48 volt return path from Protocol Handlers 0 through 3
-48B	Provides -48 volts to Protocol Handlers 4 through 7
-48BRTN	Provides -48 volt return path from Protocol Handlers 4 through 7
-48C	Provides -48 volts to PSUCOM side 0 circuit packs
-48CRTN	Provides -48 volt return path from PSUCOM side 0 circuit packs
-48D	Provides -48 volts to PSUCOM side 1 circuit packs
-48DRTN	Provides -48 volt return path from PSUCOM side 1 circuit packs
-48E	Provides -48 volts to Protocol Handlers 8 through 11
-48ERTN	Provides -48 volt return path from Protocol Handlers 8 through 11
-48F	Provides -48 volts to Protocol Handlers 12 through 15
-48FRTN	Provides -48 volt return path from Protocol Handlers 12 through 15
GRD	Central Office Ground

2.2.2 INTERNAL

2.2.2.1 CONTROL INTERCONNECT BUS (CIB)

The CIB and PIB (see next section) physically share a cable asssembly consisting of two, 24 conductor flat flexible cables terminated by a single 2x8 connector on each end.

The CIB signal naming convention is:

(*PSU2 Side* **0:1**) **CIB** (*Destination Board type* **D:P**) (*Shelf #* **0:4**) (*Signal type* **CK:DI:DO**)

CIB SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1]CIBD[0:4]CK	CF2	Data Fanout CIB clock
[0:1]CIBD[0:4]DI	DF	Data Fanout CIB data in
[0:1]CIBD[0:4]DO	CF2	Data Fanout CIB data out
[0:1]CIBP[0:4]CK	CF2	Packet Fanout CIB clock
[0:1]CIBP[0:4]DI	PF2	Packet Fanout CIB data in
[0:1]CIBP[0:4]DO	CF2	Packet Fanout CIB data out

2.2.2.2 PACKET INTERCONNECT BUS (PIB)

The PIB consists of control and data signal elements. The control signals physically share a cable assembly with the CIB (see previous section).

The data signal portion of the PIB is contained in a cable assembly consisting of 4 twisted pairs terminated on each end by a 2x4 connector.

2.2.2.2.1 PIB Control Signals

The PIB Control signal naming convention is:

(*PSU2 Side* **0:1**) **S** (*Shelf #* **0:4**) (*Signal type* **ADD[A:D]:CTS:SRTS:XRTS:SUMH:SUML**)

PIB CONTROL SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1]S[4:0]ADD[D:A]	CF2	4 bit, packet bus arbiter scan address. A is the LSB and D is the MSB.
[0:1]S[4:0]CTS0	CF2	Clear To Send
[0:1]S[4:0]SRTS0	PF2	Scan Request To Send
[0:1]S[4:0]XRTS0	PF2	Transmit Request To Send
[0:1]S[4:0]SUMH0	PF2	High summary request for PHs in slots 8
[0:1]S[4:0]SUML0	PF2	Low summary request for PHs in slots 0

2.2.2.2.2 PIB Data Signals

The PIB data signal naming convention is:
(*PSU2 Side* **0:1**) (*Shelf #* **4:0**) **PB** (*Signal type* **CK:D0:D1**) **(N:P)**

PIB DATA SIGNALS		
SIGNAL	**SOURCE**	**DESCRIPTION**
[0:1]S[4:0]PBCK[P:N]	CF2	Differential 50 MHz packet bus clock pair
[0:1]S[4:0]PBD0[P:N]	PF2/CF2	Differential packet bus data bit 0. PIB data bits are bidirectional
[0:1]S[4:0]PBD1[P:N]	PF2/CF2	Differential packet bus data bit 1. PIB data bits are bidirectional.

2.2.2.3 OUT OF SERVICE (OOS) DISPLAY SIGNALS

The OOS display signals are responsible for controlling the OOS indicator LEDs, found on the faceplate of each PF2 and DF circuit pack. These signals are sourced by CF2 and are controlled by the SM via messages communicated over the PICB. The CF2 in a specific PSUCOM side only controls the signals for that specific side. The OOS LEDs for each shelf are independent of one another, allowing circuits to be OOS on one shelf and in service on other shelves (e.g. during growth procedures).

On a PSUCOM basis, there are two signals for each shelf. One supplies power (+5 volts) and the other is an LED activation signal. When the latter is returned to ground potential on CF2, the OOS LEDs for the PF2/DF on the corresponding shelf and side illuminate. This scheme allows the LEDs to be illuminated even if the PF2/DF circuit is not powered.

The OOS signals are divided into two groups. The first applies to PF2/DF OOS displays on the base shelf, and the second applies to those displays on each of four growth shelves.

2.2.2.3.1 BASE SHELF OOS SIGNALS

The base shelf OOS display signal format is:

(*PSU2 Side* **0:1**) (*Signal type* **OOS:P5OOS**)

BASE SHELF OOS DISPLAY SIGNALS		
SIGNAL	**SOURCE**	**DESCRIPTION**
[0:1]OOS	CF2	Base shelf OOS display activation signal
[0:1]P5OOS	CF2	Base shelf OOS +5 volt power

2.2.2.3.2 GROWTH SHELF OOS SIGNALS

For growth shelves, OOS signals are routed from the base shelf to each growth shelf using a twisted pair cable assembly terminated with a 2x4 connector at each end.

The growth shelf OOS display signal format is:

(*PSU2 Side* **0:1**) **S** (*Shelf #***4:1**) **OOS (N:P5)**

GROWTH SHELF OOS DISPLAY SIGNALS		
SIGNAL	**SOURCE**	**DESCRIPTION**
[0:1]S[4:1]OOSN	CF2	Growth shelf OOS display activation signal
[0:1]S[4:1]OOSP5	CF2	Growth shelf OOS +5 volt power

2.2.2.4 PROTOCOL HANDLER PACKET BUS (PH-PB)

The Protocol Handler Packet Bus consists of control and data signal elements, both of which are contained entirely within the MLB backplane.

2.2.2.4.1 PROTOCOL HANDLER PACKET BUS CONTROL SIGNALS

The signal naming convention for PH-PB Control signals is:

(*PSU2 Side* **0:1**) (*PH slot #* **15:00**) (*Signal type* **PBCS0:PBRS0:PRSH0**)

PROTOCOL HANDLER PACKET BUS CONTROL SIGNALS		
SIGNAL	**SOURCE**	**DESCRIPTION**
[0:1][15:00]PBCS0	PF2	PH Clear To Send
[0:1][15:00]PBRS0	PH	PH Request To Send
[0:1][15:00]PRSH0	X	PH high priority Request To Send. These signals exist within the backplane between PH and PF2 slots, but have no functionality at this time.

2.2.2.4.2 PROTOCOL HANDLER PACKET BUS DATA SIGNALS

The signal naming convention for PH-PB Data signals is:

(*PSU2 Side* **0:1**) (*PH slot #* **15:00**) (*Signal type* **HSC:HSD0:HSD1**) **(P:N)**

PROTOCOL HANDLER PACKET BUS DATA SIGNALS		
SIGNAL	**SOURCE**	**DESCRIPTION**
[0:1][15:00]HSC[P:N]	PF2	Differential 50 MHz packet bus clock
[0:1][15:00]HSD0[P:N]	PF2/PH	Differential, bidirectional packet bus data bit 0
[0:1][15:00]HSD1[P:N]	PF2/PH	Differential, bidirectional packet bus data bit 1

2.2.2.5 CONTROL BUS (CB)

Connectivity for the PH Control Bus (CB) is contained entirely within the MLB backplane.

The CB signal naming convention is:

(*PSU2 Side* **0:1**) (*PH slot #* **15:00**) (*Signal type* **CBRS0:CBAS1**), OR

(*PH slot #* **15:00**) **CBERR0**

CONTROL BUS SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1][15:00]CBRS0	PF2	PH reset
[0:1][15:00]CBAS1	PF2	PH side select
[15:00]CBERR0	PH	PH error

2.2.2.6 PROTOCOL HANDLER DATA BUS (PHDB)

Connectivity for the Protocol Handler Data Bus (PHDB) is contained entirely within the MLB backplane.

The PHDB signal naming convention is:

(*PSU2 Side* **0:1**) (*PH slot #* **15:00**) (*Signal type* **DBCK1:DBSY1:DBDO1:DBDI1**)

PROTOCOL HANDLER DATA BUS SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
[0:1][15:00]DBCK1	DF	PHDB 4.096 MHz clock
[0:1][15:00]DBSY1	DF	PHDB 8 KHz sync
[0:1][15:00]DBDO1	DF	PHDB serial timeslot data out
[0:1][15:00]DBDI1	PH	PHDB serial timeslot data in

2.2.2.7 PHA OPTICAL INTERFACE

PHA OPTICAL INTERFACE SIGNALS		
SIGNAL	SOURCE	DESCRIPTION
ATMRC[00:15][N:P]	BKE1	155.52 Mb/s data in
ATMXM[00:15][N:P]	PHA	155.52 Mb/s data out
ID[0:7][00:15]	BKE1	Paddle board data bit
PBADD[0:2][00:15]	PHA	Paddle board address bit
PBRLS[00:15][N:P]	BKE1	Receiver loss of signal
PBASN[00:15]	PHA	Address strobe
PBXME0[00:15]	PHA	Transmitter enable
PBIOSL[00:15]	PHA	Paddle board Out Of Service light enable

2.2.2.8 PACKET BUS SLOT and SHELF ADDRESS

Each PH slot has inputs from the backplane which uniquely define both the slot (i.e. 1 of 16 on each shelf) and the shelf (i.e. 1 of 5). These inputs are used by a PH to determine its unique packet bus address.

There are four slot address bits, **ADD[3:0]1**, whose configuration is determined by MLB backplane routing. The following table shows the relationship between PH slot number and slot address.

PH SLOT ADDRESS				
BADD31	**BADD21**	**BADD11**	**BADD01**	**PH SLOT #**
L	L	L	L	00
L	L	L	H	01
L	L	H	L	02
L	L	H	H	03
L	H	L	L	04
L	H	L	H	05
L	H	H	L	06
L	H	H	H	07
H	L	L	L	08
H	L	L	H	09
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

In the previous table, H and L correspond to low (i.e. ground) and high (i.e. +5 volts) voltage levels respectively.

The shelf address is determined by three signals, **BADD[6:4]1**, whose assignments are made by a 982AC paddle board with a 2x6 connector. Unlike the slot address signals, the shelf address signals are common to all PH slots on a single shelf. The following table shows the relationship between shelf address configuration and physical shelf.

PH SHELF ADDRESS			
BADD61	**BADD51**	**BADD41**	**PH SHELF**
L	L	L	BASE PSU2 SHELF
L	L	H	1st GROWTH SHELF
L	H	L	2nd GROWTH SHELF
L	H	H	3rd GROWTH SHELF
H	L	L	4th GROWTH SHELF

In the previous table, H and L correspond to low (i.e. ground) and high (i.e. +5 volts) voltage levels respectively.

2.3 PHYSICAL DESCRIPTION

2.3.1 CABINET LEVEL

The PSU2 is growable from a minumum of one shelf to a maximum of five shelves. In most applications the PSU2 resides in the LTP cabinet. Cooling is provided by a mid fan unit assembley (J5D003FH-2, or equivalent). If four shelves are used, a plenum is required in the two bottom postions, EQLs 19 and 11. If five shelves are used, a plenum is required in the bottom position, EQL 11. The PSU2 requires 6 power feeders and returns per shelf, 3 from the A Bus and 3 from the B Bus. The mid fan unit requires one feeder per fan. Power is supplied via the Modular Fuse Filter Unit (MFFU).

The feeders connecting to the cabinet from the power distribution frame are are protected by 20 amp fuses. The feeders connecting to the shelves from the MFFU are protected by 10 amp fuses, and the feeders conecting to the fans are protected by 3 amp fuses. When two or more PSU2 shelves are equipped in a cabinet, ground straps are used to connect the shelves to maintain a common ground. Figure 7 illustrates how a PSU2 grows in a LTP cabinet. Figure 8 is a power schematic of a five shelf PSU2 in a LTP cabinet.

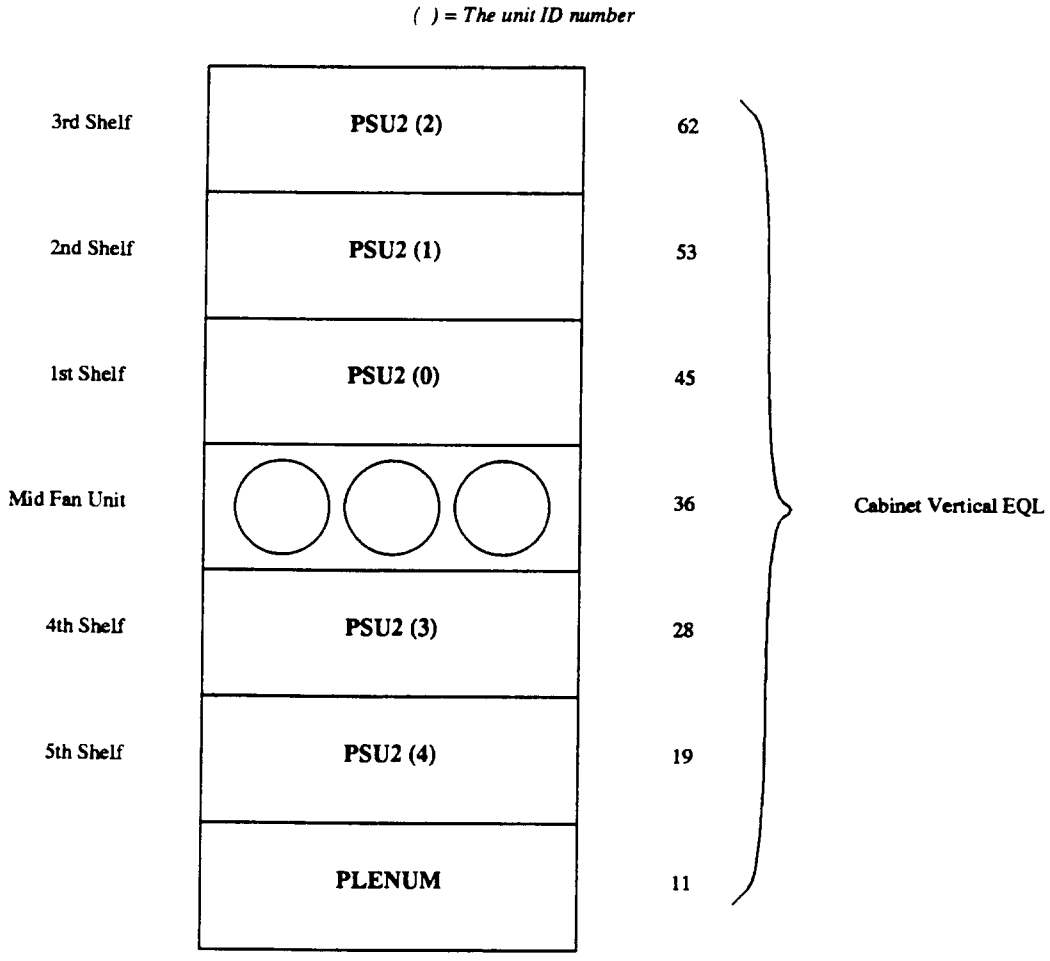


Figure 7. PSU2 EQUIPPED IN A LTP CABINET

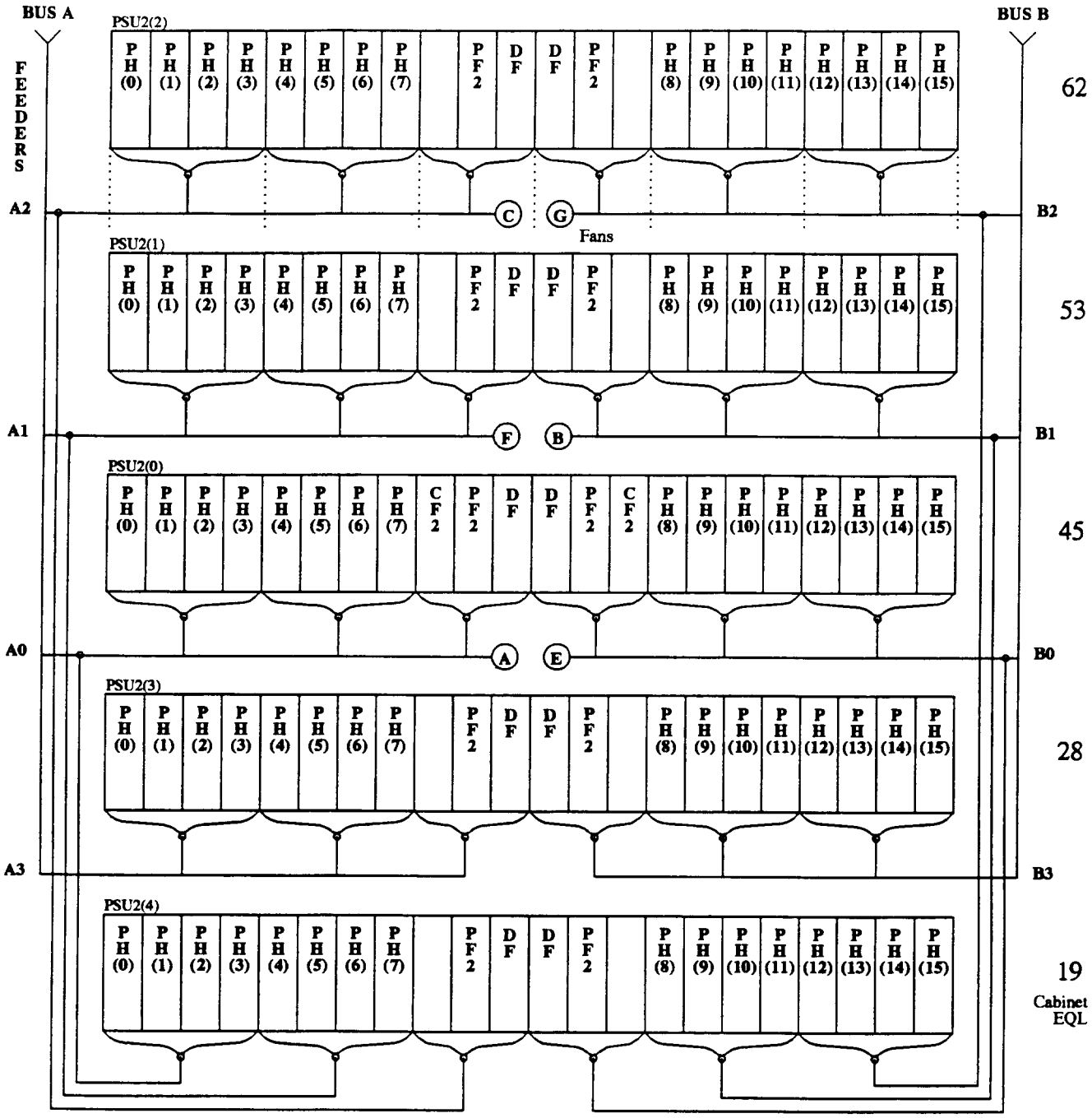


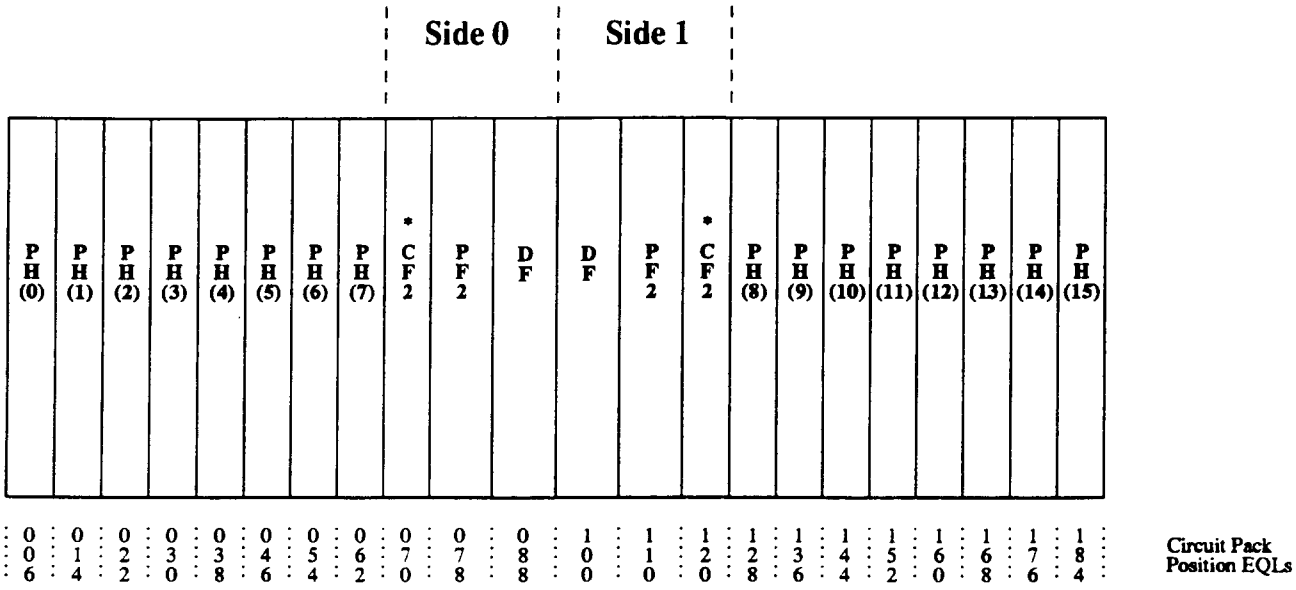
Figure 8. POWER SCHEMATIC OF PSU2 EQUIPPED IN A LTP CABINET

2.3.2 UNIT LEVEL

The PSU2 consists of a 24 1/2 inch wide backplane mounted onto a 500BE shelf. Each shelf supports from 1 to 16 Protocol Handler (PH) circuit packs, and 6 control packs. The PH packs, except for the PHA, are typically equipped from left to right with one PH acting as a spare for others of the same type. If different types of PHs are populated on a shelf, one spare is needed for each type. The control packs, Control Fanout

model 2 (CF2), Packet Fanout model 2 (PF2), and Data Fanout (DF), are duplexed and are used in a active/standby configuration. The PHA is also duplexed. The CF2 is only equipped in the 1st shelf.

Because the control packs are duplexed, the PSU2 shelf is divided into side 0 and side 1. Side 0 packs are at EQLs 70, 78, 88. Side 1 packs are at EQLs 100, 110, 120. Figure 9 shows the PSU2 shelf, along with the listing of each pack and its associated position EQL.



** The CF2 circuit pack is only equipped in the basic shelf (shelf 1).*

Figure 9. PSU2 SHELF

All circuit packs in the PSU2 use board mounted power modules. Therefore, bulk power converters or control and display packs are not used. If non Auto Power Recovery (APR) circuit packs are used in the PSU2, power-up is controlled by sequence pins mounted in the backplane. Out Of Service (OOS) LEDs are provided on each control circuit pack.

2.3.3 BACKPLANE

The PSU2 backplane is an 18-layer, controlled impedance printed wiring board which supports an aggregate base bandwidth of 100Mb/s. Layer 1 starts at the wiring side of the backplane, ending with layer 18 at the component side of the backplane. The backplane has 2 power layers, 10 signal layers, and 6 ground layers.

Power layers: Each power plane is divided into 6 segments, with each segment supplying power to 4 circuit packs.

Signal layers: Of the ten signal layers, six have controlled impedance requirements. Each of the six controlled impedance layers are separated by a ground layer.

- Layers 2, 3, 5, and 6 have a differential impedance requirement of 112 ohms (+/- 10%)[1] to support the

High Speed Data nets, e.g., 000HSD0N.

- Layers 8 and 9 have a a differential impedance requirement of 89 ohms (+/- 10%)[2] to support the High Speed Clock nets, e.g., 000HSCN.

Ground layers: Each ground layer is a full ground plane and is connected to frame gound though the backplane mounting screws.

The backplane utlizes squencing pins to support non APR circuit packs. All pins used are gold (50 micro inches thick) over nickel which conform to 5ESS Switch requirements for the world market. The same backplane is used in each shelf position.

2.3.4 SUPPORTED CIRCUIT PACK TYPES

The PSU2 supports various applications depending on its configuration. The following sections lists these applications and defines which circuit packs are needed to support the application.

2.3.4.1 BOARDS COMMON TO ALL APPLICATIONS

Code	Abbreviation	Pack Name
TN1843	CF2	Control Fanout model 2
UN396	PF2	Packet Fanout model 2

2.3.4.2 BOARDS SPECIFIC TO CDMA WIRELESS PROCESSING

Code	Abbreviation	Pack Name
TN1846	PH4	Protocol Handler model 4 (Frame Relay)
TN1844	PHV	Protocol Handler Voice
UN399	DFMP-FLEX	Data Fanout Multiple PIDBs with Flexible time slot assignment (4 PIDBs).

2.3.4.3 BOARDS SPECIFIC TO ATM CONNECTIVITY

Code	Abbreviation	Pack Name
TN1845	PHA	Protocol Handler ATM
BKE1	BKE1	PHA Optical Interface, Short Span

3. REFERENCE DATA

3.1 WORKING LIMITS

3.1.1 POWER

The maximum power consumption per shelf is 14 amps of office battery. The individual circuit pack current drains and maximum cabinet feeder current drains are listed in the next two tables.

---

1. The optimal differential impedance is 150 ohms, see IMR 510630.
2. The optimal differential impedance is 100 ohms, see IMR 510630.

3.1.1.1 CIRCUIT PACK CURRENT DRAINS

Function	Code	Amps	Watts
CF2	TN1843	0.625	30.0
PF2	UN396	0.55	26.4
DFMP-FLEX	UN399	0.80	38.4
PH4	TN1846	0.63	30.3
PHV	TN1844	0.54	27.6
PHA	TN1845	1.05 (Est)	50.3
BKE1	BKE1	0.36	1.8
FAN	KS23912L2	0.63	NA

3.1.1.2 MAXIMUM CABINET FEEDER CURRENT DRAINS

The maximum cabinet feeder current drains were calculated using a 5 shelf PSU2, equipped with 80 PH4 circuit packs. The maximum current allowed per feeder is 13.5 amps.

Feeder	Qty	Pack	Current	Total	Feeder	Qty	Pack	Current	Total
A0	12	PH4	0.63	7.56	**B0**	8	PH4	0.63	5.04
	1	CF2	0.625	0.625		1	CF2	0.625	0.625
	1	PF2	0.55	0.55		2	PF2	0.55	1.10
	1	DF	0.80	0.80		2	DF	0.80	1.60
	1	FAN	0.63	0.63		1	FAN	0.63	0.63
				10.17					**9.00**
A1	12	PH4	0.63	7.56	**B1**	12	PH	0.63	7.56
	1	PF2	0.55	0.55		1	PF2	0.55	0.55
	1	DF	0.80	0.80		1	DF	0.80	0.80
	1	FAN	0.63	0.63		1	FAN	0.63	0.63
				9.54					**9.54**
A2	8	PH4	0.63	5.04	**B2**	12	PH	0.63	7.56
	2	PF2	0.55	1.10		1	PF2	0.55	0.55
	2	DF	0.80	1.60		1	DF	0.80	0.80
	1	FAN	0.63	0.63		1	FAN	0.63	0.63
				8.37					**9.54**
A3	8	PH4	0.63	5.04	**B3**	8	PH	0.63	5.04
	1	PF2	0.55	0.55		1	PF2	0.55	0.55
	1	DF	0.80	0.80		1	DF	0.80	0.80
				6.39					**6.39**
TOTALS **A0-A3**				**34.47**	TOTALS **B0-B3**				**34.47**

3.2 FUNCTIONAL DESIGNATIONS

3.3 FUNCTIONS

3.4 CONNECTION CIRCUITS

3.5 MANUFACTURING TESTING REQUIREMENTS

3.6 ALARM INFORMATION

3.7 TAKING EQUIPMENT OUT OF SERVICE

If non APR PH packs are equipped in the PSU2, then these packs must be unseated before power is connected or disconnected to the shelf. Failure to unseat non APR PH packs before power is applied may cause the fuse on the PH pack to clear because of surge currents.

4. REASONS FOR REISSUE

5. ACRONYMS, ABBREVIATIONS OR INITIALISMS

APR	Auto Power Recovery
ATM	Asynchronous Transfer Mode
BKE1	paddle board code implementing the PHA Optical Interface, Short Span (POISS)
CB	Control Bus
CDMA	Code Division Multiple Access
CF2	Control Fanout model 2
CIB	Control Interconnect Bus
CRC	Cyclic Redundancy Check
DF	Data Fanout
DF-Flex	Data Fanout with Flexible time slot assignment
DFMP	Data Fanout Multiple PIDB's
DFMP-Flex	Data Fanout Multiple PIDB's with Flexible time slot assignment
DI	Data Interface
DLTU	Digital Line Trunk Unit
DPIDB	Directly Connected PIDB
DSL	Digital Subscriber Line
ISLU	Integrated Services Line Unit
ISDN	Integrated Services Digital Network
LTP	Line Trunk Peripheral
MFFU	Modular Fuse Filter Unit
MSC	Mobile Switch Center
OOS	Out Of Service
PB	Packet Bus
PCM	Pulse Code Modulated
PF2	Packet Fanout model 2
PH	Protocol Handler, generic name for any class of packet bus client physically residing in a PSU2 [ie: PH4, PHA, PHV, etc.]
PH4	Protocol Handler model 4 [aka: Protocol Handler General model 4 (PHG4)]
PHA	Protocol Handler ATM
PHV	Protocol Handler Voice
PI	Packet Interface
PI2	Packet Interface model 2
PIB	Packet Interconnect Bus

PHDB	Protocol Handler Data Bus
PH-PB	Protocol Handler Packet Bus
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
PSU2	Packet Switch Unit model 2
PSUCOM	PSU2 common packs - CF2, PF2, DF
QCELP	Qualcom Codebook Excited Linear Prediction
SM	Switch Module
SMP	Switch Module Processor
TSI	Time Slot Interchange
TTL	Transistor Transistor Logic

AT&T BELL LABORATORIES

DEPT ND9250100 GPO/RMG DWM