5ESS® SWITCHING EQUIPMENT MODULE CONTROLLER AND TIME SLOT INTERCHANGER UNIT MODEL 3 CIRCUIT

CONTENTS

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

This Circuit Description (CD) documents the Module Controller and Time Slot Interchange Unit, Model 3 (MCTU3) cost reduction architecture. The MCTU3 implements the MCTU-Model 2 (MCTU2) functionality and has been developed as a lower cost replacement for the MCTU2.

The MCTU3 is architected to maximize Cost of Goods (COGs) savings while minimizing software impact. The cost reduction is achieved through a combination of unit and pack consolidation on a 500 BI-type unit shelf, together with re-implementation of some of the SMP logic with less expensive technology. The MCTU3 development consists of three fundamentally new pieces:

1. a new backplane which consolidates two separate shelves, side 0 and side 1, into one shelf.
2. a cost reduced Single Board Core (SBCORE) processor board which consolidates the functionality of the MCTU2's Core Support 1 board, Core Support 2 board, Core board, the Applications board, and the six Memory boards, and
3. a combined Single Board Power-Control/ Display (SBPCD) board.

1.2 GENERAL DESCRIPTION OF OPERATION

The 5ESS Switch is a digital time division switch with a time-space-time architecture. The Time Multiplexed Switch (TMS) provides a centralized space division switching function and connects to various Switching Modules (SMs) that perform time division switching and interface to transmission facilities.

The MCTU3's Six-Fan Unit and Fuse/Filter Unit (FFU) are common to all SMs. Various peripheral units such as the Global Digital Service Unit, Metallic Service Unit, Digital Line and Trunk Unit, Line Unit, Trunk Unit, and Packet Switch Unit are equipped in the SM as needed. The MCTU3 resides within a SM and provides the following:

- a Switching Module Processor (SMP) to provide the operating environment for software and interfaces to subunits,
- a fast pump capability used for initialization of SMP memory,
- a time division switch under control of the SMP,
- preprocessing on the signaling and control bits of the time slot data,
- an interface to Network Control and Timing (NCT) links,
- an interface to peripheral units for control information from the SMP,
- an interface to peripheral units for Pulse Code Modulation (PCM) data,
- a Digital Service Unit (DSU) to provide detection/generation of tones used for signaling, and
- an Ethernet interface for the Very Compact Digital Exchange (VCDX).

The MCTU3 is a duplex unit containing two sides (side 0 and 1). The active processor updates the mate (nonactive) processor to provide the ability to switch from side to side. Under no-fault conditions, switching to the mate side is accomplished without introducing errors. Error-checking circuitry and diagnostic aids are used extensively to facilitate maintenance of the MCTU3.

2. DETAILED DESCRIPTION

2.1 FUNCTIONAL DESIGNATIONS

The MCTU3 has nine subfunctions:

1. Single Board CORE (SBCORE)
2. Dual Link Interface (DLI)
3. Time Slot Interchanger (TSI)
4. Signal Processor (SP)
5. Data Interface (DI)
6. Control Interface (CI)
7. Packet Interface (PI)
8. Digital Service Unit (DSU)
9. Single Board Power-Control/Display (SBPCD)

The SBCORE contains the core processing functionality of the MCTU3 SMP. The general architecture of the SBCORE is derived from the SMP20 with the addition of some features found in the SM2000 SMP. The SBCORE utilizes a MC68LC040 microprocessor with a basic clock frequency of 25 MHz. The I/O subsystem of the SBCORE maintain the "classic" SMP address spectrum. A MC68360 (QUICC) device is used to provide communications capabilities for the SBCORE. The SBCORE contains 1MByte of 5-volt only FLASH memory. One devices is utilized to for the generic firmware (512 Kbytes). A second 512Kbyte device contains the Programmable Logic Pump data. The SBCORE makes extensive use of RAM pumped logic devices. After power-up, the Programmable Logic Pump The program data for the pumped logic is stored in a dedicated FLASH EPROM.

The DLI provides the interface to NCT links. It recovers timing information from these links to provide timing for the MCTU3. The DLI contains the transmit and receive circuitry needed to interface to the optical links. It also provides the SMP an interface to the Message Time Slot (MTS) on each NCT link. Because the DLI is in the same failure group as the TMS, cross coupling is necessary for all connections between the DLIs and the duplex MCTU3. The DLI selects one of two NCT links connected to it or the mate DLI as a reference timing source. Under SMP control the TSI selects one of the two DLIs as a clock source and distributes this clock to the rest of the MCTU3.

The TSI is the time division switch, and it contains two 512x512 time slot interchangers, one for data from the TMS to peripheral units and one for data from peripheral units to the TMS. The two 512x512 switches are connected such that time slots may be looped, thereby providing the capability to connect peripheral time slots to other peripheral time slots for intramodule calls. The TSI also provides a data port to the DSU.

The SP performs the hit timing and processing on signaling and control bits (A-G) from peripheral time slots. It provides the SMP access to these bits and provides a First In First Out (FIFO) type queue to report state changes of these bits. It also allows the SMP to source these bits to peripheral units.

The DI provides the data interface to peripheral units. It reformats time slot information and does a 2:1 concentration on peripheral time slots. Two DIs are connected to the TSI, each providing the TSI with 256 time slots per frame. Each DI provides 16 Peripheral Interface Data Buses (PIDBs) for connection to peripheral units.

The CI provides the interface between the SMP and the various peripheral units for control information through Peripheral Interface Control Buses (PICBs). Each CI provides 23 PICB connections. The MCTU3 may be equipped with two CIs (per side) to provide a total of 46 PICBs.

The PI provides the interface to the Packet Switch Unit (PSU). The PI and associated PSU is used in a SM for the Integrated Services Digital Network (ISDN). The PI and PSU provide a centralized high bandwidth interface to support packetized data and signaling messages. By centralizing packet processing in the PSU, efficient signaling, maintenance, and administrative interfaces are maintained and the distributed architecture of the 5ESS Switch is enhanced.

The DSU is responsible for creating and transmitting call-progress tones, multifrequency signals, tone-dialing signals, and common channel interoffice signaling continuity check tones. It also does dial-pulse collection, tone-decoding and detection of multifrequency signals. To provide reliable operation the DSU is composed of two service groups that share the load so that a single fault can at most reduce the DSU capacity by 50 percent. The LDSU uses AT&T-T digital signal processing chips for its required services.

The SBPCD provides the SMP, CIs, PI, TSI-SP, and DIs a common +5 volt power supply in the MCTU3.

The sections that follow deal with the nine previously mentioned MCTU3 subfunctions in more detail.

2.1.1 Single Board CORE (SBCORE) - KBN17

The SBCORE contains the Motorola MC68LC040 microprocessor. The MC68LC040 contains a pipelined execution unit, two 4 Kbyte internal caches (one for instructions and one for data) and a paged Memory Management Unit (MMU). A bus clock of 25 MHz is supplied to the microprocessor. A 50 MHz is also supplied to the microprocessor by the phase-locked loop circuitry of the QUICC device; this clock is used internally by the MC68LC040.

2.1.1.1 QUad Integrated Communications Controller (QUICC)

The QUICC is a versatile one chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. The key features of the QUICC are:

- CPU32+ Processor with external 32 bit data and address bus.
- System Integration Module (SIM60).
- Communications Processor Module (CPM).
- QUICC Memory Spectrum
- QUICC Register Access
- QUICC Interrupt Structure
- QUICC Bootstrapper Function
- BTSR DMA Pump Data Transfer
- BTSR Test Mode
- QUICC SDLC Channels

- QUICC support of Ethernet Paddle Board
- QUICC's general Purpose Timers

2.1.1.2 Parity

Parity is calculated for each byte of the processor address and is sourced by the Flex devices when the MC68LC040 or QUICC devices are in control and is checked by the Flex devices when the Test Utility Bus (TUB) or Update bus is in control.

2.1.1.3 Update Bus Controller (UBC)

The UBC implements a pipelined update bus which is used to keep the mate processor's memory and I/O identical to the active processor's in order to provide a highly reliable duplex processor. In the update mode, all writes which take place in the active side are automatically conducted in the mate processor. The UBC also allows read or write operations to be conducted exclusively to the mate processor (regardless of the state of the update mode) on a forced basis as well as forced operations to both processor sides.

2.1.1.4 The Internal Bus Control (IBC)

The IBC translates the bus protocol of each possible bus owner (e.g. MC68LC040, QUICC, TUB or mate) into the bus protocol of each possible destination protocol (e.g. I/O subsystem, TUB, update bus or QUICC). The state flow is identical for reads and writes; the flow varies in three situations:

1. burst read accesses of the DRC,
2. special function operations, and
3. when the mate is running with access enabled.

2.1.1.5 Burst Writes

Burst writes, while supported by the MC68LC040, are not supported by the SBCORE; all burst writes are converted, via transfer burst inhibit, to long-word writes.

2.1.1.6 Bus Arbiter

The bus arbiter functionality for the SBCORE implements a fixed priority bus arbitration protocol. The following is the priority from highest to lowest: Test Bus DMA, Update bus requests, QUICC DMA and the MC68LC040; by default, the MC68LC040 is in control. If the condition exits where both processor sides are requesting the opposite side at the same time, one side will relinquish the bus and grant it to the other side. A time-out circuit monitors the length of mate requests to make sure a lock condition does not occur if the mate is faulted and unresponsive.

2.1.1.7 Test Utility Bus (TUB)

The interface from the internal address and processor data bus to the multiplexed TUB is used to provide access for various hardware and software debugging tools. Two QLWR gate arrays are utilized to perform the multiplexing of address and data onto the Test Utility Bus. Each QLWR interfaces to half the internal address bus, half the processor data bus, and half of the Test Utility Bus. Address parity is passed from the internal address bus. Data parity is generated on writes to the Test Utility Bus and are used on non-TUB read cycles, as well, to verify the integrity of the internal data bus. Invert parity signals from the Special

Function Maintenance Register can be used to allow diagnostics to force address and data parity errors.

2.1.1.8 Update Bus

Two QLWR gate arrays are utilized to perform the multiplexing of address and data onto the Update Bus. Each QLWR interfaces to half the internal address bus, half the processor data bus and half of the Update Bus. Address parity is passed to/from the internal address bus. Data parity is generated on writes through the Update Bus and passed on reads. Invert parity signals from the Special Function Maintenance Register can used to allow diagnostics to force address and data parity errors.

2.1.1.9 Dynamic RAM Controller (DRC)

The DRC device provides DRAM access, corrected data with per byte parity on reads, address parity checking, memory address checking, scrubbing of memory errors during refresh, refresh control, initialization with good hamming, a memory test and I/O registers for control and status of DRC functions. Accesses of the DRAM may be byte, word, long word, or burst, and the DRAM is accessible from the mate side. The DRC will be capable of handling 2, 4, or 6 banks of 16Mbytes each. The size and configuration of the on board memory is input to the DRC device through pins dedicated for this function. The DRAM is comprised of 4 banks of 10 4Mx4 memory devices making a total of 16M long words of system memory. Contained in each 40-bit long word is 32-bits of data, 7-bits of Hamming DRAM for error detection and correction, and 1-bit for memory address parity

2.1.1.10 Memory Expansion

There are three 72 pin sockets for DRAM Single In-line Memory Modules (SIMMs) located on the SBCORE. At least socket X1 must be equipped with the SIMM. For memory growth the sockets X2 and X3 are available. The SIMM to be used contains 32 Mbyte DRAM, configured as 8M long words with 8 bits used for EDC codes. For future memory designs, the DRC supports 4Kword (64 msec.) refresh timing. However, no mix of SIMM technology is possible. A SIMM memory sense indicator is available per SIMM socket to indicate the total amount of equipped memory.

2.1.1.11 I/O FPGA

The 32-BIT I/O FPGA implements the following functions:

- I/O Decoder - the purpose of the IO decoder is select all the registers which are used to validate the access with the right byte selects, IO lock/unlock, and read and write conditions.
- I/O State Machine - the purpose of the IO state machine is to link the IO 8 data bus to the 32 bits system data bus, do the byte alignment (68040 has no dynamic bus sizing) perform the long word access simulation to the flash EPROM and generate the IO-cycle timing to the bus controller for all IO and Flash accesses.
- Data and Address Parity Generator/Checker - the parity generator and checker functions calculate the address parity of every bus cycle and generate the data parity of all 32 bits-IO-data.
- Processor Control Registers Bus Control Registers - there are two processor control registers. These registers contain informations about the state of both this and the mate controller. It gives indications about the number of NMI's which have occurred and if controllers are running ore are in de stopped state.

- Bus Control Register (BCR) - the BCR is a register only accessible by this side of the controller. It is cleared on every NMI. The BCR controls the ability of the processor to access external resources and controls the ability of other resources to access this processor side (DMA, mate enable, etc.).
- Special Functions Registers - these registers are used to allow all kinds of maintenance operations to take place. Also access to this side only (local) or to the mate (mate) or to both sides can be forced by using these registers. The registers only fire in case there is a DATA cycle in progress.
- Address Data and Operations Shadow Registers - the address, Data and Operations Shadow register collect their information on every bus cycle. The address and Data registers contain the full 32 bits address and data of the cycle. The operations register collects information about timers, arbiter control, data/address parity errors, read or writes and if it was a local or mate or both operation. If in one of the bus-cycles an error is reported in the reset source register the contents of the shadow register is frozen until the reset source register is cleared. In the mean while, software is capable of reading the contents of the registers to determine what caused the failure.
- Reset Source Register and NMI Circuit - the reset source and NMI circuit is the final collection point of all the error information which can be generate in the MCTU3. It will generate an NMI if the errors are not masked or when a non maskable interrupt occurs like a sanity timer time-out.
- Software and Write Protect Circuits - the Software error source register captures software related errors reported via hardware check circuits. Each bit in the software error source register has the ability to be set by externally detected sources or by software. Each bit also has an associated mask bit in the appropriate mask register. If a mask bit is set, the error bit may be set, but the error does not propagate beyond the register. Unmasked bits set in software error source register report directly to the reset source register. The implementation of the write-protect circuitry together with the associated special function bits are the same as for the SMP20.
- Stack Protect Circuits - this circuit provides a mechanism for protecting the MCTU3 Stack region. This circuit prevents any writes to the Stack region that aren't to the active stack. Stack protection is the same as for SMP20.
- Interrupt and Terminating TEA Circuit - the purpose of this function is to allow the bus controller to generate a bus error (TEA to 68040) signal on those accesses which could cause the processor to read incorrect data. The TEA circuit only fires a signal to the bus controller if the required access is not allowed by means of mask bits set in the error source registers or when there is no bit already set in the reset-source register.
- Ready Time Out - this function prevents the system to be stuck in a never ending bus cycle. It times out every bus cycle taking longer than 56 usec.
- I/O Timers - the I/O timers provide a measure of control over accesses to I/O locations that have the capability to change the state of the processor. In SMP1, a single I/O timer ran for a fixed duration of approximately 114 ms. In SMP20, the I/O timer was modified to run for 256 bus cycles (not including DMA). Due to the large internal caches of the MC68LC040, and the ability for both processors to be executing code simultaneously and still access each other across the update bus, two I/O timers are provided.

  Additional UNLOCK2 and LOCK2 maintenance strobes are provided, for diagnostic capability, to access the other I/O timer from what would be accessed by the normal addresses.
- Sanity Timer - the sanity timer is a means to protect the controller for insanity. The sanity timer must be periodically strobed by the software. The maximum time on the sanity timer is 699 ms. If the sanity timer is not cleared before the time-out expires a sanity timer error is generated in the reset source

register. This error is not maskable. Also, after the sanity timer is cleared, it must not be cleared again until at least 233 ms. have elapsed, or again an error will be generated.

If a Power Fail indication is received from this processor's power control the sanity timer cannot be maintained.

- Reset Pulse Timer - the purpose of the reset pulse timer is to generate a well defined reset pulse to the processor to make sure all internal registers in the processor are cleared.
- Serial Control Interface 32-BIT I/O FPGA to 8-BIT I/O FPGA, and
- Fast Pump Bootstrapper - the Fast Pump Bootstrapper will provide the interface between the data link and the Switching Module Processor. One fixed PIDB per side is allocated for the Bootstrapper (BTSR) to transfer data in the idle time slots to the SBCORE memory. The assembled data is transferred under DMA control via the processor data bus to the SBCORE memory. The SBCORE duplex pump utilizes the pump protocol used in SMP20. The SBCORE Bootstrapper can be configured to pump the local, mate or both sides providing complete flexibility for pump configurations. The SBCORE BTSR hardware performs the following functions:

  1. Assembling of 32 bits words from any subset of the 32 PIDB time slots.
  2. Detection of the start of a pump block.
  3. FIFO buffering of incoming data with FIFO empty and overflow indication.
  4. Generation of a single level 6 interrupt after the first four 32 bit words are loaded in the FIFO.
  5. DMA control interface for transferring pump data to SBCORE memory.
  6. PIDB-In parity check to maintain the parity loop back function to support the walking parity on the PIDB-Out with a 29.5 time slot skew.
  7. Diagnostic Test PIDB is supported to test all operational BTSR modes.
  8. Diagnostic strobe point used to increment the internal time slot bit counter for verification of the correct PIDB synchronization.

  The BTSR receives serial data from a dedicated PIDB channel. Six data bits per PIDB time slot are used for transferring the pump data. With 32 used time slots per frame the transfer rate of downloading data is 192 Kbyte/sec. Any subset of time slots are allowed to be used for downloading pump data, however with a lower transfer rate.

  The SBCORE BTSR has three operational modes:

  1. interrupt,
  2. DMA, and
  3. resync mode.

  For maintenance the same three modes are available for diagnostic tests. The mode of operation is selected using the BTSR Control Register.

2.1.1.12 Timer-PIC-Controller (TPC) Device

To support all timer and counter functions, interrupt control and the CPI function, an ASIC was developed called TPC. The TPC ASIC includes the following functionality:

- One CPI gate-array - CPI provides the Administrative Module (AM) with a "hard-wired" path to the SM over which specific configurations can be forced within the SMP.

  A CPI message is received through a dedicated interface from the DLI or RS232 interface. The CPI selection between the DLI and Ethernet is made by placing the proper paddleboard on the MCTU3 backplane. In a VCDX, the CPI paddle board (982AAJ) should be used; otherwise a shorting berg will be provided which routes the DLI CPI information to the SMP.

- A CPI message consists of 1 start bit, 4 control bits, seven data bits, 51 parity bits and 1 stop bit, for a total of 64 bits. These are received serially, 1 per frame. The message requires 8 ms. to be received.

  Sixteen possible messages are available via the CPI mechanism. Eight are dedicated to diagnostic use, one is unimplemented and seven are operational messages. The operational messages are:

  1. Force Processor Reset (CPI message 7)
  2. Force Side 0 Active (CPI message 2)
  3. Force Side 1 Active (CPI message 1)
  4. Clear Force Active (CPI message 4)
  5. Disable Sanity Timer (CPI message 0xD)
  6. Enable Sanity Timer (CPI message 0xE)
  7. Enhanced CPI (CPI message 0xB)
  8. Update MSGS Status (CPI message 0x8)

  All CPI operational messages (except for Force Reset) generate a level 5 interrupt to the MC68LC040; diagnostic messages do not. Force reset generates an NMI to the microprocessor.

- 3 times AMD9519 Peripheral Interrupt Controller (PIC) functions - MCTU3 provides 24 maskable interrupts that generate a level 4 interrupt to the MC68LC040 microprocessor. These 24 interrupts are broken into two types. Sixteen interrupts are known as maintenance interrupts and have the highest priority. The remaining eight interrupts are of the operational type. When the I/O Timer is running the operational interrupts are blocked from causing the level 4 interrupt to the microprocessor.

  In general the layout of the interrupt controllers, PIC-A, PIC-B and PIC-C, has not changed from previous classic SMPs. This means that all three PIC's are cascaded with PIC-C having the highest priority.

- 2 times an Intel (82C54) Timer and counter device - All counters based on the 82C54 design are modulo 16 bit down counters. The programmable counters are an Intel 82C54 or equivalent device.

  1. 10 ms. Timer - Counter 0 of the first 82C54 device in the TPC is used as the 10 millisecond timer.
  2. Miscellaneous Timer - Counter 1 of the first 82C54 device in the TPC provides for the Miscellaneous Timer. The Miscellaneous Timer Circuit provides a programmable timer that may be used for two specific purposes within MCTU3. The output of the Miscellaneous Timer is connected to one of the interrupt inputs on the operational interrupt controller (PICA) in the maskable interrupt circuit. The second use of the Miscellaneous Timer Circuit is to provide a clock for the DLI 2x4 switch to provide a clock during certain maintenance test states.

3. 10 ms. Interval Counter - Counter 2 of the first 82C54 device in the TPC is used as the 10 ms. interval counter. The output of this counter in not connected. The user must read the value of the counter to determine the number of 10 ms. intervals. The clock in for counter 2 is the output of the 10 ms. interrupt timer.
4. Billing Counter - Counters 0 and 1 in the second 82C54 device in the TPC provide for the billing counter. The Billing Counter provides a 32-bit counter that is decremented by the DLI clock, so that the counter may provide a very accurate Time-of-Day clock for the system. It is implemented as two cascaded 16 bit counters to form a single, 32 bit counter clocked by a 8Khz clock provided by the DLI clock selection circuitry.
5. Second Miscellaneous Timer - Counter 2 of the second 82C54 device in the TPC provides for the Second Miscellaneous Timer. This Miscellaneous Timer Circuit provides a programmable timer that may be used within MCTU3. The output of the Miscellaneous Timer is not connected to anything and thus cannot provide an interrupt.

- IEEE 1149.1 (JTAG) Boundary Scan Test Access Port.
- 1.125 Mhz DLI clock output

2.1.1.13 DLI Interface

The DLI interface implements the following functions:

- DLI Serial I/O Control Interface - provides processor access to/from the Dual Link Interface (DLI) registers. The DLI Serial Interface hardware performs the following functions:
  1. I/O Address Decoder,
  2. DLI Read/Write Serial Interface,
  3. DLI Control Registers.
  4. I/O Address Decoder
- SDLC Channel Switches for DLI Link Selection -

A one of four selector is used for selecting the DLI receive data and clock to be transmitted to SDLC-A and SDLC-B. A demultiplexer function is used to transmit the SDLC-A data to one of the four DLI links. Per demultiplexer two bits are encoded to select the DLI link the data is transmitted to by SDLC A. The same function is also present for the SDLC-B data to transmit data to one of the four DLI links.

2.1.1.14 SDLC Parity Switch

The SDLC 2x4 Parity Switch is identical to the one used as the SDLC 2x4 Data Switch.

2.1.1.15 Sub Unit Interlace Bus (SUIB)

The interface signals for the SUIB are connected to the different Sub-units (e.g. Control Interface (CI), Time Slot Interface/Signal Processor (TSIU) and Packet Interface (PI)). Because the SUIB bus is a 16 bit data bus and the processor is a 32 bits bus multiplexing is performed by the QLWR chip. Data parity is generated on writes to the SUIB and is passed from the SUIB to the internal data bus on SUIB reads.

2.1.1.16 Flash EPROM

One 512Kbyte Flash EPROM is used for the generic firmware and another one is used to load the Flex and the FPGA devices during the power up initialization. Both devices are 5 Volt only programmable devices. This means that the write enables to the devices should be protected by HW to prevent unintended writes.

2.1.1.17 SBPCD and PIDB Interface

The PCD and PIDB interface provides input/output buffering for the SBPCD signals and the PIDB interface used for the on-board Fast Pump Bootstrapper (BTSR) function. The PIDB interface uses a differential line receiver and line driver. The line receiver is used to translate the differential input signals into TTL compatible output signals driving the BTSR function in the 32-bit I/O FPGA. The line driver translates the TTL output of the BTSR function into differentially driven PIDB output signals.

2.1.2 Dual Link Interface - TN1077F

The Dual Link Interface (DLI) function consists of one circuit pack per MCTU3 side and provides an interface to the NCT links. The DLI recovers clock and data from incoming NCT links and distributes the resultant clocks and data to the MCTU3. In the opposite direction, the DLI receives outgoing data from the MCTU3. The outgoing data is then multiplexed and sourced to outgoing NCT links. In each SM, two DLIs operate in a master/slave (active/standby) configuration.

The DLI consists of two Link Interface (LI) circuits:

1. a clock circuit, and
2. a control circuit.

Each LI interfaces with one pair of NCT links (outgoing and incoming) that provide 256 time slots to and from the SM. Of these 256 time slots, 255 are for voice and data paths to and from the MCTU3, and the remaining time slot is reserved for communications between the AM and the SMP (this time slot is referred to as the message time slot). The incoming 32.768 megabit/second data stream from the NCT link enters the receive (RCV) circuitry in the LI where it passes through a clock recovery circuit that derives a 32.768MHz clock from the data stream. This clock is then divided down by the RCV circuit for its own use and for use as a reference for the Phase Lock Loop (PLL) in the clock circuit. The RCV circuit "frames up" on the incoming data stream via a pseudo-random sequence inserted into the data stream at the source end of the NCT link. The incoming data stream is then converted to time slots and written into a buffer circuit (a RAM capable of containing one frame of data).

The TSI and message interface operate from clocks derived from the output of the PLL. When time slots are read from the buffer, parity is checked and regenerated. Normal voice and data time slots are sent to the duplex TSIs via nibble busses operating at 8.192 megabits/sec. The message time slot is sent to both the active and standby sides of the SMP via serial data links to the Synchronous Data Link Controller (SDLC). These data links operate at 48 kilobits/sec. The message time slot select switches (955B) provide the capability to select one of 256 time slots as the message time slot for NCT links A or B. When the MCTU3 is in a Remote Switching Module (RSM) environment, these switches are removed and the message time slot is selected by SMP software. However, in a minimally equipped RSM (two T1 lines), the switches are not removed, but the message time slots are forced to zero and one.

In the return direction, data is selected from one of the TSIs at the TSI interface and from one side of the SMP at the message interface for transmission to the TMS via the outgoing NCT link. These time slots are then multiplexed to provide a full frame of 256 time slots. In the transmit (XMIT) circuit, parity is checked and regenerated. The pseudo-random framing sequence that is generated in the control circuit is inserted (one framing bit per-time-slot). Finally, the time slots are converted to a 32.768MHz data stream and transmitted over the outgoing NCT link.

The clock circuit selects a clock reference from one of the two LIs (master mode) or from the mate DLI (slave mode). This selected clock is used as a reference for the PLL which, in turn, provides a reference voltage to the Voltage Controlled Crystal Oscillator (VCXO). The output of the VCXO is a 32.768MHz clock that is divided by the clock circuit and distributed to the remainder of the DLI, mate DLI, TSI and SMP.

The control circuit provides control for the various functions performed by the LIs and clock circuit. Errors from these circuits are latched into error source registers (ESRs) that reside in the control circuit. These control registers and ESRs are accessible for writing and reading by either side of the SMP via the SMP-DLI control interface. This interface is a 1.875MHz serial data link. The data bits that make up the commands are clocked in by the SMP, and the command is executed on the reception of a "go" signal received over a separate lead from the SMP. Parity over address and parity over data are checked in the control circuit. The control circuit provides a serial data link back to both sides of the SMP for read operations and an interrupt lead back to both sides of the SMP to indicate that an error condition exists. Each bit of the ESR can be inhibited from causing an interrupt via ESR mask registers.

Each DLI is in a failure group separate from the rest of the MCTU3 and is powered by an board mounted power module (984A). The power converter will interface to the control and display functions that are integrated onto the TN1077F. In a RSM environment the DLI will also include the Facilities Interface Unit (FIU) in its service group. In an Optically Remote switching Module (ORM) environment, the DLI will also include the Transmission Rate Converter Unit (TRCU) in its service group.

2.1.3 Time Slot Interchanger/Signal Processor - TN1086B

The Time Slot Interchanger/Signal Processor function consists of one circuit pack (TN1086B) per MCTU3 side that incorporates both the TSI and SP functions. An overview of the TSI/SP operation is presented here:

2.1.3.1 TSI

The primary data path delivers 512 peripheral time slots from the DIs to the RCV TSI RAM to be stored in consecutive order. Time slots are then translated from the RCV RAM and can be delivered to both DLIs on any of the 512 network time slots. In the opposite direction 512 network time slots from the DLIs are written consecutively into the XMIT TSI RAM. Time slots are then translated from the XMIT RAM on chosen peripheral time slots as instructed under software control and delivered to the DIs. Any peripheral time slot written into the RCV TSI RAM can be read out onto multiple (up to all) network time slots toward the DLIs. The same fanout capability is provided by the XMIT TSI RAM. A maximum delay in each direction of one frame (125us) can be introduced by the TSI.

Two DIs are connected to the TSI: one is dedicated to even TSI time slots, and one is dedicated to odd TSI time slots. Each DI provides 256 time slots to the RCV TSI RAM. Sixteen-bit time slots in nibble format are sent to the TSI by the DIs (PCM, A-G, and parity).

The TSI transmits 16-bit time slots in nibble format to the DIs. Of the A-G bits sent to the DIs, the E-G bits can either be sourced from the SP or from the alternate data RAM in the TSI. The A, B, C and D bits can either be sourced from the SP or passed through from the XMIT TSI RAM. All PCM data sent to the DIs passes through the Attenuation ROM. The attenuation ROM allows one of 31 values of digital loss to be inserted in the PCM data path on a per-time-slot basis. The loss values are 0dB through 15dB in 0.5dB increments. The integrity of the data path (TSI to peripheral unit to TSI) is protected by a walking parity scheme administrated by the TSI that inverts the parity sense of every ninth TSI time slot.

The TSI receives 512 time slots from the DLI via two 256 time slot nibble busses. The TSI selects which DLI (side 0 or 1) is the source of time slots to the TSI. This is accomplished by Automatic Time Slot Switching (AUTISS) that allows the TSI to switch its network data source on a per-time-slot basis between the active and standby sides of the system based on a validity marker (E-bit signaling stream) in each time slot. If AUTISSing occurs for 256 consecutive frames, the TSI outputs a 125us pulse that can be used to alert system software to the switching activity.

The TSI transmits 512 time slots toward both DLIs in the MCTU3. The time slots consist of sixteen bits in nibble format. The E bit of each time slot sent to the DLIs is set on a per-time-slot basis via a TSI control RAM written by SMP software. The A-D bits of each time slot sent toward the DLIs are either passed through from the RCV TSI RAM or sourced from a TSI control RAM.

Two forms of connections are possible between the XMIT and RCV RAMs. The first connection allows intramodule paths to be set up by looping time slots on the DLI side of TSI memories. A connection of this type will block an incoming time slot from the DLIs. The other connection allows intra-DLI connections to be made. A connection of this type will block an incoming peripheral time slot from reaching the RCV TSI RAM, but the blocked peripheral time slots will still have access to the SP and LDSU.

The Alternate Data RAM (ADR) provides the SMP and LDSU with access to the contents of all 512 time slots. By means of the ADR the SMP can write constants (e.g., idle code) to be sent to the DIs and DLIs, and sample time slots at various points within the TSI. The ADR also provides SMP access to the E bits received from the DLI. Parity errors on time slots received by the TSI from the DIs are reported to the SMP via the ADR. Data stored in the ADR (e.g., tones from the LDSU) can be sent to the DIs, to the RCV TSI RAM, or to the XMIT TSI RAM. The TSI time slots written to the ADR can be sourced on a per-time-slot basis from four different locations in the TSI. This permits maintenance access and allows time slots from both DIs and DLIs to be sent to the LDSU.

2.1.3.2 SP

The SP performs hit timing on all signaling and control bits received from the TSI. This hit timing is performed by scanning the data at a 3 ms rate. A time slot is considered to have changed to a new state only if the bit persists in that state for two consecutive scans.

Hit timing is accomplished by comparing data on the incoming selected TSI time slot with data contained in the Last Look RAM (LLR). The LLR contains the values of signaling and control bits from the selected TSI time slot during the previous 3 ms scan. Every 3 ms all 512 time slots are hit-timed and if a bit has remained the same for two consecutive three-ms scans it passes the hit timing algorithm.

The state of all signaling and control bits received by the SP from the TSI are stored after hit timing in the Last Report RAM (LRR). Through the LRR, the SMP has access to the most recent hit timed state of all signaling and control bits of all time slots received by the TSI from the peripheral units and all signaling and control bits whose state, after hit timing, has changed. The SP is also capable of storing (in a SMP-readable FIFO) the peripheral time slot number.

State change calculations are based on the result of the hit timing circuit, the ignore RAM, and the LRR.

The ignore RAM, set by SMP software, indicates on which bits of which time slot state change reports should be made. The LRR contains previously calculated states of all signaling and control bits after hit timing. If a new time slot bit has passed the hit timing algorithm, i.e., has not changed during the last 3 ms, it is compared to the state stored in the LRR. If a change has occurred, the LRR is updated. If the bit being processed is not set to the ignore RAM and if there is a change from the state contained in the LRR, the new bit value is written into the report FIFO. All changes for one time slot are collected before the FIFO is written. The FIFO is readable by the SMP.

The signaling and control bits (A, B, C, D, E, F, and G) are transmitted to the TSI for all 512 peripheral side time slots every 125us. These signaling bits are read from a 512 time slot RAM designated as the M RAM. The M RAM is both writable and readable by the SMP.

2.1.3.3 TSI-SP Interface

The TSI sends the seven signaling bits (A-G) of all 512 time slots received from the DIs to the Signal Processor. The time slots consist of two consecutive 4-bit nibbles and are accompanied by an 8.192-MHz clock and a 6 ms sync pulse. In the opposite direction, the TSI receives the seven signaling bits (A-G) from the SP for all 512 outgoing peripheral time slots. The TSI has the ability to send the E, F, and G bits from either the ADR or the SP to the DIs. The A through D bits are selectable as a group. They can either be passed through the TSI from the DLI or can be selected to be sourced by the SP. Even parity is used on the even time slot bytes and odd parity is used on the odd time slot bytes.

2.1.4 DATA INTERFACE - TN1377/TN1524

The Data Interface (DI) function consists of two circuit packs per MCTU3 side and provides an interface between the TSI and various peripheral units in the SM. In a domestic application the TN1377 circuit pack is used. In an international application, the TN1524 will be used in place of TN1377. This circuit pack is identical in function with the only difference being sourcing a different idle code bit pattern.

In the incoming direction, the DI performs a multiplexing function by combining time slot traffic of several peripheral units onto a single bus for the TSI. In the outgoing direction, it demultiplexes a single bus from the TSI to various peripheral units. The DI communicates with each peripheral unit over a peripheral interface data bus (PIDB). Each of these busses consist of four signals: serial data in, serial data out, a 4.096MHz clock, and an 8KHz sync. The data in and out operate at 4.096 megabits/second, carrying 32 time slots per frame, with 16 bits per-time-slot. Up to 16 PIDBs may be connected to the DI, with each PIDB carrying traffic to a service group in one of the peripheral units. The DI passes data to and from the TSI over nibble busses. These busses operate at 8.192 megabits/second carrying 256 time slots per 125us frame (two DIs, each connecting 256 TSI time slots, are needed to carry traffic for the 512 time slot TSI). With 512 peripheral side time slots (16 PIDBs x 32 time slots) and 256 TSI side time slots, the DI can perform a 2:1 concentration function. All PIDBs operate in synchronization. In the time of a single PIDB time slot, eight time slots are sent and received from the TSI. After a single time slot from all 16 PIDBs has been clocked into the DI, up to eight of those are chosen (via control information received from the TSI) to be inserted into eight time slots to the TSI. The time slots not selected are blocked and lost. If less than eight are chosen, "1s" are sent on the nibble bus to the TSI in the time slots for which no PIDB time slot was connected.

In the outgoing direction, the TSI provides eight time slots to the DI during a single PIDB time slot period. These eight time slots are connected, again using control information received from the TSI, to eight of the 16 PIDBs. PIDBs not selected to receive TSI data transmit idle code to peripheral units. All eight TSI time slots need not be connected to a PIDB time slot. If less than eight are to be connected to PIDBs, the control information from the TSI associated with the "unused" TSI time slots informs the DI to ignore that incoming time slot. All unselected PIDBs transmit idle code. In this case, more than eight will do so.

In addition to the nibble bus in and out of the DI from the TSI, the DI also receives from the TSI an 8.192MHz clock, an 8KHz sync pulse, four address leads, a board select lead, and two leads used for diagnostics. The 8.192MHz clock provides all the timing for processes internal to the DI; it is used also to generate the 4.096MHz clock for the peripheral units. The 8KHz sync pulse properly synchronizes the DI to the network and generates the sync pulse to peripheral units. The address leads indicate, on a per-time-slot basis, to which PIDB a given TSI time slot is to connect. The address is used by the DI both for the TSI-to-PIDB demultiplex function, and for the PIDB-to-TSI multiplex operation. The board-select lead informs the DI, again on a per-time-slot basis, whether to connect the TSI time slot to the PIDB, as determined by the address, or to ignore that time slot and make no connection to it. The diagnostic leads are used to loop data received from the TSI through the DI circuit and back to the TSI. These leads also provide the capability of having the DI loop idle code back to the TSI rather than the received TSI data. Maintenance of the DI, as well as of the PIDB and parts of the peripheral units, is performed by the TSI by means of the walking parity scheme.

2.1.5 CONTROL INTERFACE - UN71C

The Control Interface (CI) function consists of one/two circuit pack(s) per MCTU3 side and provides an interface between the SMP and various peripheral units for control information. This interface is called a Peripheral Interface Control Bus (PICB). Up to 23 PICBs are available with each CI. Either one or two CIs may be equipped in the MCTU3 thereby, providing a maximum of 46 PICBs. Each PICB contains five twisted-wire pairs that carry clock, output data, input data, SMP select information, and peripheral unit service requests.

The CI to SMP interface is through the Sub-Unit Interface Bus (SUIB). This bus is a parallel, 16-bit bidirectional data bus with a 6-bit address bus. The CI contains several registers that are accessible by the SMP through this bus. The CI performs four functions for the SMP:

1. Permits the SMP to write 16 bits of information to a peripheral unit register (maximum of 256 destination registers).
2. Permits the SMP to read 16 bits of information from a peripheral unit register (maximum of 256 source registers).
3. Receives, latches, and reports service requests from peripheral units.
4. Detects and reports CI operational errors.

The CI reads and writes peripheral registers through an exchange of serial messages over the PICB. A distribute operation writes 16 bits of data into a peripheral unit destination register. A scan operation reads 16 bits of data from a peripheral unit source register.

The SMP will initiate all scan and distribute operations. In all scan and distribute operations, the peripheral unit will send a reply message back to the CI. In the reply message there is a 3-bit All Seems Well (ASW) code. These bits are used to report errors detected by the peripheral unit. If errors are detected during a scan or distribute order by either the CI or a peripheral unit, the error will be reported by latching a bit in the error source register. The interrupt lead to the SMP will become active if an error occurs, the ability to inhibit this interrupt on a per-PICB basis is provided.

In addition to performing scan and distribute orders, the CI reports peripheral unit service requests by latching an active state on the PICB interrupt lead into the interrupt source registers. Inhibit registers (remote interrupt inhibit registers) are provided such that these service requests may be handled by interrupts or polling.

The UN71C differs from its predecessors by having a "multiscan" functionality which scans all 23 PICB's simultaneously. This capability is not supported in the MCTU3 environment.

2.1.6 PACKET INTERFACE/2 - TN1042/UN395

The Packet Interface (PI/2) function consists of one circuit pack per MCTU3 side and provides an interface between the MCTU3 and the Packet Switch Unit (PSU). The PSU implements Integrated Services Digital Network (ISDN) capabilities on the 5ESS Switch. The main function of the PI is to buffer signaling packets between the PSU Protocol Handlers (PHs) via the Packet Bus (PB) and the MCTU3 via the SUIB.

Resident on the PI is circuitry that interfaces to the SUIB and a Port Processor (PP), which transmits and receives packets between the MCTU3 and PHs. The PP design is common to the PI and PH. The signaling packets are FIFO buffered in a 1M byte dual port memory of the PP circuitry. The PP controls Port A of the dual port memory and transfers the signaling packets across the PB. Port B of the dual port memory transfers signaling packets to/from the MCTU3 over the SUIB.

2.1.6.1 Packet Interface Model 2 - UN395

The PI2 is essentially an enhanced version of the PI with improved performance and the ability to support multiple PSU/PSU2 complexes. The PSU2 has been developed for improved packets throughput for existing PSU features (ISDN), and for a feature for wireless referred to as Code Division Multiplexed Access (CDMA). The PI2 is architectonically the same as the PI and provides the basic PI function which is to buffer signaling packets between the PSU/PSU2 and the MCTU3.

The current PI supports one 10Mbps PSU complex. The PI2 can support up to two PSU complexs at a 10Mbps packet bus rate (PSU) or at a 100MBps packet bus rate (PSU2). The PI2 provides the buffering of signaling packets between the PSU complexes (PSU, PSU2) via the packet bus (PB) and from the MCTU3 via the SUIB. Resident on the PI2 is a 68040 based core design which administers the transmission/receiving of signaling packets to/from the PSUs via PBMAC devices and the arbitration of the sending receiving packets to the MCTU3 via a 1M byte FIFO Dual port static RAM.

2.1.7 LOCAL DIGITAL SERVICE UNIT - TN833

The Local Digital Service Unit (LDSU) function consists of one circuit pack per MCTU3 side and provides tone decoding, tone generation, voice path assurance and other features. The LDSU is implemented on one circuit called the Digital Service Circuit (DSC). Four slots in the MCTU3 are reserved for DSCs; each position represents a service group with the ability to provide a combination of all of these features. Initially, only two service groups will be used. The LDSU operates in a load-shared configuration, rather than in an active-standby mode. This means that each in-service board will handle a portion of the load. If two boards are active and one of these should fail, the capacity to perform LDSU features is decreased by fifty percent.

Each service group has a separate interface to the TSI and the CI. The interface to the TSI is via the LDSU Bus (LDSUB). This interface is functionally the same as a PIDB however, the data on the LDSUB has direct access to the TSI and does not pass through the DI. Data, typically PCM tones, and signaling bits are transmitted in both directions over the LDSUB, while clock and sync are only transmitted to the LDSU. The interface to the CI is through a standard PICB. It carries the control and status information for the board and also provides the path used to download the resident software from the SMP to the DSC.

The LDSU is one of many functions which may be overlaid on the flexible architecture of the DSC. The major functional components of the design are:

- Logical Processor (LP)
- Memory
- Unified Control Interface (UCI)
- Serial Data Interface (SDI)
- Digital Signal Processor (DSP)

The DSC may be viewed as a multi-processor system where the LP, an Intel 80188, provides the logical control for the board and orchestrates the actions of the DSPs. The architecture of the DSPs is particularly suited to the tasks of performing the algorithms needed to provide digital services. The LP determines what jobs need to be accomplished, typically per a requests from the SMP, then configures the DSPs to fulfill those requests. The LP is also responsible for performing audits and checks of both the hardware and software on the board.

The LP executes programs stored in 256K bytes of DRAM while the DSPs execute programs out of 4K bytes of on-chip RAM. The DRAM address range is divided into four write-protectable regions. On memory writes, parity is generated over seven bits of address and eight bits of data and stored in a single 256K x 1 DRAM. When the data is read from the memory, the parity is again generated and then checked against what had previously been stored. Parity and write-protect errors are reported to the SMP and the LP through the UCI.

The primary function of the UCI is that of a control interface. It provides error reporting and communication between the DSC and the SMP through the PICB. It is the source of interrupts to the SMP for peripheral service requests. This is accomplished through several maskable sources contributing to a single summary scan register. The summary scan register is sixteen bits wide; eight bits request normal service and eight bits indicate detected errors. It include mailboxes and FIFOs for message passing. The mailbox consists of a RAM and a set of maskable mailbox flags. Using these, the SMP may communicate bi-directionally with the LP in a synchronous manner. The FIFOs consist of two FIFO controllers used to read and write first-in-first-out buffers in the UCI RAM. This provides asynchronous communication between the SMP and the LP. A fault insertion register is provided for maintenance.

Two SDI devices are used on the DSC. The SDIs are essentially micro-time-multiplexed-switches. They provide the interface between the DSC and the TSI through the LDSUB. They provide data paths between the DSPs and the TSI. The SDIs transmit and receive thirty-two time slots of data from each DSP and the TSI. The column of multiplexers responsible for switching the data is controlled by an internal RAM which is accessible only to the LP. When the LP assigns a DSP to a task it must be able to direct the data to or from that DSP.

The DSC performs complex functions as a whole, but it may be viewed as a set of individual pieces each performing a more specific and straight-forward task. There is a control processor, a set of number-crunching DSPs, a bank of memory and its associated control, and finally the control and data interfaces.

2.1.8 POWER CONTROL/DISPLAY - TN1424/TN1425

2.1.8.1 Functional Requirements

The SBPCD can be broken down into the 17 subfunctions listed below:

- Power Supply 5 V, 150 W (TN1424)

  Power Supply 5 V, 150 W and 3.3 V, 33 W (TN1425).
- Converter Control Interface.
- Converter/Fuse Alarm Interface - In addition to making use of the existing interface provided in all affected units, the SBPCD must provide an interface to detect and report unequipped converter(s).
- Scan Points Interface - The scan points interface must be compatible with the TTL interface used in the SM and the SCSDC Interface used in the IOP.
- Distribute Point Interface - The distribute point interface must be compatible with the TTL interface used in the SM and the SCSDC Interface used in the IOP.
- Request In Progress.
- Out Of Service.
- Mate Power Fail Interface.
- Power Fail/Manual Off Control.
- Manual Override Control.
- Request Out Of Service/Request Restore.
- Periphery Fuse Alarm Interface.
- Diagnostic Control.
- Auto Power Restart.
- SM2000 auto power shutdown.
- Low voltage detection -48V.
- RSM stand-alone and sanity lamps interface.

2.1.8.2 Software Interfaces

The SBPCD has three distribute points used for software control of the OOS-LED, RQIP-LED, and diagnostics.

Setting any of the distribute points to a "1" activates the respective function. When the RQIP, OOS, and diagnostic distribute points are all set to a "1", the Diagnostic, W, X, Y, and Z scan points are forced to the off-normal state. Clearing any one of the distribute points causes the scan points to return to their original state.

2.1.8.3 Converter/Fuse Alarm Detection

The state of an external converter (on/off) is indicated by a relay contact located within the converter (contact open indicates converter on, contact closed indicates converter off).

An interlock loop is provided to detect a missing external converter. The interlock loop starts at the INT terminal, which has -48V source on it, goes to each external converter which complete the path with two terminals shorted together inside the external converter, and return to the INTR terminal, which is connected to -48RTN. The interlock loop therefore grounds terminal INT when all converters are present and allows -48V to be at INT when one or more external converters are missing.

A fuse failure results in a -48V source being applied to the fuse alarm bar located in the fuse block. The fuse alarm bar is also connected to the SBPCD alarm input. The fuse alarm for the SMC cabinet equipment is connected to the ALARM terminal.

2.1.8.4 Scan Points Interface

2.1.8.4.1 Mate Power Fail Scan Point

The presence of -48V on the SBPCD alarm input activates a scan point to be used for the force active function in an SM.

2.1.8.4.2 Extra Scan Point

An extra scan point is provided that is activated in case the signal "EXIN" is tied to -48V via a resistor.

2.1.8.5 Converter Control Interface

Maintaining a connection between control leads RS2 and RS3 keeps the on-board and external converter(s) (if present) in the power up state.

2.1.8.6 Out Of Service (OOS)

Activating the OOS distribute point operates the OOS-LED. In addition, activating the OOS distribute point bypasses the MOR-SWITCH allowing manual power down of converters using only the OFF-SWITCH and disables the V scan point preventing a manual power off from activating the scan point.

Releasing the OOS distribute point extinguishes all OOS-LEDs, enables the V scan point, and requires MOR be used with OFF to manually power down a converter.

The MOR-SWITCH must be used with the OFF-SWITCH to manually power down an SBPCD failure group that does not have it's OOS-LEDs active. Manually powering down a failure group in such a state activates the V scan point. Once activated, the V scan point is released by depressing the ON-SWITCH.

2.1.8.7 Periphery Fuse Alarm Interface

A periphery fuse failure results in a -48V source being applied to the fuse alarm bar in the fuse block.

2.1.8.8 Auto Power Restart

The Auto Power Recovery (APR) is an optionable requirement since the US market is not allowed to have hardware auto-startable. For the International market, particularly where AC power is unreliable or battery power reserve is exhausted, the auto recovery feature is required. Therefore, auto recovery is a requirement for International markets, but must be an option for the US market. To be compliant, both the hardware and software are required to automatically recover to specifications after -48Vdc power is restored following a major power outage. A major power outage is a state in which commercial AC power is not present, office battery is in deep discharge, and backup (diesel) power is not available. This feature also provides automatic recovery for short duration, transient power losses, possibly due to exchange technician errors. If primary power (-48V) falls below 39V the following takes place:

- All on-board converter(s) and external converter(s) (if present) are powered down. The OFF-LED and ALM-LED are both lighted.

If primary power (-48V) rises above 39V the following takes place:

- All on-board converter(s) and external converter(s) (if present) will start immediately. If after one second an alarm is still present all converter(s) are shut down.

2.1.8.9 On-board Converter Control

A circuitry was made to avoid a voltage gap between the 3.3V and 5V, exceeding 4 Volts. In case the OFF-SWITCH (and MOR-SWITCH if required) is depressed or an on-board power converter alarm becomes active the on-board power converters are triggered to shutdown. In case of a short current of the 3.3V the on-board power converters are switched off, but no guarantee can be given concerning the difference in voltage between the 3.3V and 5V output voltage remains <=4V. Also it is not possible to start the power modules in case the lever-switch is not in the right position.

2.1.8.10 Over-Current Control and Power Modules

2.1.8.10.1 5V Power Converter

The 5V is delivered by a FE200-series Power Module; dc-dc converters; 48Vdc input. The module is capable of supplying 5V, 200W but due to derating the TN1424 is capable to supply 5V, 150W. The output voltage is adjusted to 5.1V in order to compensate for a possible voltage drop between SBPCD and the consuming cards. The sense leads of the power modules are connected to the output voltage of the power module at the backplane. So the voltage drop across the connector will be compensated.

2.1.8.10.2 3.3V Power Converter

The 3.3V is delivered by a FE200-series Power Module; dc-dc converters; 48Vdc input. The module is capable of supplying 3.3V, 200W but due to derating and lack of backplane pins the TN1425 is capable to supply 3.3V, 33W. The output voltage is adjusted to 3.4V in order to compensate for a possible voltage drop between SBPCD and the consuming cards. The sense leads of the power modules are connected to the output voltage of the power module at the backplane. So the voltage drop across the connector will be compensated.

2.1.8.10.3 Over-Current Control

The current programming for the 5V and the optional 3.3V are combined in one circuit. This circuit measures the total delivered current. In this situation only one current programming resistor, which reflects the total consumed current (3.3V and 5V current), is needed on the consuming circuit packs. In case more than the programmed current is consumed the 5V and the optional 3.3V on-board converters are shut down.

2.1.8.11 Alarm Detection and Converter Interface

A circuitry is made to detect a fault in the output voltage/current of the SBPCD. In case signal "ONINV" is activated for one second, a momentary connection is established between converter control leads RS1 and RS2 (for one second) causing the on-board converter(s) and external converter(s) (if present) to power up. However in case after one second an alarm is still present, the on-board converter(s) and external converter(s) (if present) are turned off. The RS1 and RS2 connection can support a minimum of 19.5 mA.

2.1.8.12 RSM Stand-alone and Sanity Lamps Interface

In case signal "ONINV" is activated for one second, a momentary connection is established between converter control leads RS1 and RS2 (for one second) causing the on-board converter(s) and external converter(s) (if present) to power up. However in case after one second an alarm is still present, the on-board converter(s) and external converter(s) (if present) are turned off. This circuit interfaces between the coreboard and the RSM control monitor display circuit which provides both a stand-alone and a sanity indicator. This circuit was copied from the UN516B and for that reason there is no longer the need to supply the coreboard with -48V. A scan point is provided to inform the system software that a low battery condition exists. The detector is activated in case the -48V power is below the level of 44 volts. In that case the LOW-SCR is no longer triggered and is deactivated. Also a circuit is present which detects the 39 Volts level. If the -48V power is below that level the on-board power converter(s) and the external converter(s) (if present) are switched off.

2.2 EXTERNAL INTERFACES

In SD-5D536-01 external interfaces consist of cables connecting MCTU3 functions to other 5ESS equipment and are referenced as CAD 1 with individual element identifiers.

2.2.1 User Intervention Interface

This interface is used when the MCTU3 is used in a RSM environment. The element identifiers AC and DY of CAD 1 are the interconnections between the SMP and the Multi Module RSM (MMRSM) alarm and status unit (ED-5D586-01). The MMRSM alarm and status unit allows the following User operations of the SMP:

- Force either side of the SMP active.
- Monitor the status of communication between the RSM and the host by indicating the state of the links between them.

- Monitor the status of the SMP by indicating the current state of sanity in each processor.

2.2.2 DLI Control and Display Interface

In a RSM environment, the FIU will become part of the DLI service group via cables installed at the locations specified in element identifier DI and IF of CAD 1. In an ORM environment, the TRCU will become part of the DLI service group via cables installed at the locations specified in element identifier DI and IF of CAD 1. In a SM environment, 982JJ shorting bergs will replace these cables to provide a path from the DLI converter back to its control and display functions.

2.2.3 DLI Fuse Alarm Interface

The DLI fuse alarm interface consists of signals between the DLI alarm circuitry, FFU and the CS1 circuit pack of the SMP. The interface is used to monitor blown fuses. When a DLI 70-type indicator fuse is blown, the fuse connects -48 volts to a signal used to light a red alarm LED on the FFU, the cabinet bezel and on the DLI circuit pack. The DLI alarm circuitry informs the SMP of the fuse alarm through two scan points. The SMP monitors the scan points and will take appropriate recovery actions if they become active. The SMP can test continuity of the DLI fuse alarm circuitry and its connection to the FFU through a combination of three distribute points. The element identifiers in CAD 1 for DLI fuse alarms are DH and IE.

2.2.4 Revertive Pulsing Interface

If the SM is equipped for revertive pulsing the DSC circuit packs are removed from the MCTU3 and a Digital Service Unit (DSU) is installed in the SM. The MCTU3 DSC slots are cabled to the DSU. The element identifiers in CAD 1 for DSU cabling are DQ, DR, DS, DT, IP, IQ, IR, ans IS.

2.2.5 Fan Unit Scan and Distribute Interface

A fan failure is reported to the SMP through a scan point from the Six-Fan Unit to the SBCORE circuit pack. When a fan fails a scan lead becomes active and is used to light a red the Six-Fan Unit and a yellow alarm LED on the cabinet bezel. The SMP monitors this scan point and will take appropriate recovery actions if the scan point becomes active. A fan alarm can be retired by SMP software using a distribute point or by manually through a push button located on the rear of the Six-Fan Unit. The Six-Fan Unit scan and distribute interface appears in element identifier AA and DW of CAD 1.

2.2.6 MCTU3 Controller Fuse Alarm Interface

The controller fuse alarm interface consists of signals between SBPCD alarm circuitry and the FFU. The interface is used to monitor blown fuses. When a MCTU3 controller 70-type indicator fuse is blown, the fuse connects -48 volts to this signal used to light a red alarm LED on the FFU, the cabinet bezel and on the SBPCD circuit pack. The mate SMP monitors the scan points and will take appropriate recovery actions if they become active. The SMP also monitors fuse alarms from peripheral units through Z scan point. The SMP monitors the Z scan point and will take appropriate recovery actions if it becomes active. The SMP can test continuity of the MCTU3 controller and peripheral fuse alarm circuitry and its connection to the FFU through a combination of three distribute points. The element identifiers in CAD 1 for controller fuse alarms are AB and DX.

2.2.7 Peripheral Interface Data Bus (PIDB)

A PIDB provides the physical link for PCM data between the DI and any connected peripheral unit. It consists of four balanced, differentially driven, RS422 compatible, twisted wire pairs. The PIDB carries 4.096 megabit/second serial data from the DI to the peripheral units, a 4.096MHz clock and 8KHz sync to the peripheral units, and 4.096 megabit/second serial data to the DI from the peripheral units. The twisted pair carrying data from the periphery is terminated at the DI.

The 4.096MHz clock has a 244-ns period. The duty cycle of the clock, excluding this +-20 ns is 50% +-5%. The 8KHz sync is a normally high signal ("1" state) that pulses low for one 4.096MHz clock period every 125us. The peripheral units should clock PIDB data in from the DI on the falling edge of the 4.096MHz clock, and clock data out onto the PIDB on the rising edge of that clock.

During the sync pulse, the peripheral should clock PIDB time slot No. 29, bit 7 in from the PIDB on the negative edge of the 4.096MHz clock and clock out PIDB time slot No. 31, bit 15 onto the PIDB using the positive edge of the clock. Note the 2 1/2 ns time slot skew between incoming and outgoing information - this is caused by the skew required by the TSI and DI to perform their functions.

A peripheral unit service group will receive a PIDB from each side of the duplex MCTU3. In a fully operational SM, data will flow over both PIDBs. Using control information received from the SMP via the CI, the peripheral unit will select only one PIDB from which to receive information. However, it will transmit the same data back over both PIDBs. The skew of the two PIDB clocks received from the duplex SM can be up to +-60 ns.

The elements identifiers of PIDB interfaces in CAD 1 are: CC, CD, CE, CF, CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CR, CS, CT, CU, CV, CW, CX, CY, CZ, DA, DB, DC, DD, DE, DF, DG, FY, GA, GB, GC, GD, GE, GF, GG, GH, GI, GJ, GK, GL, GM, GN, GO, GP, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, IA, IB, IC, and ID.

2.2.8 Peripheral Interface Control Bus (PICB)

A PICB consists of 5 balanced, differential driven, RS422 compatible, twisted pairs. The clock pair carries a 2.048MHz gated clock signal to the peripheral units. The data out pair carries serial information to the peripheral units from the CI. The data in pair carries serial data from the peripheral units to the CI. The select pair carries signaling information which is used to select the active side CI and the interrupt pair transmits service requests from the peripheral units to the CI.

Although the cable length of the PICB may vary, it has a maximum limit of 20 ft. Data is to be gated in and out of the peripheral unit on the negative edge of the clock. To avoid a timeout error, the reply must be received by the CI within 21.5us from the first clock pulse.

The elements identifiers of PICB interfaces in CAD 1 are: AE, AF, AG, AH, AI, AJ, AK, AL, AM, AN, AO, AP, AQ, AR, AS, AT, AU, AV, AW, AX, AY, AZ, BA, BB, BC, BD, BE, BF, BG, BH, BI, BJ, BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU, BV, BW, BX, BY, BZ, EA, EB, EC, ED, EE, EF, EG, EH, EI, EJ, EK, EL, EM, EN, EO, EP, EQ, ER, ES, ET, EU, EV, EW, EX, EY, EZ, FA, FB, FC, FD, FE, FF, FG, FH, FI, FJ, FK, FL, FM, FN, FO, FP, FQ, and FR.

2.2.9 Packet Switch Unit (PSU/PSU2) Interface

The PB is a duplexed bus connecting the PI/PI2 to the PSU or PSU2 complex. A PI only supports a 10Mbps PB, whereas the PI2 supports both 10Mbps and 100Mbps PBs. The following paragraphs describe the 10Mbps and 100 Mbps packet bus interface. For the 10Mbps interface six differentially balanced signals are used:

(a) Clear To Send

(b) Transmit/Receive Data

(c) Request To Send

(d) Receive Clock

(e) Transmit Clock

(f) Carrier Sense

For 10Mbps communication, the PSU provides the receive clock which is looped on the PI/PI2 back to the PSU (transmit clock). If the PI/PI2 is transmitting a signaling packet to the PSU, the PI/PI2 will issue a request to send. The PSU responds by sending carrier sense and clear to send and the PI/PI2 transmits the signaling packet. If the PSU is transmitting signaling packets to the PI/PI2, the PSU sends carrier sense and receive data are sent to the PI/PI2.

For the 100Mbps interface eight differentially balanced signals are used:

(a) Clear To Send

(b) Two - Transmit/Receive Data

(c) Receive Clock

(d) Transmit Clock

(e) Carrier Sense

For 100Mbps communication, the PSU2 provides the receive clock which is looped on the PI2 back to the PSU2 (transmit clock). If the PI2 is transmitting a signaling packet to the PSU2, the PI2 will issue a request to send. The PSU2 responds by sending clear to send and the PI2 transmits the signaling packet. If the PSU2 is transmitting signaling packets to the PI2, the PSU2 sends receive data to the PI2.

The elements identifiers of the PSU interface in CAD 1 are: BW, BX, BY, BZ, FS, FT, FU, and FV.

2.2.10 DLI-TRCU Interface

This interface is used when the MCTU3 is in an ORM environment. The four NCT links between the TRCU and the DLI's are implemented with a short (less than 2 feet) shielded, twisted pair cable. The NCT to D3 Rate Converter (NDRC) circuit pack in the TRCU produces an 8KHz reference signal by dividing down the incoming 45 MHz clock. This signal is sent to the DLI to be used as a reference for its phase locked loop. Each of the four NDRC circuit packs provides an 8KHz reference signal with only one being selected by the two DLI's. In the NDRC circuit pack those references not selected are synchronized to the reference that is selected.

Two leads from its associated DLI provide an indication to an NDRC circuit pack whether its reference has been selected as the phase locked loop input. One of these leads indicates whether a particular DLI is master or slave, and the other indicates whether the A or B link is being used as a reference. The NDRC circuit pack also produces an out-of-frame output. This output indicates whether the NDRC circuit pack can frame up on the incoming 45 Mb/s signal. This signal is sent to the DLI where it is used to force the phase locked loop to free run if the 8KHz signal to which it is locking is produced by a clock derived from a bit-stream that the NDRC circuit pack can not frame up on. The power control and display function for the power converters in the TRCU is provided by the power control and display circuitry in the DLI's.

2.2.11 Fiber Optic NCT Link Interface

This interface is used when the MCTU3 is in a SM, TRM or RSM environment. The serial data received and transmitted over the NCT links is at a 32.768MHz rate. The DLI will track the received serial data up to +-1KHz of the nominal frequency (+-32 PPM). Each frame consists of 256 16-bit time slots. Bits 0 through 7 are PCM data bits in the 255 voice and data time slots. Bits A through E are signaling bits. The G bit is the bit position into which the pseudo-random framing sequence is inserted. The F bit is toggled at the beginning of each frame and is used for fault detection in the DLI-TMS interface. The P bit is such that the 16 bits of the time slot have odd parity. In the message time slot, bits 0 through 5 are the data bits that contain data to/from the SMP; bit 7 is the CPI bit.

The fiber optic NCT links for the SM and RSM appear in element identifier IT, IU, IV, IW, IX, IY, IZ, and JA of CAD 1. The fiber optic NCT Links for the Two Mile Optically Remote Switching Module (TRM) appear in element identifier DM, DN, DO, DP, IJ, IK, IL, and IM of CAD1.

2.2.12 DLI External Clock Enable

There is a cable that can bring in an external clock to the DLIs in APR or non-APR applications. The element identifiers of the enable are DL and II.

2.2.13 DLI Time Slot Selection Switches

Each DLI has two message time slot registers for the A and B NCT links. Each message time slot register has two modes of operation: software programmable and backplane programmable. The backplane programmable mode is selected by plugging 955B message time slot select switches onto the MCTU3. The backplane switches ground the message address enable lead allowing the switches to indicate an 8-bit binary number corresponding to the NCT link time slot used for transmitting messages to and from the SMP and AM. After the switches are removed, the address enable lead is pulled high and the message time slot number can be programmed by the SMP writing to the message time slot address registers of the DLI. The elements identifiers of the DLI Time Slot Selection Switches are DJ, DK, IG, and IH.

2.2.14 Ethernet Interface

There is an optional interface between the SBCORE and the Ethernet Paddle board, which provides a "Thin Ethernet" as specified in IEEE 802.3 10BASE2 standard. The Ethernet Interface board is a paddle board of the 982 type (982AAH) and is located at the back of the MCTU3 backplane at the lower part of the connector of the core board KBN17 (row 300 and 400). The board contains one coaxial Ethernet connection that interfaces with the MC68360 QUICC communications controller at the Core board. The elements identifiers of Ethernet Paddle board interfaces in CAD 1 are AD and DZ.

2.2.15 Feature Enable Straps

Auto-Power Restart (APR) is enabled for the SMP and DLI via shorting straps (switch). The elements identifiers of APR enable interfaces in CAD 1 are CA and FW.

Additional features such as Administrative Work Station (AWS), RSM, T1 - 30 channel or 24 channel, and undefined future features are enabled via shorting straps (switch). The elements identifiers of Additional features enable interfaces in CAD 1 are CB and FX.

2.2.16 CPI Interface

A CPI Paddle board (982YN) translates the messages sent over the RS232 message interface into CPI compatible messages for termination in the MCTU3. The paddle board physically mounts in the backplane of the MCTU3 unit and directly drives the CPI interface on the SBCORE circuit pack. The CPI paddle board is fully duplex, i.e. 1 paddle board per MCTU3 side, and uses a separate RS232 interface for each of the paddle boards. The interface between the CPI and MCTU3 is cross coupled allowing a paddle board to transmit a CPI message to both MCTU3 sides. The paddle board will use a resident 87C51 Microcomputer to translate the RS232 messages into CPI messages for transmission into the MCTU3. The elements identifiers of CPI Paddle board interfaces in CAD 1 are DU, DV, IN, and IO. When the CPI Paddle board is not used, 982ET shorting Berg connectors are populated in element identifiers DU and IN.

2.3 INTERNAL INTERFACES

In SD-5D536-01 internal interfaces consist of backplane wiring. All cross-coupled interfaces (signals between side 0 and 1) are connected internal to the backplane.

2.3.1 SMP Sub-Unit Interface Bus

The Sub-Unit Interface Bus (SUIB) is used as the SMP control interface to the sub-units (TSI, SP, CI, PI). The SUIB is not cross-coupled to both MCTU3 sides. It utilizes a 16-bit bidirectional data bus and a 6-bit address bus. Parity leads are used to provide error checking over address and data. The data bus has two bidirectional parity leads one each for the low byte and high byte of data. The parity is computed such that the sum of bits set to a logic one in each byte (including the parity bit) is even. One parity lead is used for the address bus. Odd parity is calculated over the address bus, i.e., the sum of bits set to a logic one (including the parity bit) is odd.

The SUIB has five control leads. Two of these, the read and write signals, are shared by all sub-units. These two signals distinguish between read and write operations to a sub-unit and are used by the selected sub-unit to gate the data to/from the data bus. The other three controls are board select, ready, and interrupt. Each individual sub-unit has separate board select, ready, and interrupt leads. The board select lead enables the desired sub-unit, the ready lead allows the sub-unit to extend the SMP bus cycle for sub-units with slower response time, and the Interrupt lead allows the sub-unit to interrupt the SMP. In addition, the CIs receive a lead called SMPACTN that is used to force the Select wire pair in the PICB on the non-active side to a nonconductive state.

2.3.2 SMP-DLI Message Interface

The SMP-DLI message interface consist of two cross-coupled 48 kilobits/sec X.25 message links and a Central Processor Intervention (CPI) link.

The message time slot is extracted from the NCT link by the DLI and parity is then generated over the six bits of data. The generated parity and message time slot data is sent to the Synchronous Data Link Controller (SDLC) in both sides of the SMP over separate data leads. At the same time, the Central Processor Intervention (CPI) bit is sent to the CPI gate arrays in both sides of the SMP. Two clocks are sent to both sides of the SMP from the clock circuit in the DLI. These clocks are used by the SMP to clock the received message time slot data and parity into the SDLCs. In the return direction, the SMP uses these clocks, provided by the DLI, to clock data and parity to the DLI. Each DLI contains a message interface to and from both sides of the duplex SMP.

2.3.3 SMP-DLI Control Interface

The SMP controls the DLI through a cross-coupled interface and consists of six signals. A module processor active lead originates from the SMP to indicate which side is sending commands to the DLI. A module processor read/write lead comes from the SMP to control when a read or write command is executed by the DLI. A 1.875MHz clock is sent by the SMP along with serial data that specifies the command to be executed. The entire write operation is specified in a serial 16-bit command in which the first eight bits contain the data to be written, followed by a spare bit and a parity bit for the eight bits of data. The next bit is an operation bit specifying a write operation, followed by the parity bit for the address and four address bits that specify the register to be written. During a read operation, only six bits are sent by the SMP to specify the command. The first bit is the operation bit specifying the read operation, followed by the address parity and the four address bits that determine the register to be read. Following the execution of the read command as initiated by the module processor go signal, eight bits of data plus one parity bit (parity over the data) are sent back to both sides of the SMP on separate signal leads with the results of the read operation. An interrupt lead indicating that error conditions exist in the ESRs of the DLI are also a part of the SMP-DLI control interface. The interrupt signal is asynchronous to the SMP and have no specified timing relationship.

2.3.4 TSI-DLI Interface

The TSI and DLI interface with one another through cross-coupled 4-bit nibble buses. The TSI transmits the 512 time slots to both DLIs in the MCTU3. In the opposite direction, the TSI provides a switch, set under SMP control, to select 512 time slots from one of the two DLIs. This provision allows the TSI to be configured to receive its time slots from the active DLI, and under normal (no fault) conditions, to switch between the two DLIs, on a per-time-slot basis, without introducing data errors. The interface consists of two 256 time slot busses to and from each DLI. Each bus transmits 16-bit words made up of four consecutive 4-bit nibbles. The parity bit is set such the sum of bits (including parity) set to a logic one is odd. Each DLI supplies the TSI with an 8.192-MHz clock, an 8KHz sync pulse, and a 6 ms sync pulse in addition to data. The TSI is required to perform an error free switch when selecting a DLI timing source. To accomplish this switch the maximum DLI clock skew between the duplicated DLIs can not exceed 20 nsec.

2.3.5 TSI-DI Interface

The interface between the TSI and the DI consists of a nibble bus in each direction carrying call traffic, control information from the TSI to the DI, clock, and sync. The TSI-DI interface is not cross-coupled to both MCTU3 sides. Two DIs are connected to the TSI each supplying 256 time slots in nibble format. The nibble busses carry a time slot on four consecutive nibbles, and operate at 8.192Mbits/sec; 256 time slots per frame are transmitted in each direction to each DI. These busses use a walking parity scheme for fault detection. In this scheme the parity is normally odd but in every ninth time slot, the parity is even.

The control information includes a 4-bit PIDB address that selects the source and destination for the 512 time slots associated with the DIs and a DI board select lead. This lead tells the DI to connect the TSI time slot with which it is associated to the specified PIDB, or to ignore the time slot and make no PIDB connection to it.

Two additional leads are used to diagnose the DI. One lead informs the DI to loop the TSI data received on that time slot through itself and back to the TSI on the same time slot of the next frame. The other lead directs the DI to replace the received TSI data with PIDB idle code.

The clock lead nominally is an 8.192MHz clock (122 ns period). The 8KHz sync is a normally "high" signal with an active "low" pulse of one 8.192MHz period in duration occurring every 125us (once per frame).

2.3.6 TSI-DSC Interface

The TSI-DSC interface is cross-coupled between side 0 and 1 of the MCTU3. The TSI transmits and receives 32 serial time slots to and from each DSC service group. Any of these 64 time slots can be selected as a source of PCM data for any time slot going to the DLIs or DIs. Similarly, the TSI can send the 16-bit word of any time slot received from the DLIs or DIs out on any of the 64 time slots to the local DSC. The data format and timing of the local DSC interface is of the PIDB type consisting of four balanced, differentially driven, RS-422 compatible, twisted-pair wires. Signals provided by this interface are a 4.096MHz clock out, an 8KHz sync pulse out, 32-time slot serial output data, and 32-time slot serial input data.

2.3.7 Unit Test Interface

This interface is used when the MCTU3 is in a unit or lab test environment. The test slot is used for unit test or software testing via the UN364- DUS/SMITS board. Use of SMITS permits a user to examine and modify the execution of a program. SMITS accommodates step-by-step execution of target programs, the setting of breakpoints, and the running of error detection programs. Additional test cables are required when using DUS or SMITS.

2.4 UNIT LAYOUT

The MCTU3 is a single shelf unit containing one backplane (ED-5D801-01). It functions as a duplexed entity, with both sides (0 and 1) on the same shelf.

Equipment locations for all component codes in the MCTU3 are shown below:

EQL	FDESIG	COMPCODE
04-000	TESTBRD	UN364
04-014	0SBPCD	TN1424
04-021	0SBCORE	KBN17
04-032	0CI-0	UN71C
04-040	0CI-1	UN71C
04-048	0PI2	UN395
04-056	0TSI-SP	TN1086B
04-066	0DI-0	TN1524
04-074	0DI-1	TN1524
04-084	0DLI	TN1077F
04-094	0DSC2	TN833C
04-106	1SBPCD	TN1424
04-113	1SBCORE	KBN17
04-124	1CI-0	UN71C
04-132	1CI-1	UN71C
04-140	1PI2	UN395
04-148	1TSI-SP	TN1086B
04-158	1DI-0	TN1524
04-166	1DI-1	TN1524
04-176	1DLI	TN1077F
04-186	1DSC2	TN833C

3. REFERENCE DATA

Supplementary information is contained in the following documents:

(a) Module Controller and Time Slot Interchanger Unit, Model 2 - SD-5D151-01

(b) Module Controller and Time Slot Interchanger Unit, Model 2 - CD-5D151-01

(c) Switching Module Control Cabinet, Model 2 - CD-5D160-01

(d) CPSM-UN364

(e) CPSM-TN1424

(f) CPSM-TN1425

(g) CPSM-KBN17

(h) CPSM-UN71C

(i) CPSM-UN71B

(j) CPSM-UN395

(k) CPSM-TN1086B

(l) CPSM-TN1042

(m) CPSM-982YN

(n) CPSM-TN1524

(o) CPSM-TN1377

(p) CPSM-TN077F

(q) CPSM-TN833C

3.1 WORKING LIMITS

Voltages:

(a) +5±0.5 volts

(b) -48 volts +4.5, -6.25 volts

Ambient Temperature:

(a) 0° to 70° Centigrade (at circuit pack).

(b) 0° to 50° Centigrade (office aisle ambient).

Growth:

With the basic unit equipage each side of the MCTU3 contains 32 PIDBs and 23 PICBs. The unit may be expanded by adding another CI to each side, for a total of 46 PICBs per side.

3.2 FUNCTIONAL DESIGNATIONS

Functional designations for all component codes in the MCTU3 are shown below:

FDESIG	MEANING	COMPCODE
TESTBRD	TEST BOARD	UN364
(0,1)SBPCD	SINGLE BOARD POWER CONTROL/DISPLAY	TN1424 or TN1425
(0,1)SBCORE	SINGLE BOARD CORE	KBN17
(0,1)CI-0	CONTROL INTERFACE 0	UN71C
(0,1)CI-1	CONTROL INTERFACE 1	UN71C
(0,1)PI2	PACKET INTERFACE - MODEL 2	UN395
(0,1)TSI-SP	TIME SLOT INTERFACE/SIGNAL PROCESSOR	TN1086B
(0,1)DI-0	DATA INTERFACE 0	TN1377 or TN1524
(0,1)DI-1	DATA INTERFACE 1	TN1377 or TN1524
(0,1)DLI	DUAL LINK INTERFACE	TN1077F
(0,1)DSC2	DIGITAL SERVICE CIRCUIT - MODEL 2	TN833C
(0,1)MTSSWA	MESSAGE TIME SLOT SWITCH A	955B
(0,1)MTSSWB	MESSAGE TIME SLOT SWITCH B	955B
(0,1)CPIPB	CPI PADDLE BOARD	982YN
PWRLUG	POWER/GROUND LUG	- - -

3.3 FUNCTIONS

The function of this unit is described in Section II of this Circuit Description.

3.4 CONNECTING CIRCUITS

When this circuit is listed on an application schematic, the connecting information thereon is to be followed.

3.4.1 Main connecting circuits

Main connecting circuits:

(a) Time Multiplexed Switch Unit - SD-5D043-01

(b) Time Multiplexed Switch Unit 2 - SD-5D061-01

(c) Six-Fan Unit - SD-5D081-01

(d) Fuse/Filter Unit - SD-5D053-01

(e) Multi Module RSM MMRSM Alarm and Status Unit - ED-5D586-10

3.4.2 Peripheral Units

Peripheral Units:

(a) Line Unit - SD-5D051-01

(b) Line Unit 2 - SD-5D032-01

(c) Line Unit 3 - SD-5D180-01

(d) Trunk Unit - SD-5D300-01

(e) Digital Carrier Line Unit - SD-5D203-01, SD-5D202-01

(f) Integrated Services Line Unit - SD-5D091-01

(g) Packet Switch Unit - SD-5D074-01

(h) Digital Line and Trunk Unit - SD-5D201-01

(i) Digital Line and Trunk Unit Export - SD-5X204-01

(j) Metallic Service Unit - SD-5D033-01

(k) Modular Metallic Service Unit - SD-5D015-01

(l) Digital Service Unit - SD-5D035-01

(m) Digital Service Unit 2 - SD-5D092-01

(n) Digital Service Unit Export - SD-5X201-01

(o) Remote Clock Unit - SD-5D075-01

(p) Facilities Interface Unit - SD-5D401-01

(q) Transmission Rate Converter Unit - SD-5D086-01

(r) Switching Transmission Facilities Unit - SD-5D167-01

(s) Directly Connected Test Unit - SD-2P077-01

(t) Echo Canceler #5 Signaling Unit - SD-5X213-01

3.5 MANUFACTURING TESTING REQUIREMENTS

Manufacturing Test Requirements For Module Controller And Time Slot Interchange Unit, Model 3 (J5D003FS-1)

3.6 ALARM INFORMATION

The function of this unit is described in Section II of this Circuit Description.

3.7 TAKING EQUIPMENT OUT OF SERVICE

Reference the following document, AT&T 235-105-xxxx Practices for Procedures.

4. REASONS FOR REISSUE

NA

5. ACRONYMS, ABBREVIATIONS OR INITIALISMS

ADR	Alternate data RAM
ALM	Alarm
AM	Administrative module
APPL1	SMP application 1 circuit pack
ASW	All seems well
AUTISS	Automatic time slot switching
AWS	Administrative Work Station
BCR	Bus Control Register
BTSR	Bootstrapper
CAD	Cabling and distribution
CDMA	Code Division Multiplexed Access
CI	Control interface
CLM	Communication link monitor
COGs	Cost of Goods
CORE	SMP core circuit pack
CPI	Central Processor Intervention
CPM	Communications Processor Module
CPU32	Central Processor Unit 32 bit
CS1	SMP core support 1 circuit pack
CS2	SMP core support 2 circuit pack
DI	Data interface
DLI	Dual link interface
DMA	Direct memory access
DRAM	Dynamic random access memory
DRC	Dynamic Ram Controller
DSC	Digital service circuit
DSP	Digital signal processor
DSU	Digital Service Unit
DUS	Demon utility system
EDC	Error Correction Detection
EIA	Electronics Industry Association
EPROM	Erasable, Programmable, Read-Only Memory
ESR	Error source register
FIFO	First in, first out
FIU	Facility interface unit
FFU	Fuse/filter unit
FPGA	Field Programmable Gate Array
I/O	Input/output
ISDN	Integrated Services Digital Network
LDSU	Local digital service unit
LDSUB	Local DSU Bus
LED	Light emitting diode
LI	Link interface
LLR	Last look RAM
LRR	Last report RAM

LP	Logical processor
MEM	SMP memory
MCTU2	Module Controller Time Slot Interchange Unit, Model 2
MCTU3	Module Controller Time Slot Interchange Unit, Model 3
MMRSM	Multi Module RSM
MMU	Memory Management Unit
MPF	Mate power fail
MSGS	Message switch
MTS	Message time slot
MUPEN	Mate update enable
NCT	Network control and timing
NDRC	NCT to D3 rate converter
NMI	Non Maskable Interrupt
OOS	Out of service
ORM	Optically Remote Switching Module
PB	Packet bus
PBMAC	Packet Bus Media Access Controller
PH	Protocol handler
PIC	Programmable Interrupt Controller
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
PLL	Phase lock loop
PP	Port processor
PI	Packet interface
PSU	Packet switch unit
PSU2	Packet Switch Unit, Model 2
PWRCTRL	Power control
PWRLUG	Power Lug
QLWR	Quad Long Word Register
QUICC	QUad Integrated Communications Controller
RAM	Random access memory
RCV	Receive
ROS	Request for out of service
RQIP	Request in progress
RS	Remote System
RSM	Remote switching module
SBCORE	Single Board CORE
SBPCD	Single Board Power-Control/Display
SDI	Serial data interface
SDLC	Synchronous Data Link Controller
SIM60	System Integration Module
SIMM	Single In-line Memory Module
SM2000	Switching Module 2000
SM	Switching module
SMC	Switching Module Control
SMITS	Switching Module Integrated Test System
SMP	Switching module processor

SMP1	Switch Module Processor, Model 1
SMP20	Switch Module Processor, Model 2
SMP40	Switch Module Processor, Model 4
SMPACTN	Switch Module Processor Active signal
SP	Signal processor
SUIB	Sub-unit interface bus
TMS	Time multiplexed switch
TPC	Timer-PIC-Controller
TRCU	Transmission Rate Converter Unit
TRM	Two-mile optically Remote switching Module
TSIU	Time Slot Interchanger Unit
UBC	Update Bus Controller
UCI	Unified control interface
VCDX	Very Compact Digital Exchange
VCXO	Voltage Controlled crystal Oscillator
XMIT	Transmit

AT&T

DEPT NQ9240400-DAS-CCL