CIRCUIT DESCRIPTION

CD-5X201-01
ISSUE 1
APPENDIX 5B
DWG ISSUE 6B
DISTN CODE BT13

5ESS® Switching Equipment
Global Digital Service Unit – Export
Circuit

A. Changed and added Functions

A.01 MC-5D069A1 (TN1032) was added to provide mu-law 6-port
      conference circuit capability to SD-5X201-01. Please note
that this firmware provides the same capabilities as MC-5X262A1
which is the A-law 6-port conference circuit firmware for TN1032.

D. Description of Changes

D.01   Added MC-5D069A1 (TN1032) to Apparatus Figure 15.

AT&T BELL LABORATORIES

DEPT 122Z231320-JRK-EBH

CIRCUIT DESCRIPTION

CD-5X201-01
ISSUE 1
APPENDIX 4B
DWG ISSUE 5B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT
GLOBAL DIGITAL SERVICE UNIT – EXPORT
CIRCUIT

CHANGES

B. Changes in Apparatus

SUPERSEDED | SUPERSEDED BY

MC5X400A1B App. Fig. 12   MC5X400A1C App. Fig. 14
TN898 App. Fig. 9   TN898B App. Fig. 13

D. Description of Changes

D.1 In FS 2 and 5 reference to options 5, 6, 7, 8, 9, 10, and 12 removed.

D.2 In FS 2 and 5 reference to notes 311 and 312 added.

D.3 In notes 302, 304, 306, and 307 references to TN898B and MC5X400A1C added.

AT&T BELL LABORATORIES

DEPT 11NW532240-JDF-EBH

CIRCUIT DESCRIPTION

CD-5X201-01
ISSUE 1
APPENDIX 3A
DWG ISSUE 4A
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT
GLOBAL DIGITAL SERVICE UNIT - EXPORT
CIRCUIT

CHANGES

B. CHANGE IN APPARATUS

SUPERSEDED   SUPERSEDED BY

MC5X400A1(TN899) App Fig. 10   MC5X400A1B App. Fig. 12

D. DESCRIPTION OF CHANGES

D.1 In FS 2 and 5 MC5X400A1B circuit pack added as option 12.

D.2 In notes 302, 304, 306, and 307 reference to MC5X400A1B added.

D.3 Note 310 added.

AT&T BELL LABORATORIES

DEPT 11NW532240-JDF-EBH

CIRCUIT DESCRIPTION

CD-5X201-01
ISSUE 1
APPENDIX 2B
DWG ISSUE 3B
DISTN CODE BT13

5ESS® SWITCHING EQUIPMENT

GLOBAL DIGITAL SERVICE UNIT – EXPORT
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added

TN1032 Circuit Pack – FS 2, 5, APP FIG. 11.

D. Description of Changes

D.1 In FS 2 and 5, TN1032 circuit pack, option 11, 6-port conference circuit was added.

D.2 Apparatus FIG. 11 was added.

AT&T BELL LABORATORIES

AT&T-T DEPT 11NW532240-JLG-EBH

5ESS* SWITCHING EQUIPMENT

EXPORT GLOBAL DIGITAL SERVICE UNIT
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The export digital service unit (DSU-E) is an export 5ESS peripheral that provides the export 5ESS with the functions of tone decoding, tone generation, conferencing, and certain AC tests. Each DSU consists of two independent service groups to provide partial service availability in the presence of a single hardware failure. Each service group provides up to 32 time slots of service features and consists of one common circuit pack and up to eight service circuit boards. Both service groups share a single 2-ft, 2-in. wide equipment shelf.

1.02 The current 5ESS system architecture designates two types of DSUs: a local DSU and a global DSU. They differ only in the equippage of the optional service circuit boards (two shelves versus one shelf, respectively), and in their position in the 5ESS network architecture. The local DSU is module-dedicated, i.e., each local DSU serves a single switching module. It provides the high-usage functions of tone generation and tone decoding for its associated switch module (SM). The local DSU connects to the SM via the local digital service unit bus (LDSUB), and does not use any of the 512 internal time slots in the TSIU. The global DSU can be shared by all modules in the 5ESS office and is accessed via the switching network. It provides low-usage functions, such as conferencing and transmission testing. Global DSUs connect to the SM via the peripheral interface data bits (PIDB) and are engineered over the entire office, as needed. Both the local and global DSUs communicate control information to the SM via the peripheral interface control bus (PICB).

SECTION II - DETAILED DESCRIPTION

1. INTRODUCTION

1.01 The export digital service unit is an Export 5ESS peripheral that provides the Export 5ESS with tone decoding, tone generation, conferencing, AC testing, and other appropriate functions, as required. The Export 5ESS system architecture requires two types of DSUs: a local DSU (LDSU-E) and a global DSU (GDSU-E). The local DSU unit consists of a 2-shelf unit with wiring for only the local DSU functions. The global DSU unit for export is exactly the same as the unit and backplane for the domestic local and global DSU except for the SD and ED numbers. This document covers both local and global DSU units and will serve as the CD for both units. Information on the GDSU-E TTF functions will be included in the form of an attached DS that covers those boards in detail.

1.02 This design specification is based on the circuit description document for domestic, except that it has been modified to reflect the export unit differences.[1] This circuit description first addresses the high-level functional and interface requirements of the DSU. Subsequent sections describe the implementation details of the DSU beginning with its internal architecture, following with the DSU common circuits (TN128/TN848), interface requirements for all service circuit plug-ins, and finally a description of the existing circuits; the TN850 tone decoder, TN852 tone generator, and TN841/TN851 conference circuit.

2. DSU REQUIREMENTS

OPERATIONAL REQUIREMENTS

2.01 The DSU is required to provide the following functions in Export 5ESS:

(a) Tone Decoding

(b) Tone Generation

(c) Conferencing

(d) Transmission Testing

2.02 In addition to the above, the architecture of the DSU should be flexible enough to allow for the addition of new service functions in later Export 5ESS generics as these services are defined and are deemed appropriate for DSU inclusion.

A. Tone Decoding

2.03 The LDSU-E will provide the tone recognition functions required by Export 5ESS call processing. The following tone types must be recognized by the Universal Tone Decoder (UTD-E):

(a) TOUCH-TONE* Signals (16 tone pairs)

(b) Multifrequency Signals (15 tone pairs)

(c) Multifrequency Compelled Signals (30 tone pairs)

2.04 When performing the tone decoding function for the above classes of tones, the UTD-E must meet the frequency, amplitude, and timing requirements established for tone decoders of each respective signaling type, as specified in the following standards:

(a) Switching System Specifications (LSSS), Section 6.4.

(b) CCITT Volume III Fascicle III.3 Rec. G.711

(c) CCITT Volume VI Fascicle VI.4 Rec. Q.440 - Q.490

(d) CEPT Rec. T/CS 46-02

(e) Dutch PTT spec. TF 510-02 Issue 2

B. Tone Generation

2.05 The GDSU-E must be capable of generating the following tones required by Export 5ESS:

"Call Progress Tones" as specified on a per-application basis Multifrequency Signals (15 tone pairs), Multifrequency Compelled Signals (30 tone pairs), TOUCH-TONE Signals (16 tone pairs), and CCIS Continuity Check Tones (1780 and 2010 Hz).

2.06 All tones generated by the Universal Tone Generator (UTG-E) must meet the amplitude and frequency requirements specified in the above domestic and export requirements. The DSU must supply enough different tones at any given time to satisfy the load requirements placed on it by a fully equipped switching module (SM). The fanout of a given tone to multiple destinations will be performed by the Time Slot Interchange (TSI) circuit in

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* A registered service mark of AT&T.

the SM. The TSI also will supply cadence or other special timing functions for those tones that require such features, i.e., busy tone, audible ring, etc.

C. Conferencing

2.07 The GDSU-E will provide conference calling features for Export 5ESS. Voice bridging capability for only 3-party conferencing will be provided. Three-party conference calling is used as a customer service, for busy-line verification, and for certain switch maintenance functions.

2.08 For the special case of busy-line verification, the DSU will also perform the required interchange of the A, B, C, and D signaling bits for the three parties involved in the call.

D. Transmission Test Function

2.09 The GDSU-E will provide a Transmission Test Function (TTF) that will perform all voice band transmission tests required in an Export 5ESS office. These include facility testing and CODEC testing, in addition to noise, loss, and frequency response measurements. Test lines provided for the 5EE1 generic include:

   (a) 105 Test Line,
   (b) Remote Office Test Line (ROTL), and
   (c) DUAL TONE MULTIFREQUENCY Test Line.

Two separate Development Specifications have been issued for the TTF.[2] [3]

3. MAINTENANCE REQUIREMENTS

3.01 The following is a list of general maintenance objectives that govern the design of the DSU, as well as other maintainable Export 5ESS units:

   (a) The maintenance philosophy of the DSU shall be consistent with

the maintenance philosophy of Export 5ESS.

   (b) The DSU shall contain sufficient redundancy so that no single DSU failure will result in complete loss of DSU service.

   (c) The DSU shall contain circuits with sufficient error-detection capability. It accomplishes this by using self checking and software initiated per call tests. Undetected failures in the DSU will not result in a degradation of service that reduces the reliability performance for call failures in Export 5ESS.

   (d) Conservative design, which prevents intermittent or marginal operation of the unit from occurring, shall be followed in the DSU.

   (e) The design of the DSU shall be modularly partitioned such that the ability of the diagnostic programs to resolve faults will meet the Export 5ESS maintenance requirements.

   (f) All DSU circuit packs that contain EPROM devices will be compatible with the version C of the Prompt Remotely Operated Memory Updating System (PROMUS-C). The PROMUS-C system is a FASTECH™-compatible piece of equipment that allows the erasure and programming of EPROM contents while the devices remain intact on the circuit packs.

4. DSU DESIGN IMPLEMENTATION

4.01 The Export 5ESS architecture identifies two types of DSUs: a "local DSU" (LDSU-E) and a "global DSU" (GDSU-E). The local and global DSUs differ primarily in the types of service functions performed by each and

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their positions in the Export 5ESS network architecture.

LOCAL DSU

4.02 The local DSU provides the heavily used functions of tone generation and tone decoding for Export 5ESS. Each switching module (SM) will be equipped with a single local DSU, and that local DSU will be dedicated to provide tone generation and tone decoding only for lines and trunks terminating on that SM. The decision to segregate tone generation and tone decoding from the rest of the DSU functions was made early in the development of the 5ESS switch. Distributing these functions to each module, rather than providing them in a centralized pool shared by all modules, greatly reduces the amount of intermodule message traffic, because these services are heavily used in call processing.

4.03 The local DSU is connected to the Local Digital Service Unit Bus (LDSUB) of the TSI and receives time slot data from the alternate data RAM in the TSI. Access to the local DSU is gained by creating TSI paths from peripheral side time slots into the alternate data RAM. The 64 time slots used by the local DSU are not part of the TSI's 512 peripheral time slots, and thus the appearance of a local DSU on each SM does not reduce the switching capacity of the TSI.

GLOBAL DSU

4.04 The global DSU provides conferencing, transmission testing, and other low-usage services that may be developed in the future. Because global DSUs provide low-usage service functions, they are not module dedicated, but are equipped as needed in the Export 5ESS office. The global DSU is attached to the TSI via the Peripheral Interface Data Bus (PIDB) in a manner identical to all other TSI peripheral units (line unit, trunk

unit, etc.). Access to the global DSU is obtained via the TSI/TMS switching network. The 64 time slots used by the global DSU are part of the TSI's 512 peripheral time slots, and thus the termination capability of the network is reduced by that amount with the addition of each global DSU.

5. DSU ARCHITECTURE

5.01 The architecture of the DSU, Figure 1, consists of two independent service groups to provide redundancy and service availability. Each Global DSU service group accesses 32 time slots from the TSI and consists of the GDSU Common Board (GDSUCOM-E), TN 128, and one to eight Global Digital Service Circuit (GDSC) plug-ins. Each Local DSU service group accesses 32 time slots from the TSI and consists of the LDSU Common Board (LDSUCOM-E), TN 848, and two to 16 Local Digital Service Circuit (DSC) plug-ins.

5.02 Proper engineering of the DSCs in each DSU service group is important to ensure adequate reliability for each service. In the local DSU, the service groups should be engineered with one tone generator circuit and identical complements of tone decoder circuits. This ensures that under any single failure condition in the DSU (loss of one service group at most), a maximum of only half of each service is lost. This will allow call processing to continue in the IM, resulting in only a degraded form of service (a minimum of 50 percent peak capacity).

5.03 Service circuit engineering on the global DSUs is much less critical, but should follow these three guidelines to obtain optimum service availability:

(a) In an office with only one GDSU-E, services should be split between the two service groups for reasons explained in the previous paragraph.

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(b) For multiple global DSUs, service circuits of each type should be distributed as evenly as possible among global DSUs to provide service availability in the presence of duplex failures (i.e., both DSU service groups fail or a duplex SM failure).

(c) Software has the ability to support multiple GDSUs on the same SM. However, a maximum limit of seven GDSUs per SM exists, and a limit of one TTF per SM is set.[4]

6. EXTERNAL INTERFACES

A. Control Interface

6.01 The DSU communicates control information to and from the switching module processor unit (SMPU) via the peripheral interface control bus (PICB). Each service group provides a duplex PICB interface to the duplicated SMPU. A duplex-to-simplex interface conversion is performed at the interface by decoding a select lead on each bus, such that the DSU listens only to the active side of the SMPU. Reply messages are sent to both SMPU halves. However, the interrupt signal to the SMPU is sent only to the active SMPU half.

B. Data Interface

6.02 The DSU communicates data information to and from the time slot interchange unit (TSIU). The data interface to the local DSU is the local DSU bus (LDSUB), and to the global DSU it is the peripheral interface data bus (PIDB). In either case, the busses are identical electrically and consist of four differential balanced TTL signals: a 4-MHz clock, an 8-Hz frame synchronization pulse, and a 32-time-slot serial data stream in each direction. As with the PICB, this bus is presented in duplicate to each DSU service group (one from each half of the TSI). A peripheral control channel

(PCC) writable bit selects the active bus to listen to, but the 32-time-slot data bus to the TSI is returned to both TSI halves.

C. Power Interface

6.03 Each DSU service group is powered from the -48V battery plant; DSU service group 0 and DSU service group 1 each receives -48V from separate battery feeds. Each service group contains a -48V to +5V FASTECH power converter (coded 495FB), which supplies +5V power to the entire service group with a maximum rating of 250 usable watts (14 or 28 watts per circuit pack for local or global DSU, respectively). Current programming resistors located on each DSU circuit pack will determine the output current limitations of the power converter. The value of each current programming resistor can be calculated, based on the circuit pack current requirements as shown below:

$$R(Kohms) = 10/(1.19 \times IMAX)$$

The power converter will shut down should the total service group current drain fall outside the window specified by the sum total of current programming resistors.

6.04 DSC circuit packs must be inserted or removed from a powered-up DSU without causing converter shutdown, or service-altering glitches on the +5V power or ground busses. As indicated above, the power converter will shut down should the total service group current drain exceed the total specified by the sum total of the current programming resistors. Exceeding the specified current may occur momentarily when a circuit pack is inserted into a powered-up DSU if the current programming resistor pins on the circuit pack do not engage with the backplane pins before the +5V power and ground pins. Also, on insertion, the circuit pack +5V bus capacitance causes a surge current which, in turn, causes

Page 6

a transient on the backplane +5V bus. To restrict the current to a level that is compatible with the time delay requirements for converter shut down, and to reduce the transient on the backplane +5V bus, the design described below is implemented.

6.05 First, each circuit pack position, excluding the power converter and the TN128/TN848 (DSUCOM), will be equipped with seven long (0.75 inch) backplane pins. The converter and the TN128/TN848 will not be pulled in the powered-up position. When a DSC-type circuit pack is inserted into the DSU, these seven pins will engage the circuit pack connector before the normal length pins. Four of the pins are connected to ground. Two pins are associated with the circuit pack programming resistor. The last pin is +5V. The circuit pack connector pin associated with this +5V long backplane pin will have a high inductance, low resistance choke connected between it and the circuit pack +5V bus. When a circuit pack is inserted into a powered up DSU, the programming resistor, ground, and +5V (single pin with the choke in series) make contact first. The programming resistor adjusts the converter for the expected circuit pack current drain, and the choke restricts the surge current to reduce the transient on the backplane +5V bus. The overall current is restricted to a level that does not exceed the converter shutdown requirements. When the circuit pack is fully inserted, the remaining power and ground connections are made, and the pack functions normally; this shorts out the choke. Removing a circuit pack from the powered-up DSU does not cause a problem with regard to converter shutdown; neither is it detrimental to the circuit pack or to the backplane pins.

An additional power converter requirement is that the equivalent series resistance of the converter output filter be low enough to accommodate power surges under worst-case conditions.

7. DSU CIRCUIT PACKS

7.01 In subsequent sections of this document, reference will be made to five commonly used DSU gate array devices.[5] These LSI devices were designed to save board area and reduce power consumption, both of which were necessary to provide a flexible DSU architecture having one service circuit per board. The five gate arrays are listed below:

(a) Delayed Synchronization Generator (41KT)

(b) Interrupt Register (129DK)

(c) Parity Generator (129DF)

(d) Parity Checker (129DL)

(e) Time Slot Select Register (267S)

DSU COMMON - TN128/TN848

A. Introduction

7.02 The DSU common circuit pack (DSUCOM) serves primarily as the interface between the duplex SMPU/TSIU and the simplex digital service circuits (DSCs). The DSUCOM, coded TN128/TN848, for the (GDSUCOM-E)/(LDSUCOM-E) respectively, performs the required duplex <-> simplex conversion on the data and control busses from SMPU/TSIU, typically listening on the active bus and replying on both. The DSUCOM distributes the 4 MHz clock, 8Hz frame sync, 32 time slots of data, and control information on all DSCs. The DSUCOM multiplexes data and control return information from the DSCs for reply to the SMPU/TSIU. In addition, the DSUCOM contains interrupt registers with each DSC's parity, error, and summary scan interrupt status. Partial equippage of DSCs is allowable because the DSUCOM uses a pesting strategy and

writable control memories to ignore unused DSC positions.

B. Control Interface

7.03 The DSUCOM control interface to the SMPU/TSIU is the Peripheral Interface Control Bus (PICB). The DSUCOM receives a simplex PICB from each SMPU half as shown in Figure 2. Each PICB consists of a 2MHz clock, (C0,C1), data in (ID0,ID1), data out (OD0,OD1), select (S0,S1), and not interrupt (NINT0,NINT1) as shown. Clock, data in, and data out are balanced, differentially driven, twisted pair signals. Clock and output data in are terminated with a 220 ohm shunt resistance. Controller select and not interrupt also use differentially balanced twisted pairs. The select leads enable the DSUCOM to select one of the PICBs as the active bus. If both select leads contain the same logical value, PICB0 is selected as the active bus; if their values differ, then PICB 1 is selected.

7.04 As shown in Figure 3, the clock (CLK) and data (DI) from the selected bus are sent to a peripheral sequencer gate array (Code 241AA), through a quad differentially balanced line receiver (Code 502KA). The input clock (2.048MHz) is also monitored by a retriggerable monostable multivibrator with a typical pulse width of 2.6 microseconds to provide a reset to the peripheral sequencer between control messages. The peripheral sequencer checks the serial input message for correct format and outputs data shift clock (DSCKOUT) and serial message data signals (DWOUT) that are buffered for use on the DSUCOM and then separately buffered to the backplane for use by the DSCs. In conjunction with three address decoder gate arrays (Code 41JU), the 241AA produces a 24-bit parallel peripheral address from the 9-bit serial address contained in the input message. (Refer to Figure 4.) This is accomplished by doing a 3-to-8 decoding function on the

input message address bits 3-5, 6-8 and 9-11 to produce three groups of eight address bits each as shown. Similar to the data shift clock and serial message data signals, most of the 24 address bits are then buffered twice - once to supply address information to the DSCs, and once to address the scan and distribute gate arrays on the DSUCOM. The 512 address spectrum of the PICB is divided among the eight DSC positions and the DSUCOM as shown in Figure 4. Each DSC is allotted 16 read and 16 write addresses, with the absolute address dependent on the DSC slot position number. The DSUCOM is allotted the remainder of the address space (128 write and 128 read addresses).

C. Data

7.05 The DSUCOM data interface to the SMPU/TSIU is via the Peripheral Interface Data Bus (PIDB) for a Global DSU, and via the Local DSU Bus (LDSUB) for a Local DSU. The busses are electrically identical and, as shown in Figure 5, each consists of a 4MHz input clock, an 8Hz frame synchronization pulse, and a 32 time slot (16 bits/time slot) serial data bus as inputs, and a 32 time slot serial data bus output. For this discussion, only the PIDB will be referred to.

7.06 All inputs and outputs on the PIDB are balanced, differentially driven, twisted pair signals. Incoming signals are terminated by 110-ohm resistors from each side to ground. The DSUCOM selects the active PIDB by a control channel writable bit. For the following discussion, refer to Figure 6.

7.07 The 4MHz input clock (4MC0,1) and the 8Hz synchronization pulse (8KS0,1) are buffered and fanned out separately to each DSC position and internally to the remainder of the DSUCOM. The 8Hz sync is reclocked and thus delayed by one full clock cycle (244 ns). A 16-bit destination

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register controls inhibit circuitry that permits the 4MHz clock and/or 8Hz syncs to be selectively disabled to any DSC for diagnostic purposes. TSI select is synchronized with clock via a two flip-flop circuit to ensure continuity on a clock switch.

7.08 The DSUCOM checks parity on each time slot of the incoming data bus. The sense of the incoming parity (even or odd) on each time slot is returned to the TSI on the same time slot during the following frame. This parity loop-around feature is useful in maintaining both directions of the data bus on the PIDB, since the TSI periodically walks even parity through the time slots on each PIDB and checks for even parity on the same time slot of the returning data bus. This walking parity is used with Global DSUs only.

7.09 The incoming data bus is fanned out separately to each DSC after being reclocked and regenerating parity on each time slot. This results in a 3-clock cycle (732 ns) delay from input to output. A 32-bit register, located in the parity generator gate array, is writable via the PCC, and is used to select even or odd parity to be regenerated on each time slot. Each bit in the register controls the parity selection for its respective time slot. Parity is regenerated so that incoming parity errors on the PIDB do not propagate to the DSCs. The ability to generate even or odd parity with per time slot control is useful as a maintenance feature.

7.10 The time slot select register (TSSR) gate array is a per time slot controller used in conjunction with a 38A memory to produce eight control outputs for every 3.906 usec time slot. The 38A is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC with the TSSR operating as a memory

controller. The TSSR autonomously reads the 38A memory once per time slot to fetch the eight control bits for the next time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906 usec time slot and are held valid for the remainder of the time slot to provide control functions on a per-time-slot basis.

7.11 The GDSUCOM-E has the capability to receive a 32-time-slot serial data bus from each of the eight DSCs. During each time slot, the GDSUCOM-E selects one of the eight DSCs as the source for data transmitted to the TSI. Using an 8-to-1 multiplexer circuit, the GDSUCOM-E routes the 16 data bits from the selected DSC to a parity check circuit through a 2-to-1 multiplexer. The LDSUCOM-E has the capability to receive a 32-time slot serial data bus from each of the 16 DSCs. During each time slot, the LDSUCOM-E selects one of the 16 DSCs as the source for data transmitted to the TSI, and using a 16-to-1 multiplexer circuit, routes the 16 data bits from the selected DSC to a parity check circuit through a 2-to-1 multiplexer. A pullup resistor to +5V is attached to all inputs to the 8, 16 to 1 multiplexer so that the inputs from unequipped DSC positions will be a constant logic one (bad parity). DSCs that do not transmit data to the DSUCOM must ground their data out lead so the DSUCOM input is a constant logic zero (also bad parity).

7.12 For diagnostic purposes, the DSUCOM has an internal data loopback that allows the 32 time slot data bus normally transmitted to the DSCs to be selected as return data. This is done in the 2-to-1 multiplexer that follows the 8, 16-to-1 DSC multiplexer. The control leads to both multiplexers are supplied by the TSSR, so that during any time slot, any of the DSCs or the internal loopback may be selected for data transmitted to the TSI. The internal loopback, due to circuit timing, inserts a 3-time slot

offset in the looped back data stream; i.e., if loopback is selected in the DSUCOM for time slot N, the data that is looped back to the TSI is that data sent by the TSI to the DSUCOM in time slot N-3. The circuitry required to align precisely the loopback time slot data is an additional 304-bit shift register, which was judged too costly to implement. Because the loopback feature is used only in the diagnostic, the slip translations will be compensated for in software.

7.13 The 32-time slot serial output of the multiplexer circuits is then checked for parity errors on each time slot as well as having parity regenerated for all time slots so that parity errors do not propagate to the TSIs. Should a parity error be detected on any time slot, a bit corresponding to the time slot number is set in a 32-bit error source register, and an interrupt is sent back to the active SMPU/TSIU. Also, at this point, the input parity sense (even or odd) for each time slot from the TSI is inserted into the outgoing time slots for transmission to the TSI. Two TSSR control bits, an error mask bit, and interrupt mask bit will inhibit errors and interrupts, respectively, on a per time slot basis, so that parity errors on unused or out-of-service time slots may be ignored.

7.14 The 32-time slot serial output from the Parity Check Gate Array is reclocked, buffered and then transmitted on both PIDBs, with quad balanced differential TTL bus drivers(Code 502JN).

D. Interrupts

7.15 The interrupt structure on the DSUCOM is shown in Figure 7. Three separate interrupt registers are contained on the TN128/TN848: the DSC fault register, the DSC parity error register, and the DSC summary scan register. A logic zero level on interrupt inputs to each of the interrupt registers sets a corresponding latch to hold the interrupt. The interrupt latches are readable and clearable on each register via the PCC. Should any of the latches contain an interrupt (be set), an interrupt output lead from the interrupt register will go low. The contribution of each latch to the output interrupt may be inhibited by setting the corresponding bit in an interrupt mask register. The following registers are 8 or 16 bits for TN128 and TN848, respectively.

7.16 The DSC fault register contains an input from each DSC that indicates if that DSC has detected an internal failure. A low level on an input lead will set the corresponding bit in the fault register.

7.17 The DSC parity error register contains an input from each DSC that indicates if that DSC has detected a parity error. An active low level on an input lead indicates that a parity error has been detected and will set the corresponding bit in the parity error register.

7.18 The summary scan register contains a lead from each DSC that goes low when the DSC initiates some type of service request (i.e., a tone decoder has a digit in its buffer ready for unloading). Pullup resistors to +5V are provided on all interrupt register inputs supplied by the DSCs, so that should a DSC position be unequipped, the interrupt input will be in the noninterrupting state.

7.19 For the TN128 the remaining eight inputs to the summary scan register contain the interrupt output summary leads of the DSC fault register and the DSC parity error register, GDSUCOM-E internal failure indicators, and one spare. The output from the summary scan register is sent to the active SMPU/TSIU via an opto-isolator. For the TN848, the 16-bit summary scan register contains a lead from each DSC.

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The output from this register, along with the outputs of the parity error and fault registers, goes to the interrupt register along with the LDSUCOM-E internal failure indicators.

UNIVERSAL TONE DECODER - TN850

7.20 Universal Tone Decoder (UTD) circuit packs are located in the local DSU where they perform the Export 5ESS tone decoding functions required for call processing. Each TN850 contains two independent tone decoders that can be configured to decode either TOUCH-TONE, Multifrequency (MF) or Multifrequency Compelled (MFC) tones.

7.21 The following sections describe the TN850 architecture and operation.

E. LDSUCOM-E - TN850 Interface

7.22 The TN850 transmits and receives all signals to and from the LDSUCOM-E, which functions as the interface between the SMPU/TSIU and the service circuits. The signals between the LDSUCOM-E and the TN850 are shown in Figure 8 and include clock, sync, data, control channel signals, and interrupt signals. The incoming data signal transmits the tone samples to the TN850; the control channel lines permit reading and writing of the UTD's source and destination registers, and the interrupt leads transmit fault indicators and service requests to the LDSUCOM-E.

7.23 Three data signals are sent from the LDSUCOM-E to the UTD-E: a 4.096 Mb/s serial data bus, a 4.096-MHz clock, and an 8KHz sync line. The data line presents the UTD-E with 32 time slots of data, each time slot being 16 bits long. The first eight bits of each time slot contain the u255 or A-law PCM sample; the last eight contain the A through D signaling bits, E, F, and G bits, and an odd parity

bit. The 4.096MHz clock line is buffered and directed to the clock inputs of all the flip-flops and is also buffered and directed to the two delayed sync generator gate arrays. These gate arrays generate delayed 8KHz Sync pulses that initialize circuit counters in the time slot select register (TSSR) and the parity check gate array.

7.24 The control channel lines allow software to read and write the numerous source and destination registers of the UTD-E. Control words are transmitted and received on separate bus lines at a 2.048 Mb/s rate. These reads and writes occur asynchronously with respect to the 4.096 Mb/s data bus, 8KHz Sync, and 4.096 MHz clock. The LDSUCOM-E generates addresses by simultaneously activating one of two possible B address signals and one of eight possible A address signals. Additional signals involved in each control channel operation include a 2.048-MHz data shift clock, a read select lead, and a write select lead. The control channel expects an acknowledgment pulse on one of two all seems well (ASW) leads for every control channel operation.

7.25 Three interrupt lines transmit UTD-E interrupts back to the LDSUCOM-E. The first, the parity error interrupt signal, generates an interrupt pulse whenever an incoming time slot parity error has been detected. The second, the fault interrupt signal, generates a latched interrupt level whenever an error is detected by the UTD's fault detection circuitry. The third, the summary scan interrupt signal, generates a latched service request interrupt whenever a decoder requires attention. The summary scan interrupt and the fault interrupt are latched on the UTD-E, and remain present until they are cleared by control channel write operations.

F. UTD-E Hardware and Operation

7.26 The UTD hardware is divided into two groups: a functional group, and a maintenance group. The functional group is the circuitry that performs the actual tone decoding on the UTD-E. The maintenance group is additional circuitry that performs monitoring and checking and permits software access to exercise the UTD-E hardware.

G. Maintenance

7.27 Each DSC, including the UTD-E, has a maintenance register and an identification-loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out-of-service lamp, and another is looped back to the identification-loopback register for control channel verification. The identification loop-back register, when read, returns the looped bit and a 7-bit UTD-E identification code. Each DSC type has a unique code.

H. Parity Check Gate Array

7.28 The parity check gate array monitors the incoming 4.096 MHz data bus. It checks for odd parity over the 16 bits in each time slot. If a time slot parity error (even parity) occurs, the corresponding bit of an internal 32-bit latch is set. Also, a parity check error pulse is generated to the LDSUCOM-E on the Parity Error Interrupt Line. Two Time Slot Select Register bits allow per time slot mask control over parity interrupts and parity error bit setting in the 32-bit latch. The 32-bit register can be read and cleared by the control channel.

I. Fault Interrupt Gate Array

7.29 The fault interrupt gate array monitors for four(4) internal board error lines. Each line can cause a fault interrupt to the LDSUCOM-E. The interrupt signal generated is a latched level. Each interrupt input, when active, sets an internal latch. The latch outputs are OR-ed together so that any of the four inputs can generate an interrupt out of the gate array. The latch outputs into the OR circuits can be masked individually to ignore undesired inputs. The latches can be read, cleared, and the per-line mask enabled by control channel writes. Two retriggerable monostable multivibrators monitor the incoming 4.096-MHz clock and the 8K Sync lines. If either signal is missing or intermittent, the monostables send active low-error signals to the fault interrupt register inputs. Other fault lines monitor a TSSR parity error output, and the Parity Checker 8-Hz Sync loss output.

J. Functional Description

7.30 Figure 9 shows a functional diagram of the UTD-E. The incoming data stream is buffered through a flip-flop and proceeds into the parity check gate array and to the two decoder circuits.

7.31 The time slot select register (TSSR) gate array and a 38A random access memory work together as a per-time slot controller. The TSSR has eight output control bits that are available to enable and disable per-time slot UTD-E functions. The 38A stores eight bits of control data for each of the 32 time slots. These 32 8-bit words are sequentially displayed at the control outputs, and the pattern is repeated every 125 usec. The TSSR allows the 38A contents to be

written and read asynchronously through the control channel without affecting the synchronous output of the stored data.

7.32 The UTD-E uses four of the TSSR's eight output control bits. Two are directed to the parity check gate array, where they control per-time slot masking of the interrupt output and per-time slot masking of parity error latching. The other two bits each enable a tone decoder circuit. When enabled, the decoder will use the next 8 PCM bits as inputs. During normal decoding operation, a decoder reads only one time slot's PCM bits per frame. The TSSR's flexibility permits a decoder to receive any of the 32 incoming time slots. Figure 10 displays the architecture of a decoder section. The block has two major components: The digital signal processor (DSP) and an 8748 microcomputer. The DSP is a programmable digital signal processor device packaged in a 40-pin DIP. It is a specialized microcomputer optimized to perform signal processing oriented functions. In this application it is programmed to perform digital filtering on the incoming PCM bits. The 8748 is an 8-bit, single-chip microcomputer that performs digit timing and verification. The two work together to complete the tone-decoding function. Both are initialized simultaneously through the control channel to choose the mode configuration (TOUCH-TONE reception, multifrequency, etc.). Each mode selects a different operating program in the DSP and 8748. The DSP firmware is stored in an external EPROM memory circuit. The 8748 firmware is stored in an internal EPROM.

7.33 Each DSP, when receiving sync from the TSSR, reads 8 PCM bits every frame and performs digital filtering on the incoming PCM samples. The algorithms, stored in EPROM, contain the filter coefficients, threshold detectors, and encoding routines required for the DSP to

perform the different filtering functions. During operation, the DSP provides an 8-bit output response when requested by the 8748. This response represents the results of the digital filtering, and the 8-bit code indicates which frequencies are present at the input. The DSP's serial output is converted to a parallel word and made available to the 8748 to read. The 8748 performs tone validation and digit timing analysis using the DSP's output response. When a valid tone or tone combination is recognized, a 4-bit encoding of the tone combination is generated and stored in a first-in/first-out (FIFO) firmware controlled buffer inside the 8748. (Refer to Figure 11.) The first stored digit is placed at the 8748 output ports, readable via the control channel. Subsequent decoded digits are stored in sequential FIFO buffer locations. The FIFO is programmed to store a maximum of 16 digits per call. Peripheral software is informed of the digit storage by a Summary Scan Interrupt. This interrupt is initiated by the digit present interrupt (DPI) of the 8748. This signal remains active as long as digits remain in the buffer. Two control channel operations alter the buffer status: first, the buffer pointer can be incremented to shift the buffer's contents so that the previously decoded digit is lost and the next stored digit is shifted to the 8748 output ports; second, another control channel write will reset both the DSP and 8748 decoder processors, initializing them to the selected mode and clearing the FIFO buffer completely. Interrupt responses from the decoder circuit are sent to the summary scan interrupt register, which generates a summary scan interrupt response to the LDSUCOM-E.

UNIVERSAL TONE GENERATOR - TN852

7.34 The Universal Tone Generator service circuit will provide up to 64 different tones on any or all of the 32 time slots in the DSU service

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group. The tones are generated using erasable, programmable read-only memory (EPROM) to store the digital samples (mu 255 PCM) or (A-law PCM) of each tone. Eight hundred samples of each tone are repeated until they fill 1K bytes of memory and are stored in EPROM to provide tone generation with frequencies possible at 10-Hz intervals. Thus, all frequencies generated will be within ± 5Hz of specification.

K. Introduction

7.35 A functional block diagram of the Universal Tone Generator (UTG-E) is shown in Figure 12. This circuit can be separated into two distinct groups – a functional group and a maintenance group. The functional group is the circuitry that performs the actual tone generation on the UTG-E. The maintenance group is additional circuitry that monitors, checks, and then permits software access to exercise the UTG-E hardware.

L. Functional

7.36 Timing and synchronization signals required for operation of the UTG-E are derived from the 4 MHZCKN and the 8KSYNC signals, which are inputs from the Local Digital Service Unit Common Board - Export (LDSUCOM-E).

7.37 Proper operation of the UTG-E is determined by control signals (CONTROL IN on Figure 12) that are received from the Switching Module Processor Unit (SMPU) via the LDSUCOM-E. The data control section serves as the distribution point for these signals shown as CIN in Figure 12. These signals are inputs to the maintenance register, loop register, clear generate register, time slot select register (TSSR), interrupt register, and parity generator gate array.

7.38 Control signals perform either a write-to or a read-from a

register. At the end of a write or read command to a register in the UTG-E, an all-seems-well pulse (ASW in Figure 12) is returned to the SMPU via the LDSUCOM-E. This signal indicates only that a write or read was performed by the associated register. When a read command is sent to a particular register, the register will clock out the data that exists at its input. This data appears on the DTRD lead and is sent to the SMPU via the LDSUCOM-E at a 2-MHz rate.

7.39 Two 10-bit counters (address and parity) are used in the UTG-E. These counters count an 800-count sequence starting at 224, incrementing to 1023, and resetting to 224 again. The address counter provides the lower 10 bits (A0 through A9) of address for the EPROMs. The parity counter checks the address counter, and its outputs are used as inputs to the Parity Check Circuit. Both counters are clocked by the 8-Hz CTRSYNC pulse. These counters can be stopped, cleared, and incremented under program control for diagnostic purposes.

7.40 The TSSR gate array is a per time slot controller used in conjunction with a 38A memory to produce eight control outputs for every 3.906-usec time slot. The 38A is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC and LDSUCOM-E with the TSSR operating as a memory controller. The TSSR autonomously reads the 38A memory once per time slot to fetch the eight control bits for the next time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906-usec time slot and are held valid for the remainder of the time slot to provide control functions on a per-time-slot basis.

7.41 The UTG uses seven of the TSSR's eight output control bits. Three

bits (A10 - A12) are used to select one of eight memory address levels in the eight EPROMs that store the digital tones. Two of these bits (A10 and A11) are also used as address leads for the Parity Bit Store EPROM. Three bits (A13 - A15) are used as inputs to a three-to-eight-line decoder to enable one of eight EPROMs. These three bits are also used as inputs to to a one of eight data selector that selects a parity bit column in the parity bit store. Finally, one bit (ACTTS) is used to mask data from appearing at the UTG-E output (force all zeros) for unused time slots.

7.42 Eight EPROMs are used to store the digital tones in the UTG-E. The circuit is wired to accept 2764A (8K x 8) EPROMs.

7.43 Each tone occupies the upper 800 contiguous bytes of memory in a 1024-byte memory block. Therefore, a 2764A EPROM will store eight tones. Eight 2764s allow 64 tones to be stored. Tones are stored either as true sign, magnitude inverted 8-bit mu 255 PCM code (sign bit, plus seven data bits), or true sign, even magnitude bits inverted 8-bit A-law PCM code (sign bit, plus seven data bits).
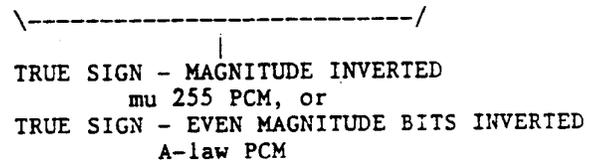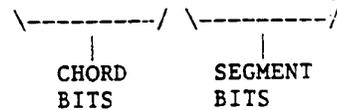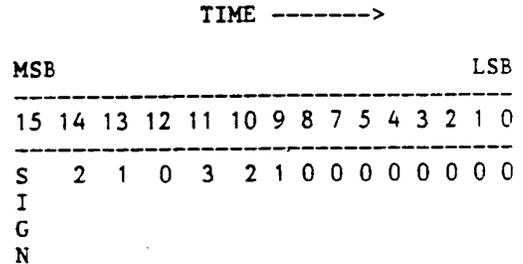
7.44 Ten bits, A0 through A9, from the address counter provide the address of the stored tones. Three bits, A10 through A12, from the TSSR select tones 0 through 7 in each EPROM, and the desired EPROM is enabled by the three-to-eight line decoder, which has for its control inputs three bits, A13 through A15, from the TSSR.

7.45 The output circuit includes the parallel input serial output register (PISO) and the parity generator.

7.46 The PISO receives the 8-bit parallel data from the EPROM parallel data bus for all time slots and converts these inputs to a 32 time

slot 4-MHz, 16-bits-per-time slot, input for the parity generator. The time slot data format is shown below.

PISO OUTPUT TIME SLOT DATA FORMAT

TIME ------->

```
MSB                                  LSB
-----------------------------------------
15 14 13 12 11 10 9 8 7 5 4 3 2 1 0
-----------------------------------------
S   2  1  0  3  2 1 0 0 0 0 0 0 0 0
I
G
N

   \---------/ \---------/
        |            |
      CHORD        SEGMENT
      BITS          BITS

\---------------------------/
              |
```

TRUE SIGN - MAGNITUDE INVERTED
        mu 255 PCM, or
TRUE SIGN - EVEN MAGNITUDE BITS INVERTED
        A-law PCM
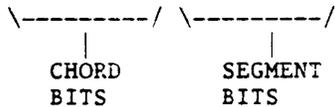
Bits 0 through 7 will be all "0"s.

For time slots masked by the ACTTS bit in the TSSR, the output from the PISO will be 16 "0"s.

7.47 The parity generator includes two 16-bit registers with write-only capability. One register addresses time slots 0 through 15. The other register addresses time slots 16 through 31. All bits in both of these registers should be set low ("0") for normal operation. For this condition, the parity generator checks the data input from the PISO and generates a parity bit to provide odd parity output on the data bit stream; that is, an odd number of "1"s resides in the 16 bits of output for each time slot. The parity bit location is shown in the UTG-E DATA OUTPUT FORMAT shown below.

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UTG-E DATA OUTPUT FORMAT

```
                  TIME ------->

MSC                                    LSB
------------------------------------------
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
------------------------------------------
S   2  1  0  3  2 1 0 0 0 0 0 0 0 0  P
I                                    A
G                                    R
N                                    I
                                     T
                                     Y
                                    (ODD)

   \---------/ \---------/
        |           |
     CHORD       SEGMENT
      BITS        BITS

\----------------------------/
              |
TRUE SIGN - MAGNITUDE INVERTED
       mu 255 PCM, or
TRUE SIGN - EVEN MAGNITUDE BITS INVERTED
       A-law PCM
```

Bits 1 through 7 will be all "0"s. Even parity can be forced on time slots 0 through 31 by writing the appropriate parity generator register time slot bit (or bits) to a "1". This feature is used for diagnostics.

M. Maintenance

7.48 Each DSC, including the UTG-E, has a maintenance register and an identification loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out-of-service lamp, and another is looped back to the identification loopback register for control channel verification. The identification loopback register, when read, returns the looped bit and a 7-bit UTG-E identification code. Each DSC type has a unique code.

N. Interrupt Register

7.49 Self maintenance checks are continually performed in the UTG-E. The Interrupt Register monitors the output from these maintenance circuits and when a fault occurs, it latches the fault into an internal register and reports to the LDSUCOM-E that a fault has occurred. This is done autonomously and is indicated by the normal "1" level on the DSCFLN interface lead between the UTG-E and LDSUCOM-E going to a "0" level. The interrupt register is an 8-bit register with both write and read capability. At this time, only five bits are used. The write function is used to mask interrupts. Writing a "1" to a particular bit position prevents an interrupt from occurring at the interrupt register FLTINT output (refer to Figure 12) even though a fault signal for that bit position has occurred at the input to the interrupt register. With the mask written for all "0"s, all interrupts are enabled. If a fault occurs, and it is reported to the LDSUCOM-E as previously described, a subsequent read command can be issued to the interrupt register to determine the cause of the interrupt. After a fault has been cleared, the interrupt register can be cleared by writing the CLRINT bit in the clear generate register to "1".

7.50 The five bits presently used on the interrupt register are utilized as follows: One bit indicates the loss of the 4-MHz clock at the input to the clock check circuit. One bit indicates the loss of the 8K sync input to the sync check circuit. One bit indicates the absence of the 8K sync input to the TSSR. An interrupt will also occur at this bit position if the parity check circuits inside the TSSR detect a parity failure at the 38A memory. This indicates a memory failure or internal logic failure of the TSSR. This error can be forced by writing the parity invert bit on the TSSR to a "1" during any write

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order to the TSSR. One bit indicates that a fault occurred in the parity check circuit. Finally, one bit indicates the loss of the 8K sync input to the parity generator gate array. Maintenance circuits in the UTG-E that cause interrupts as a result of the absence of 4MHz clock and 8K sync can be checked during diagnostic routines by disabling the clock and the sync signals at the output of the LDSUCOM-E.

O. Parity

7.51 Extensive parity is used for fault detection in the UTG-E. Parity is checked across address and data for all tone EPROMs. The description that follows implies the use of eight 8K by 8 EPROMs (2764A) for tone data and one 8K by 8 EPROM (2764A) for parity. This is the arrangement used for the export version of the UTG-E.

7.52 The 10 bits, A0 through A9, as shown in Figure 13, provide the lower 10 bits of address (224 - 1023) for all tones. The three bits, A10 through A12, select one of eight memory address levels (one of eight tones) in each 2764A EPROM. Also, the last three bits, A13 through A15, enable only one of the eight EPROMs which places the addressed byte of data on the parallel data bus.

7.53 A computer program has been developed to determine the correct parity bit "1" or "0" that should be loaded into the parity bit store EPROM for each address and each byte of data addressed.

7.54 Parity bits for all tones located in levels 0 through 7 of each EPROM stored in one EPROM. These bits are arranged in the parity bit store EPROM as 1 bit x 800 word groups, with the lowest addressable parity bit occupying the least significant bit position of location 224 in the parity EPROM.

7.55 Addressing for these parity bits is as described here. The same 10 bits, A0 through A9, that addressed the EPROMs used for storing the digital tones provide the lower 10 bits of address for all parity bits. Bits A10 through A12 select one of eight memory address levels in the parity bit store EPROM. The column selection of the 800 bit slice of the desired parity bits is made by the one of eight data selector which is connected to the eight data out leads of the parity EPROM and is controlled by bits A13 through A15. The result is that only one parity bit is output for each tone address location.

7.56 As shown in Figure 13, the parity counter uses the same clock input as the address counter. The two counters are synchronized through software initialization for the UTG-E. The 10 bits, A0 through A9, from the parity counter are inputs to the parity check circuit as is the PA10A15 lead from the TSSR, which represents parity across A10 through A15. In addition, the parity bit output from the one-of-eight data selector and the eight bits from the parallel data bus are used as input to the parity check circuit.

7.57 Internal to the parity check circuit, the 10 bits of address from the parity counter, and the parity result across A10 through A15 from the TSSR are used as inputs to a parity generator, the output of which represents the parity across the full 16 bits of address. The eight bits of data also are used as inputs to a parity generator. The output from these two parity generators is exclusive OR-ed. The output from this exclusive OR circuit is parity across 16 bits of address and eight bits of data. This signal is connected to the input of a second exclusive OR circuit, which has for its other input the parity bit from the parity bit store. The parity developed across data and

address is compared on a per-time-slot basis with the parity bits stored in the parity bit store. This output is connected to a NAND gate, which has, as its other input, a strobe pulse for sampling the parity result at a time when it is stable. The output from this NAND circuit is used as an input to the interrupt register.

7.58 Normal operation results in a high-level "1" on the parity check circuit output lead connected to the interrupt register for all time slots. However, should a problem occur in either the address or parity counter TSSR, three-to-eight line decoder, any bit of tone data or parity in the EPROMs, or the one-of-eight decoder, the output from the parity check circuit will go low "0" when strobed and will latch a PARINT fault in the interrupt register which will be reported to the LDSUCOM-E via the DSCFLN interface lead between the UTG-E and the LDSUCOM-E.

UNIVERSAL CONFERENCE CIRCUIT - TN841/TN851

7.59 The TN841/TN851 circuit pack provides the function of conference calling for 5ESS. Only 3-party conference calls will be performed by the TN841/TN851. The present TN841/TN851 design allows five simultaneous 3-port conference calls on a single TN841/TN851 circuit pack. In addition to the 3-party calling feature, the conference circuit can be used for "busy line verification" as well as in conjunction with the "service evaluation system." The TN841 is the u-law version of the universal conference circuit. The TN851 is the a-law version.

7.60 Busy line verification involves processing of the signaling bits in addition to the normal conference processing of the PCM signals. This verifies the ON or OFF hook status of

the line in question and requires that an interchange of the A signaling bits be performed on the incoming time slots. The following example illustrates this process.

7.61 Assume a 2-party call is in progress between parties A and B. The operator is requested to verify the A party's line to see if a call is indeed in progress. The 5ESS reconfigures the call as a 3-port conference call with the operator bridged on as the "C" party. It is required that the A signaling bit from the A party be output on both the B and C (operator) time slots and that the A signaling bit from the B party be placed on the A party's outgoing time slot. The interchange of the signaling bits takes place in the TN841/TN851 as part of the conferencing algorithm.

7.62 When the line is verified, the C (operator) input time slot to the conference circuit shall contain idle code (0x7F). Busy line verification calls must be configured as indicated above, that is, the A party is the line to be verified; the B party is the second party of the original call; and the C party is the operator. A, B, and C refer, respectively, to the first, second, and third time slots assigned to the conference connection.

P. Introduction

7.63 The block diagram of the universal conference circuit (UCC) is shown in Figure 14. This circuit can be separated into two distinct groups: a functional group and a maintenance group. The functional group is the circuitry that performs the actual conferencing function. The maintenance group is additional circuitry that performs monitoring and checking and permits software access to exercise the UCC hardware.

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Q. Functional

7.64 Referring again to Figure 14, timing and synchronization signals required for operation of the UCC are derived from the 4MHZCKN and the 8KSYNC signals, which are inputs from the GDSUCOM-E. The timing and synchronization circuit also supplies the clock signals required by the digital signal processors (DSPs) which perform the conferencing algorithm. These are shown in Figure 14 as 4MHZ, 4MHZI, and 4MHZO. 4MHZ is used to control the frequency of each DSP clock generator; 4MHZI is used to shift data bits into each DSP; and 4MHZO is used to shift data bits out of each DSP. DSPSYNC, 0C0 through 4C0 are used for synchronization of the DSPs.

7.65 Proper operation of the UCC is determined by control signals (CONTROL IN on Figure 14) that are received from the switching module processor unit (SMPU) via the GDSUCOM-E. The data control section serves as the distribution point for these signals shown as CIN in Figure 14. These signals are inputs to the maintenance register, loop register, clear register, parity check register, time slot select registers (TSSRs), interrupt register, parity generator, and the DSP control and status registers.

7.66 Control signals perform either a write to or a read from a register. At the end of a write or read command to a register in the UCC, an all seems well pulse (ASW in Figure 14) is returned to the SMPU via the GDSUCOM-E. This signal indicates only that a write or read was performed by the associated register. When a read command is sent to a particular register, the register will clock out the data that exists at its input. This data appears on the DTRD lead and is sent to the SMPU via the GDSUCOM-E at a 2.048-MHz rate.

7.67 The DSPs must be reset before each new conference call. ORESET through 4RESET are used to enable this function in the 0DSP through 4DSP, respectively. These reset pulses are provided by the clear generate register. This register produces a single pulse output in the desired bit position when addressed. It is not required to remember the state of this register because the register automatically clears after each write. The clear generate register also is used to clear the interrupt register, as well as the parity fault register in the parity check gate array.

7.68 Two time slot select registers (TSSRs) are in the UCC. The TSSR gate array is a per-time slot controller used in conjunction with a 38A memory to produce eight control outputs for every 3.906 usec time slot. The 38A is functionally used as a 32 x 9-bit memory with eight data bits and a parity bit developed over address and data. The memory is writable and readable via the PCC and GDSUCOM-E with the TSSR operating as a memory controller. The TSSR autonomously reads the 38A memory once per-time slot to fetch the eight control bits for the next time slot. The control bits are synchronously latched at the TSSR output at the beginning of each 3.906 usec time slot and are held valid for the remainder of the time slot to provide control functions on a per-time-slot basis.

7.69 The UCC uses all of the OTSSRs eight output control bits. Five bits (0ISY through 4ISY) are used to control the data input to the 0 through 4 DSPs, respectively. One bit (DSPSYNC) is used to synchronize the time-slot data inputs to each DSP with the program that resides within each dsp in ROM. This bit is brought high ("1") for the first active time slot associated with each DSP. This serial

pulse train (2 pulses maximum) is used as an input to the timing and sync circuit. The outputs from the timing and sync circuit, as a result of the DSPSYNC, are 0CO through 4CO, which are inputs to the 0 through 4 DSPs, respectively. The DSPs will remain in a suspended state (the program does not continue) until a CO pulse is received. These pulses are timed (1 per frame) to occur at the time the data for the first of the three time slots associated with that DSP is loaded into the DSP input buffer. One bit (EMASK) is used on a per-time-slot basis to prevent parity faults that are detected in the parity check circuit from being latched into the 32-bit parity fault register in the parity check circuit. This bit also prevents these same parity fault signals from occurring on the DSCPEN interface lead between the UCC and the DSUCOM. Another bit (IMASK) is also used on a per-time-slot basis and allows parity faults detected in the parity-check circuit to be latched into the 32-bit parity fault register in the parity check circuit, but prevents these faults from being reported to the GDSUCOM-E on the DSCPEN signal lead.

7.70 The UCC uses only five of the 1TSSR's eight output control bits. These five bits (0OSY through 4OSY) control the data output from the 0 through 4DSPs, respectively. These bits are set high ("1") for the same time slots selected for the 0ISY through 4ISY bits in the 0TSSR.
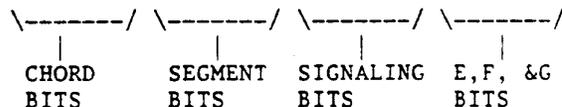
Input data to the UCC is from the time slot interchange unit (TSIU) via the GDSUCOM-E. This input is a 4.096-MHz, 32-time-slot, 16-time-per-time-slot, serial-bit stream.

The input time slot data format is shown below.

UCC INPUT TIME SLOT DATA FORMAT

TIME -------->

```
MSB                                      LSB
-------------------------------------------
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
-------------------------------------------
S  2  1  0  3  2 1 0 A B C D E F G P
I                                    A
G                                    R
N                                    I
                                     T
                                     Y
                                   (ODD)

   \-------/ \-------/ \-------/ \-------/
       |         |         |         |
    CHORD      SEGMENT   SIGNALING  E,F, &G
    BITS       BITS      BITS       BITS

   \---------------/
           |
```

TRUE SIGN - MAGNITUDE INVERTED
     mu 255 PCM (TN841) or
TRUE SIGN - EVEN MAGNITUDE BITS INVERTED
     A-LAW PCM (TN851)

7.71 The 32 time slots of data are reclocked and then used as an input to the parity check circuit. The parity check circuit includes two 16-bit registers with read only capability. One register holds parity input errors for time slots 0 through 15. The other register holds parity errors for time slots 16 through 31. Internal to the parity check circuit, the data input (16 bits) for each time slot is checked for odd parity. If bad

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(even) parity is detected for any time slot, the error for that time slot is latched into the corresponding time slot position in the related register. In addition to latching the parity error into the register, the error is also reported to the GDSUCOM-E via the DSCPEN signal lead. If a parity error occurs, and is reported to the GDSUCOM-E as previously described, a subsequent read command can be issued to the parity check circuit to determine the time slot that caused the fault. After a fault has been cleared, the parity check circuit registers can be cleared by writing the CLRPCHK bit in the clear register to "1". Two mask bits (EMASK and IMASK) are provided in the OTSSR for inhibiting the parity check parity errors. These bits were described previously.

7.72 The PCHKPI bit in the maintenance register can be used to force even parity on the data output from the parity check circuit. This affects the parity on all time slots. Forcing even parity with PCHKPI does not cause a fault in the parity checker in the parity check circuit.

Also, the absence of the 8K sync input to the parity check circuit will cause the PCSYNCE interrupt bit in the interrupt register to be set.

7.73 Figure 15 shows the time slot assignment format required by the UCC. As shown, up to 30 time slots are available for a UCC. The reserved time slots may be even or odd, as shown. The 30 time slots are divided into 10 groups of three each. Each group consists of every tenth time slot, e.g., time slots 0, 10, and 20 for the first group. Any of the DSPs may be assigned to any of the 10 groups. The assignment of the first time slot in the first group is not restricted to time slot 0 as shown, but may range from 0 through 31. However, it is required that every tenth time slot format be maintained. That is, if the first group is selected to be time slots 1, 11, and 21, the tenth group of time slots would be 10, 20, and 30.

7.74 The DSP is a programmable digital signal processor. The program for each DSP is contained in internal ROM. The frequency of the DSP is controlled by the 4MHz-clock, which is derived from the system clock.

The task for each DSP in the UCC will be as follows:

(a) Input three time slots of 16-bit data (8PCM bits and the A through G bits plus the parity bit).

(b) Perform a 3-port conference algorithm on the eight PCM bits contained in the three time slots.

(c) Perform a time-slot interchange on the A through G bits for the three time slots.

(d) Combine the PCM output bits for each time slot with the proper A through G bits.

(e) Generate an odd parity bit over the output PCM bits and the A through G bits for each time slot. Affix this parity bit "1" or "0" to the parity bit position of the data output.

(f) Provide a means for forcing bad (even) parity on the data output under external program control using the C1 control bit on the DSP.

(g) Perform additional functions by S0, S1, and STB.

7.75 A brief functional description of the DSP I/O leads shown in Figure 14 is given here.

7.76 DI receives the serial data from the Parity Check Circuit, and DO transmits serial data to the parity generator. ISY indicates the start of a data transfer to the input buffer, and ICK shifts bits into the input buffer via DI. CTSO enables the start of a data transfer from the output buffer, and OCK shifts bits out of the output buffer via DO.
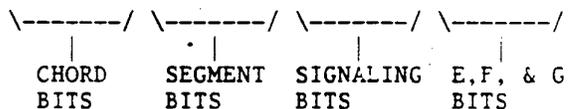
7.77 Control input C0 is tested by the DSP program. This input synchronizes the DSP program with the input of the first of the three time slots associated with the particular DSP. C1, S0, S1, and STB are used in conjunction with the DSP control and status registers.

7.78 Data output from each active DSP consists of three time slots of 4.096 MHz, 16 bits per time slot, data with odd parity. The latter is true provided that the associated DSP control register has the least significant bit written to a "1". The other bits are don't cares. Writing the least significant bit of this register to a "0" will result in bad (even) parity on the data output for the third time slot associated with the conference call and will set the PGPERR in the Interrupt Register. The outputs from the DSPs and the outputs from an idle time slot simulator are multiplexed to form 32 time slots of 4.096-MHz, 16-bits-per-time-slot data. The format for the active time slots is shown below.

TIME SLOT DATA FORMAT

TIME ------->

```
MSB                                    LSB
-------------------------------------------
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
-------------------------------------------
S  2  1  0  3  2 1 0 A B C D E F G P
I                                   A
G                                   R
N                                   I
                                    T
                                    Y
                                  (ODD)

  \-------/ \-------/ \-------/ \-------/
     |        · |        |         |
   CHORD     SEGMENT   SIGNALING  E,F, & G
   BITS      BITS      BITS       BITS

\---------------/
       |
```
TRUE SIGN - MAGNITUDE INVERTED
    mu 255 PCM (TN 841) or
TRUE SIGN - EVEN MAGNITUDE BITS INVERTED
    A-LAW PCM (TN851)

7.79 Idle time slots are filled with 15 "0"s and a "1" in the parity bit position to provide odd parity. The output data is reclocked and then used as the input to the parity generator.

7.80 Internal to the parity generator, the data input (16 bits) for each time slot is checked for odd parity. If bad (even) parity is detected for any time slot, as indicated previously, the error is latched into the PGPERR bit position of the Interrupt Register and will be reported to the GDSUCOM-E

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via the DSCFLN signal lead. This procedure serves to check the basic sanity of the DSP chips (the ability to generate odd parity on its output data) and the integrity of the circuit that multiplexes the DSP data streams together and inserts the "idle" data.

7.81 The parity generator includes two 16-bit registers with write-only capability. One register addresses time slots 0 through 15; the other register addresses time slots 16 through 31. All bits in both of these registers should be set low ("0") for normal operation. For this condition, the parity generator checks the data input and generates a parity bit to provide odd parity output for each time slot. This is done even though a parity bit error may have been detected and reported to the GDSUCOM-E as previously described.

7.82 The parity generator data output format is the same as that shown above, except that it will be delayed in time. Idle time slots are filled with 15 "0"s and a "1" in the parity bit position. Also, the A through G bits have been slot interchanged as described previously.

Even parity can be forced on time slots 0 through 31 by writing the appropriate parity generator register time slot bit or bits to a "1". This feature is used for diagnostics.

R. Maintenance

7.83 Each DSC, including the UCC, has a maintenance register and an identification loopback register. By writing specified bits of the maintenance register active, the three types of outgoing interrupts (parity, fault, and summary scan) can be generated. Also, one bit controls the out-of-service lamp, and another is looped back to the identification loopback register for control channel verification. The identification loopback register, when read, returns

the looped bit and a 7-bit UCC identification code. Each DSC type has a unique code. Finally, one bit of the maintenance register is provided to force bad (even) parity output from the parity check gate array.

S. Interrupt Register

7.84 Self-maintenance checks are performed continually in the UCC. The interrupt register monitors the outputs from these maintenance circuits; when a fault occurs, it latches the fault into an internal register and reports to the GDSUCOM-E that a fault has occurred. This is done autonomously and is indicated by the normal "1" level on the DSCFLN interface lead between the UCC and GDSUCOM-E going to an "0" level. The interrupt register is an 8-bit register with both write and read capability. Only seven bits presently are used. The write function is used to mask interrupts. That is, writing a "1" to a particular bit position prevents an interrupt from occurring at the interrupt register FLTINT output even though a fault signal for that bit position has occurred at the input to the interrupt register. With the mask written for all "0s", all interrupts are enabled. If a fault occurs, and is reported to the GDSUCOM-E as previously described, a subsequent read command can be issued to the interrupt register to determine the cause of the interrupt. After a fault has been cleared, the interrupt register can be cleared by writing the CLRINT bit in the clear generate register to "1".

7.85 The seven bits presently used on the interrupt register are utilized as follows: one bit indicates the loss of 4 MHz clock at the input to the clock check circuit; one bit indicates the loss of the 8K sync input to the sync check circuit; one bit indicates the absence of the 8K sync input to the OTSSR. An interrupt will also occur at this bit position if the parity invert bit (PINV) on the OTSSR

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is set to a "1" for any time slot position. Another bit provides the same function for the 1TSSR. One bit indicates the loss of the 8K sync input to the parity generator gate array. One bit indicates the absence of the 8K sync input to the parity check gate array. One bit indicates that a parity error has been detected on the data input to the parity generator.

REFERENCES

[1] H. A. Kalvonjian and J. A. Palsha, "5ESS Digital Service Circuit Unit Development Specification," DS5C 1.05.05.00, April 24, 1981.

[2] G. J. Brossoni, "5ESS Transmission Test Function Development Specification," DS5D 1.05.08.00, August 22, 1980.

[3] G. J. Brossoni, "Design Requirements for Export Application of 5ESS Transmission Test Function (TTF)," DS5RE 1.05.08.02, January 15, 1982.

[4] T. J. Chiu, "Multiple Global Digital Services Unit System Test Results," May 9, 1984.

[5] H. A. Kalvonjian, "Gate Array Designs for the 5ESS DSU," Memorandum for File, January 15, 1981.
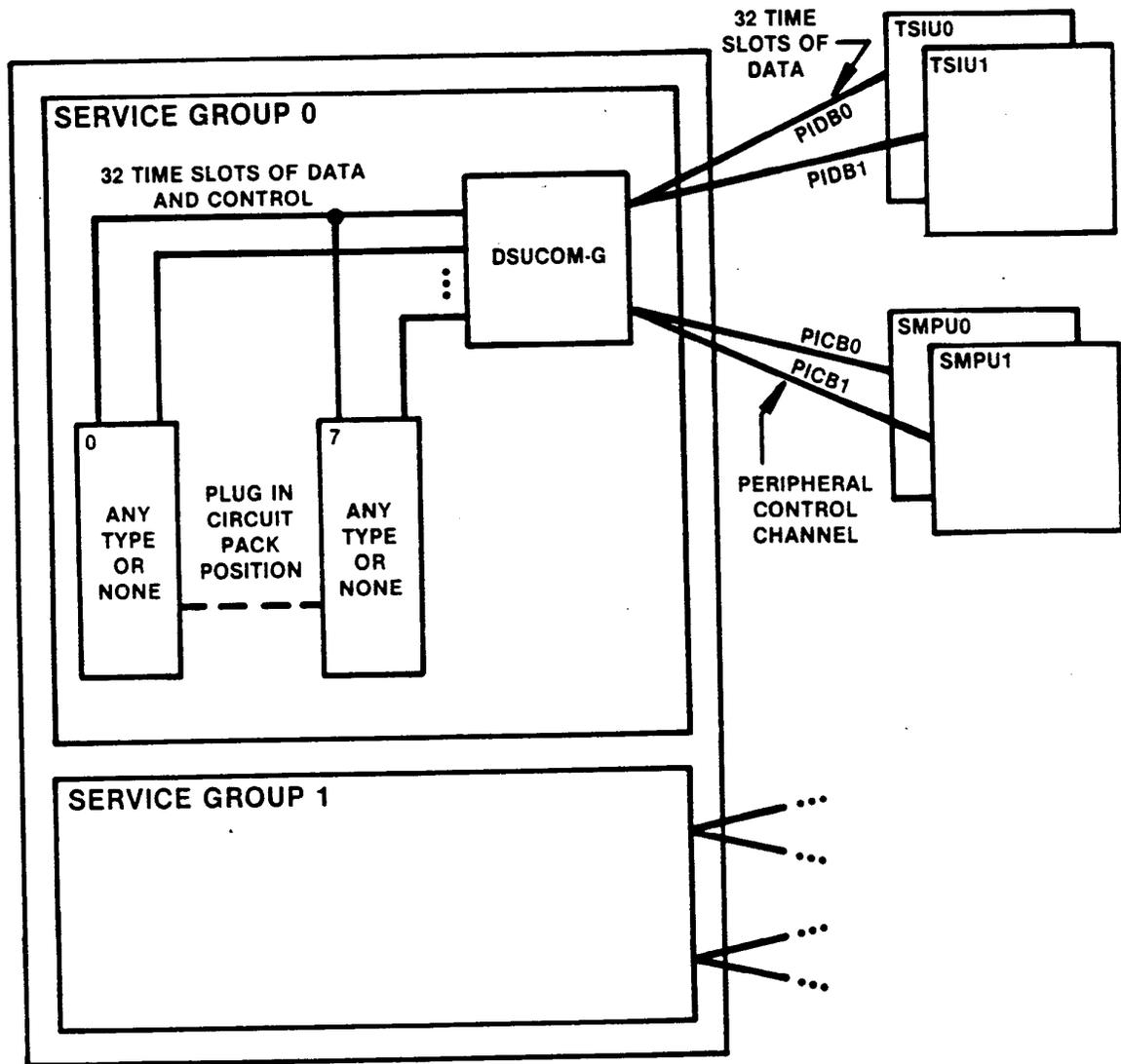
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Figure 1   Global Digital Service Unit Architecture
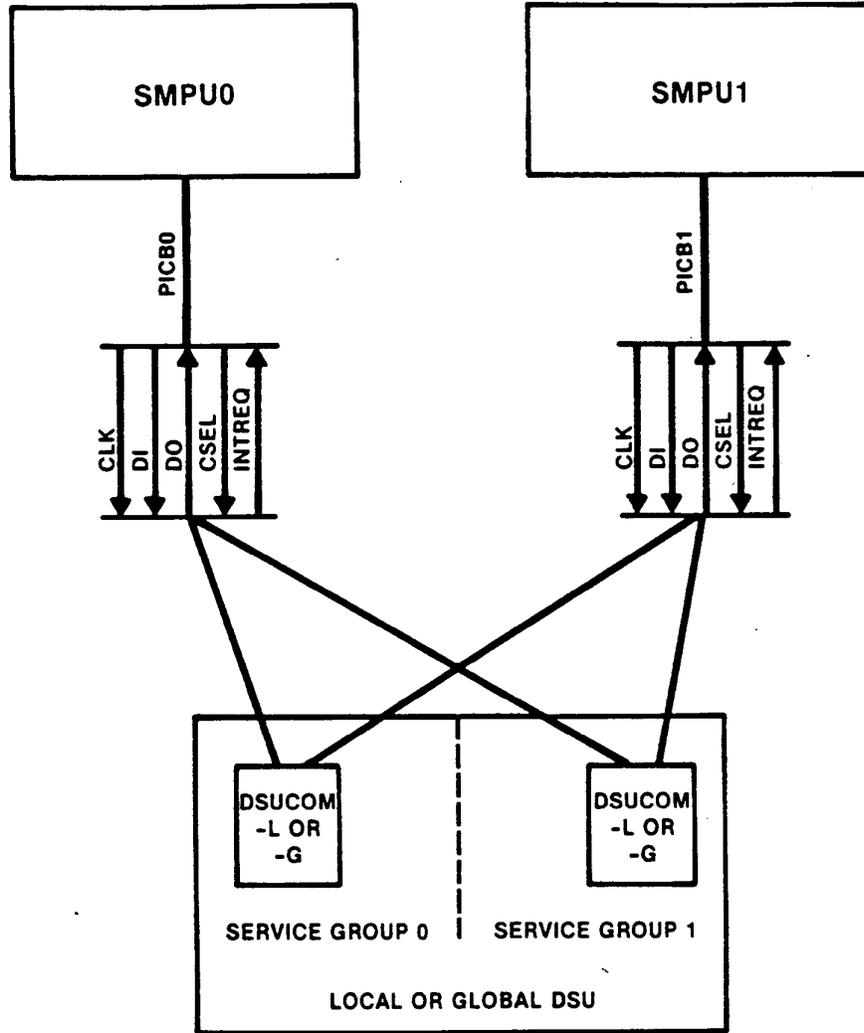
IHM41918A13
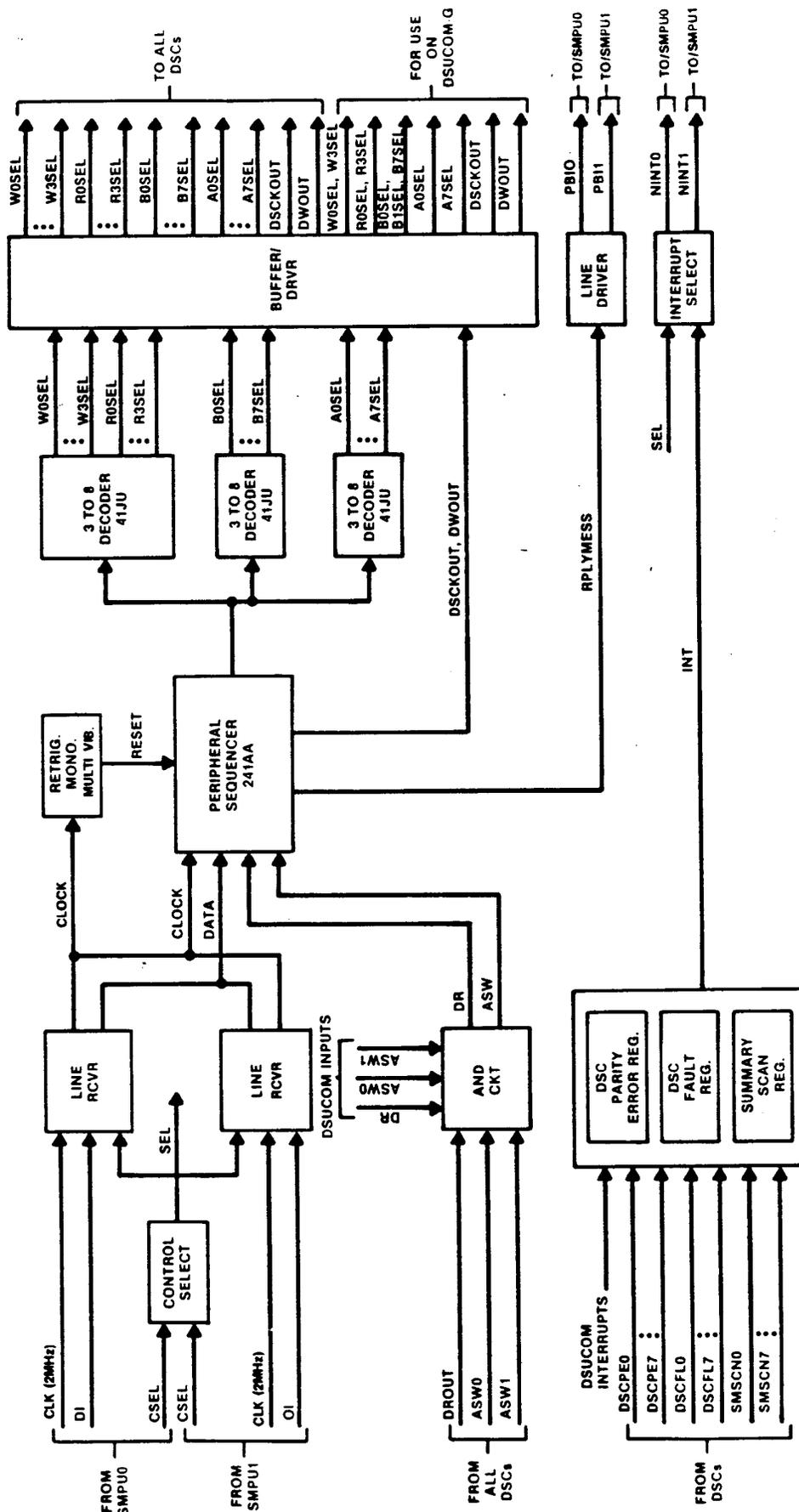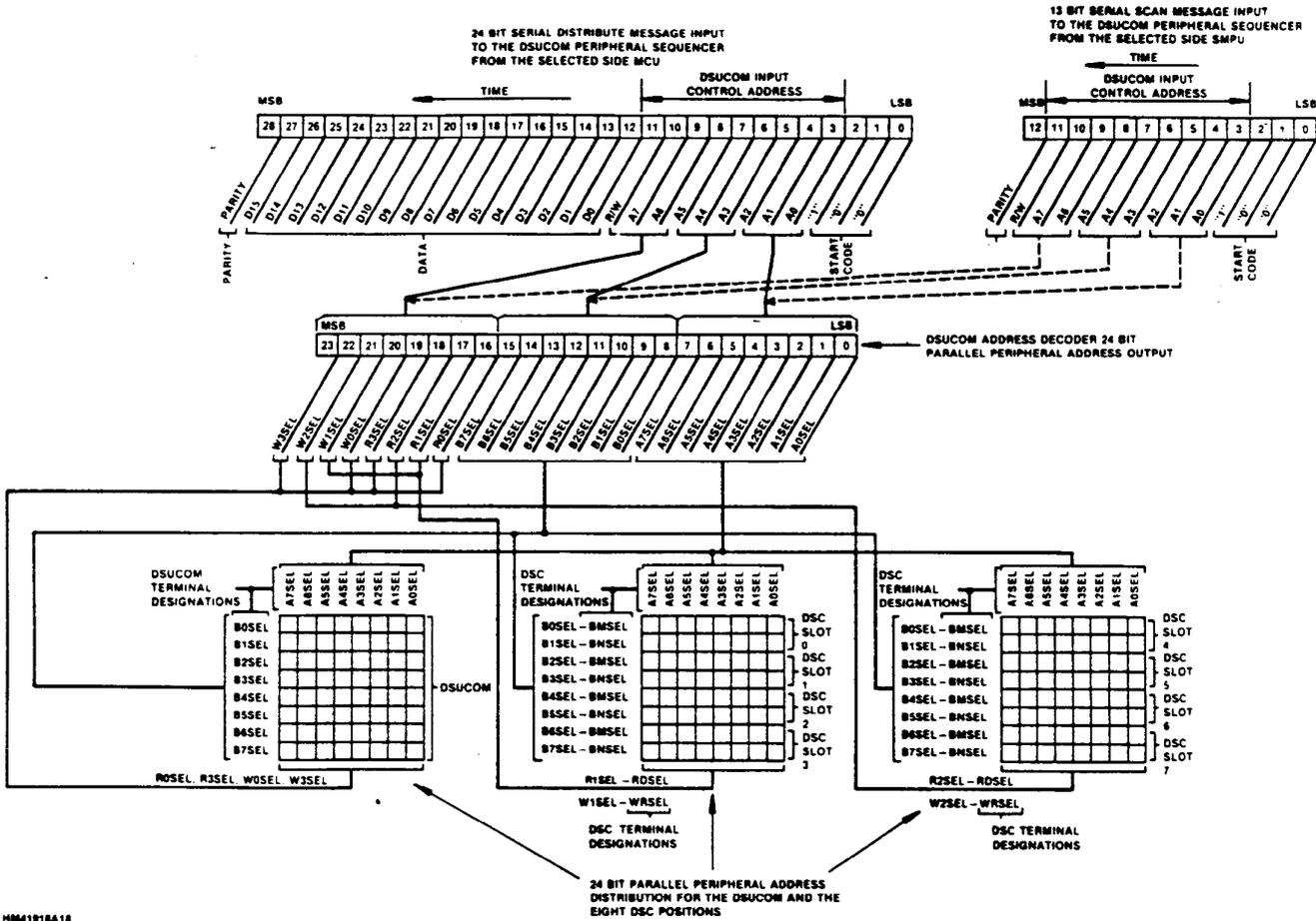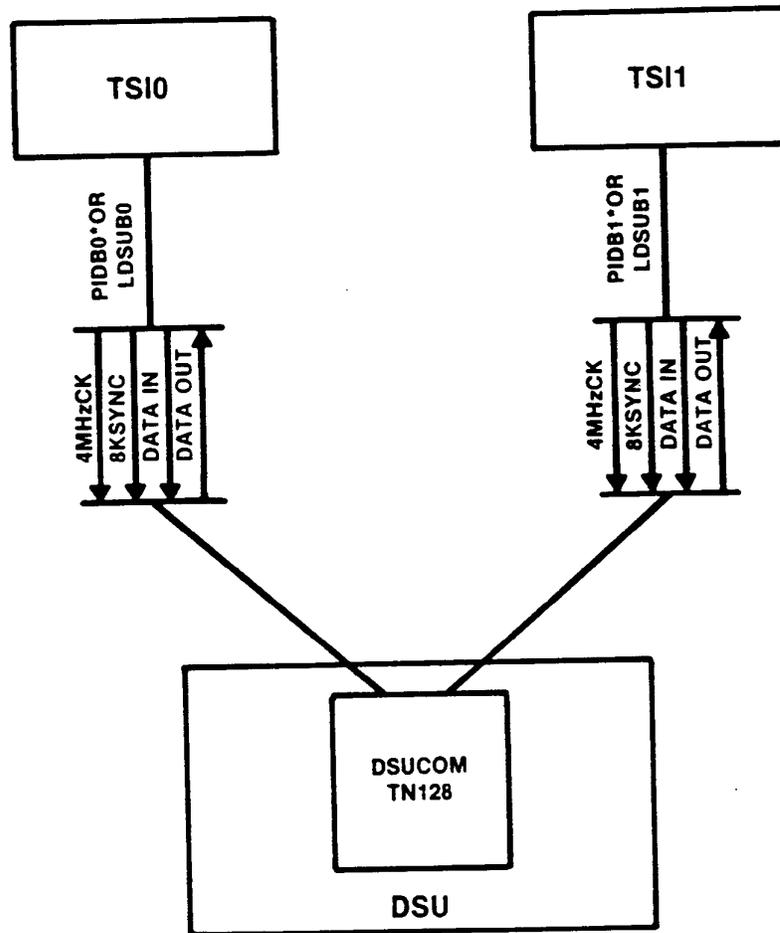
L: LOCAL
G: GLOBAL

Figure 2   DSU Control Interface

Figure 3 DSUCOM-G Control Interface

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Figure 4   Global DSU Control Address

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*PIDB IS ASSOCIATED WITH A GLOBAL DSU
AND LDSUB IS ASSOCIATED WITH A LOCAL
DSU. ELECTRICALLY BOTH BUSSES ARE
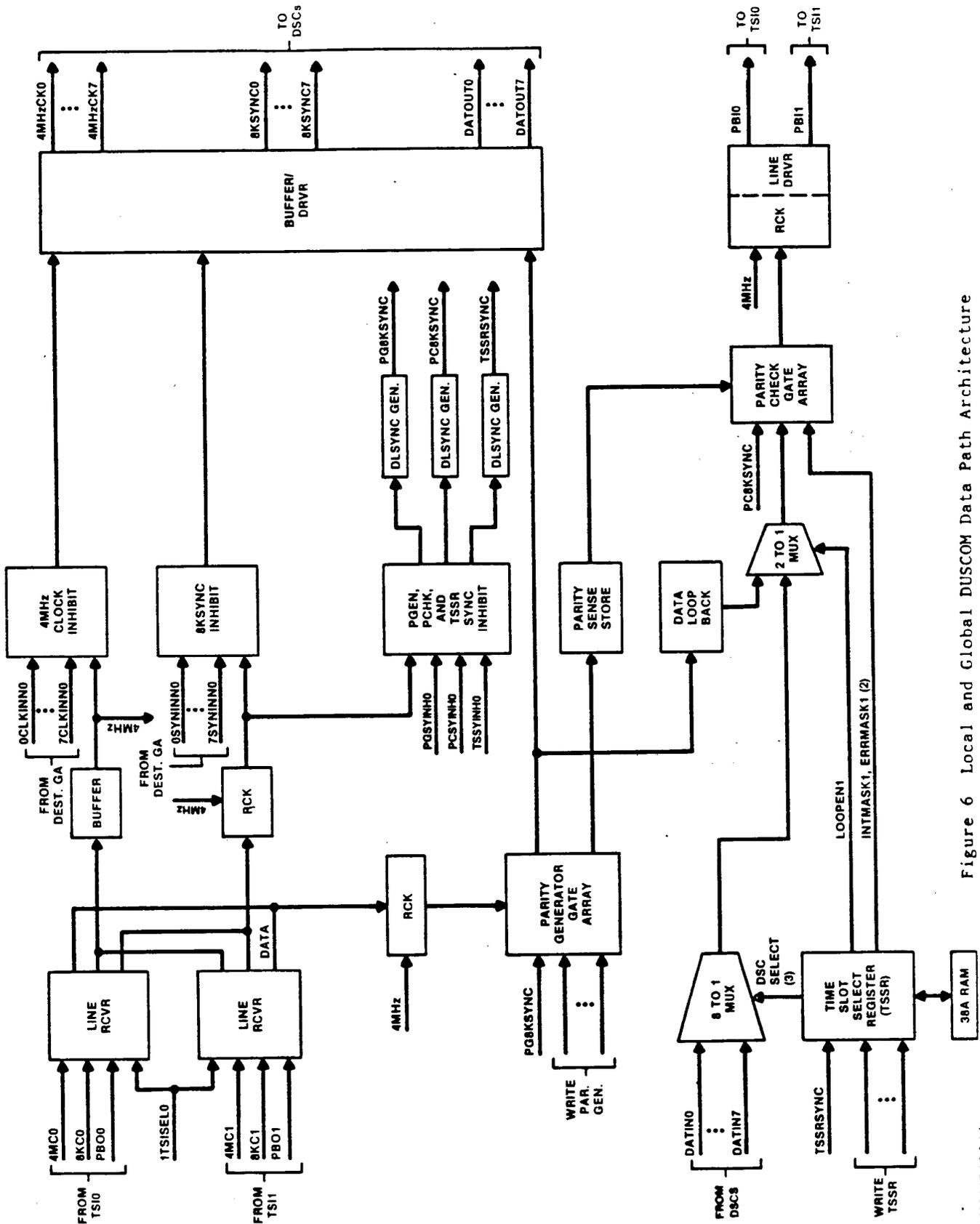THE SAME.

Figure 5   Peripheral Interface Data Bus

IHM41918A10

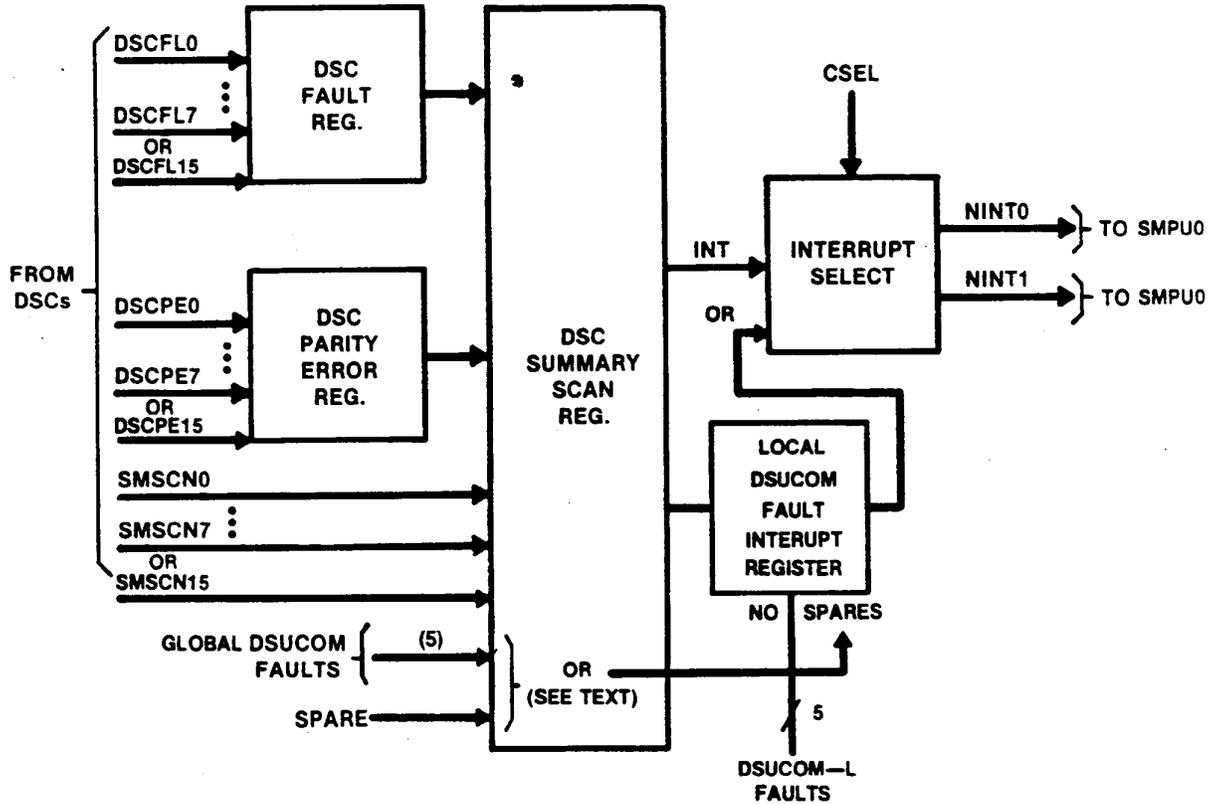Figure 6 Local and Global DUSCOM Data Path Architecture
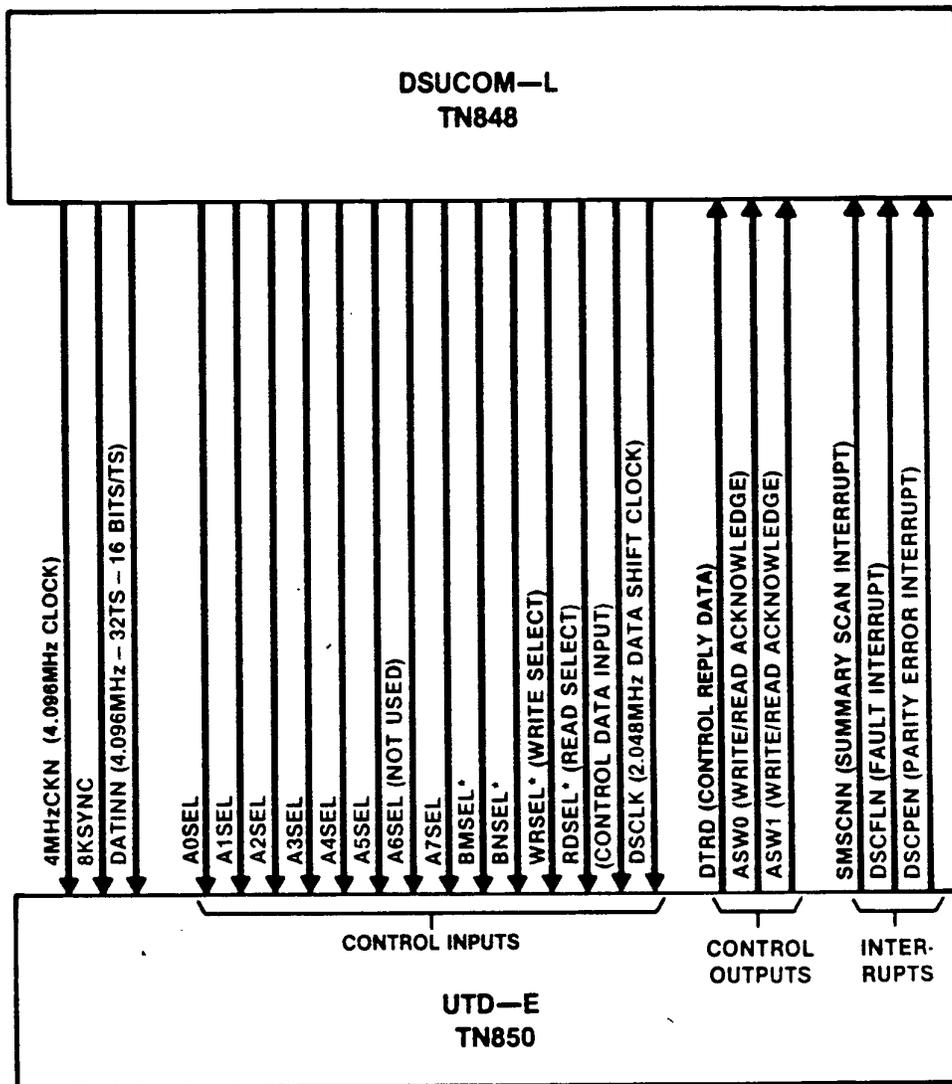
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IHMA1Q1RA11

Figure 7 Local and Global DUSCOM Intercept Architecture

*THESE SIGNALS ARE SLOT POSITION DEPENDENT.
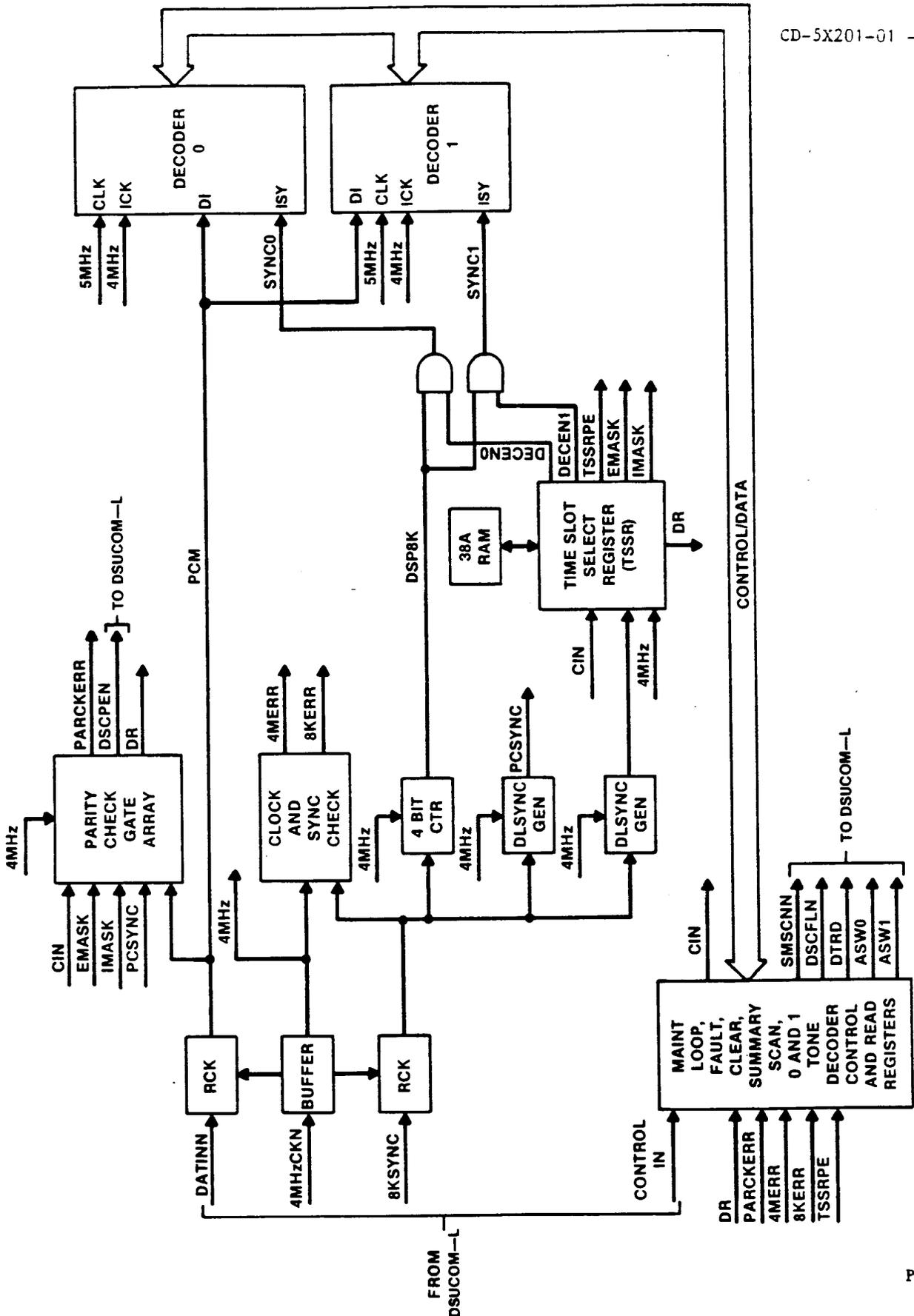
IHM41918A14

Figure 8   DUSCOM - UTD Interface
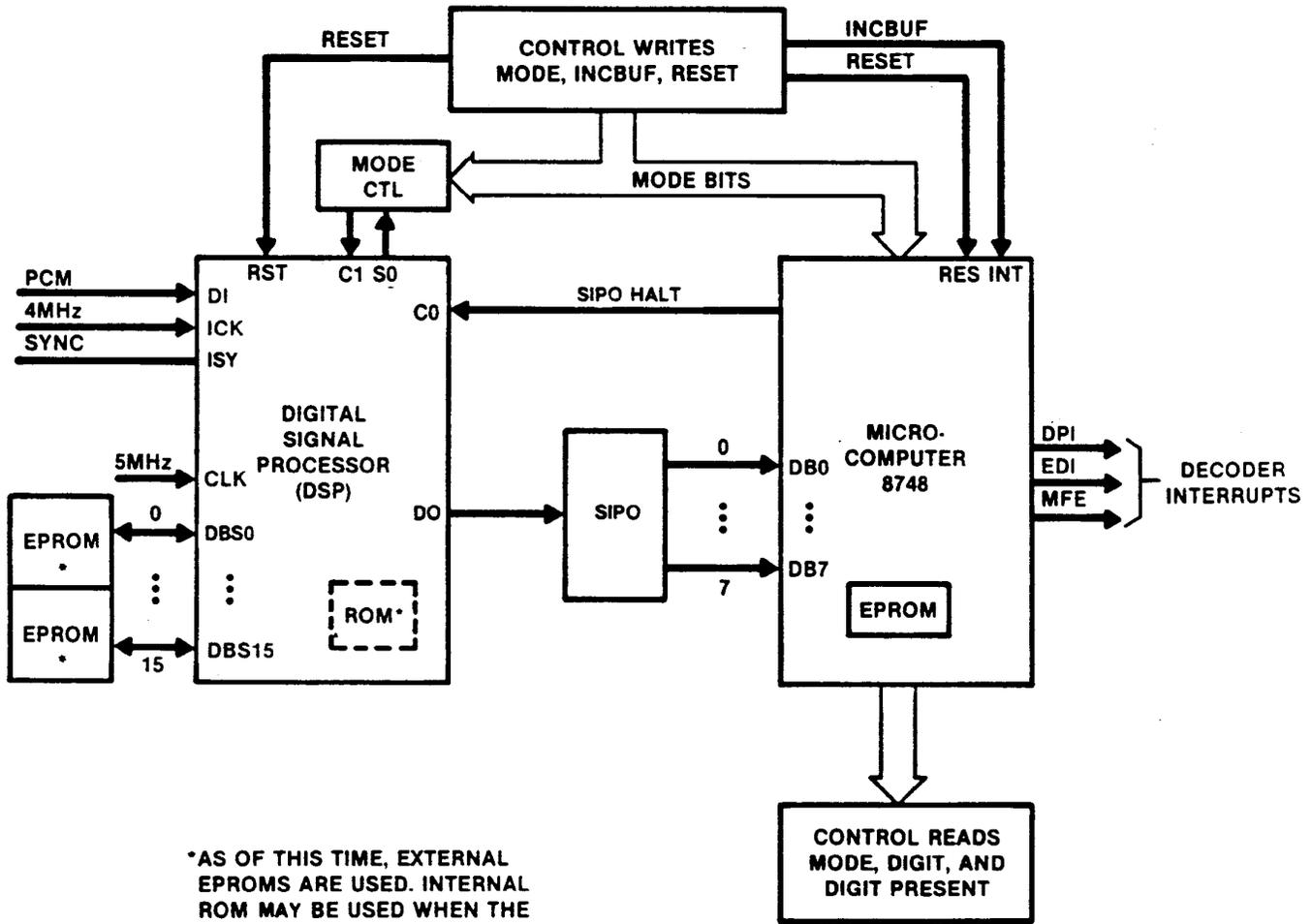
Figure 9 Universal Tone Decoder (UTD)

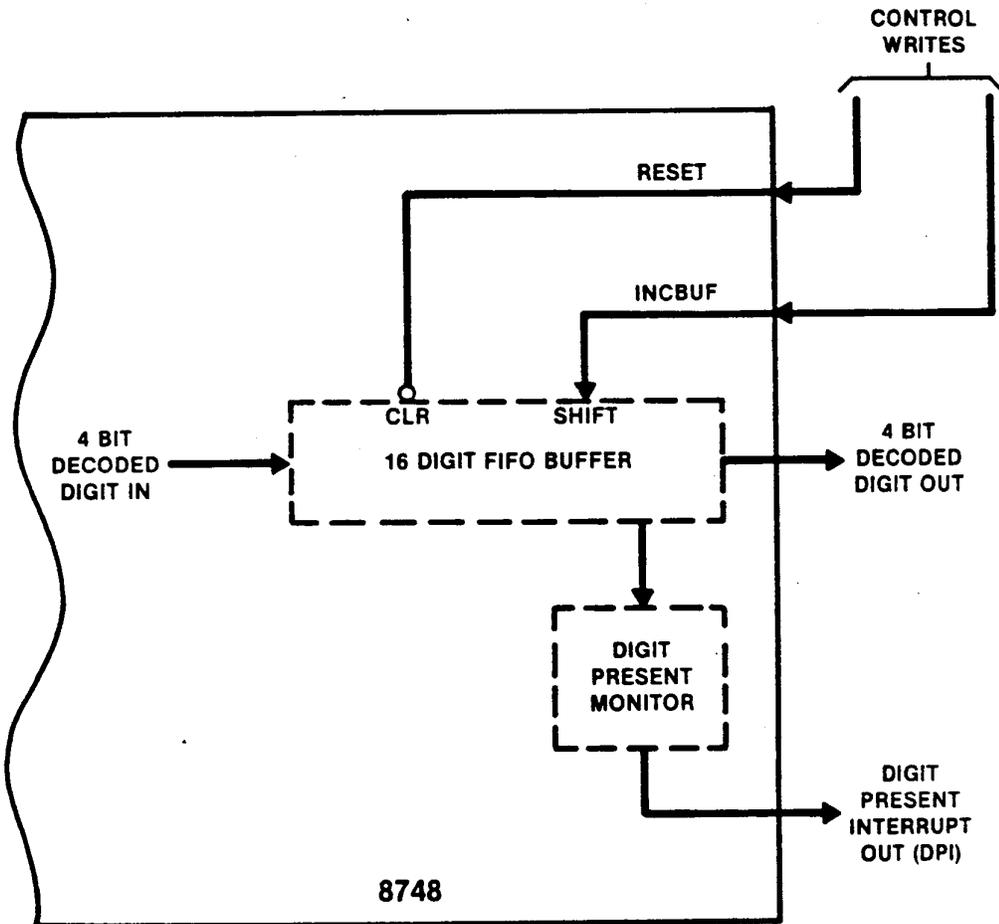Figure 10   UTD Decoder Architecture

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Figure 11   8748 Software FIFO Buffer

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FIGURE 12 Universal Tone Generator Circuit Pack
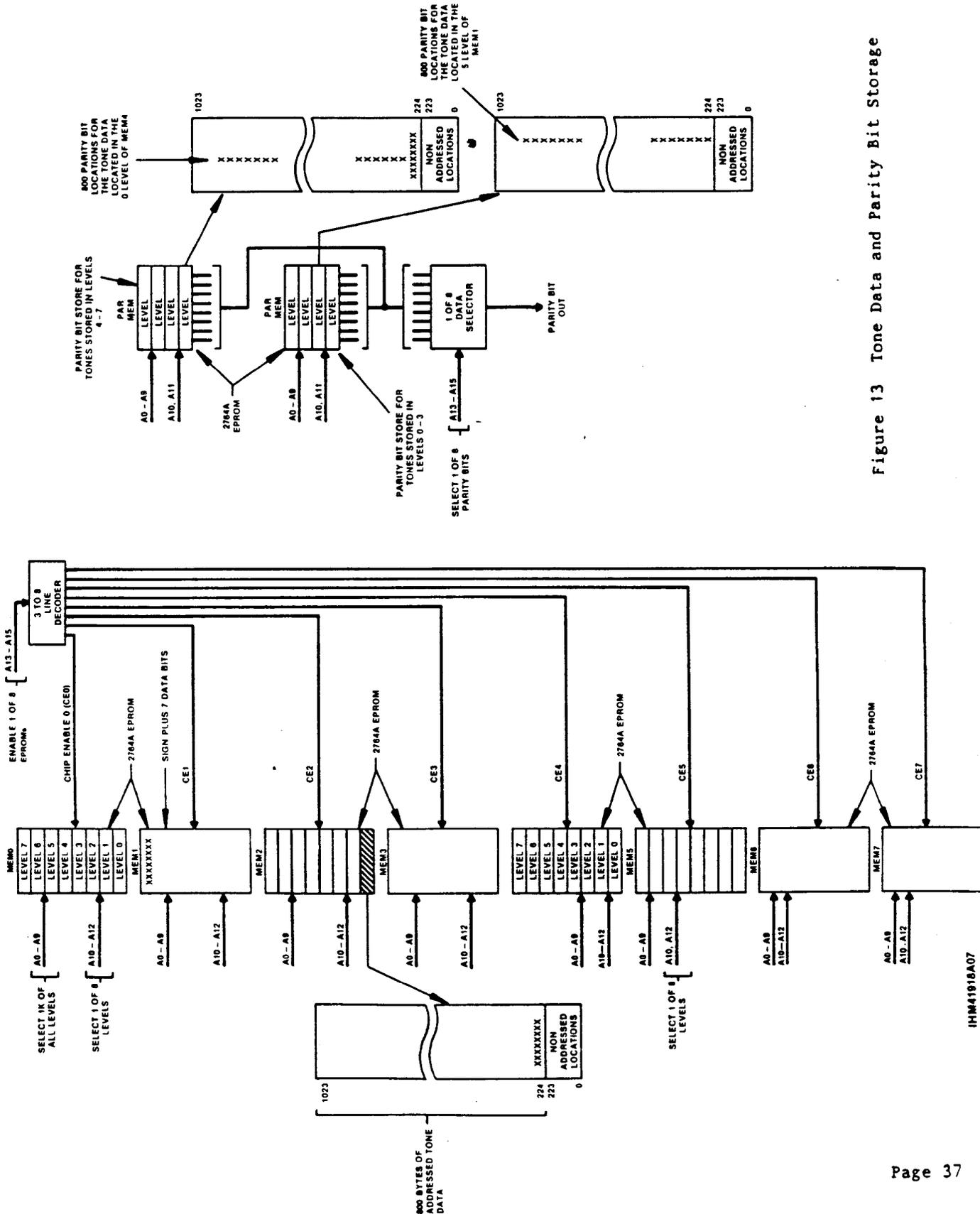
Figure 12 Universal Tone Generator Circuit Pack

Figure 13 Tone Data and Parity Bit Storage

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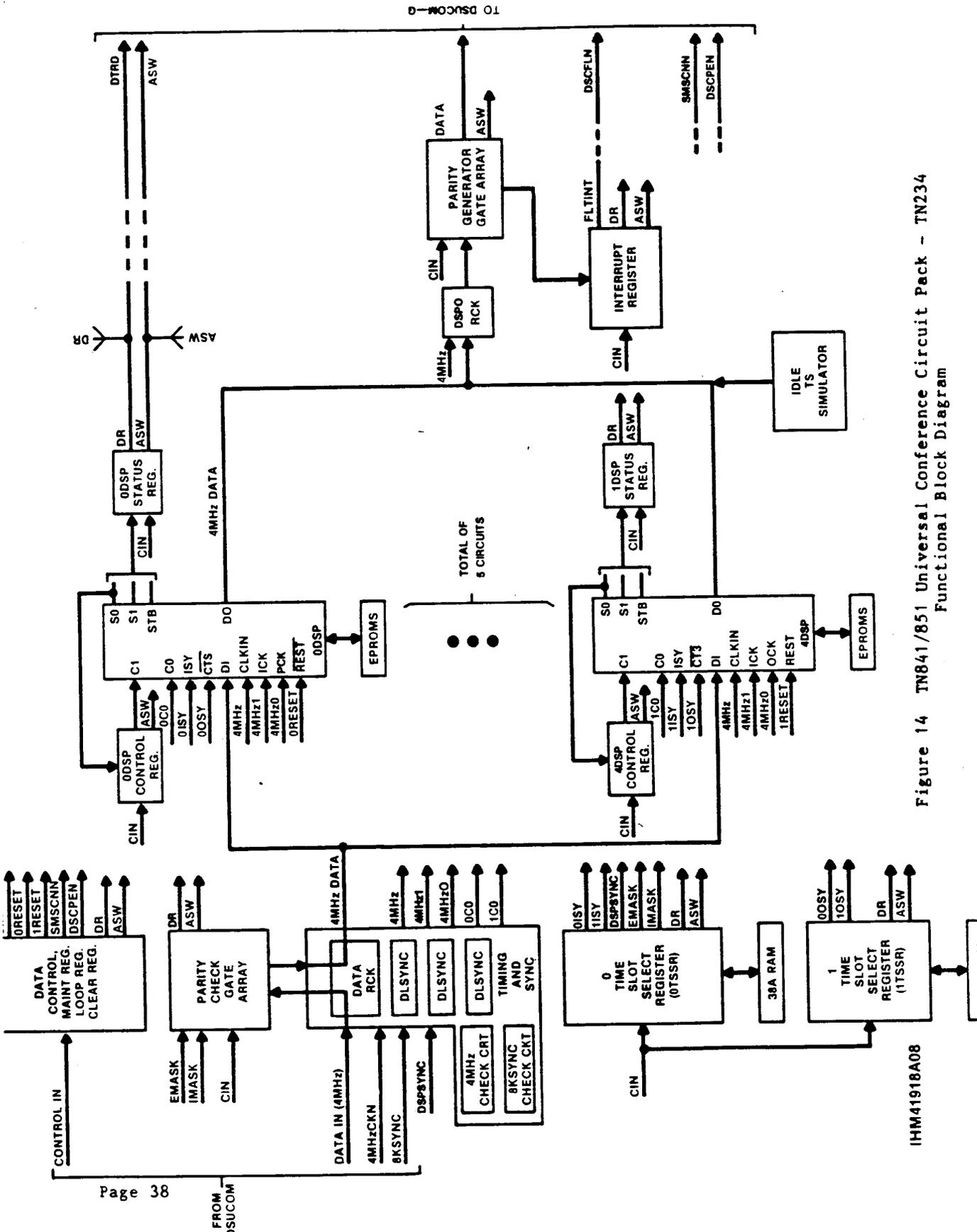
Figure 14 TN841/851 Universal Conference Circuit Pack - TN234
Functional Block Diagram

IHM41918A08

Figure 15 TN841/851 Conference Circuit Pack - TN 234
Time Slot Assignment Format

APPENDIX

GDSUEMNEM FILE
GLOBAL DSU EXPORT MNEMONIC
SD5X-201-01

+5V(0,1)DSCM	1,4/1	SERVICE GROUP 0 OR 1, +5V TO DSUCOM
+5V(0,1)DSC(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, +5V DIGITAL SERVICE CIRCUIT 0 - 7
-48RTN(0,1)	3,6/1	SERVICE GROUP 0 OR 1, -48V RETURN
-48V(0,1)	3,6/1	SERVICE GROUP 0 OR 1, -48 VOLTS
(0,1)ABUS(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY A-BUS LEADS 0 - 7
(0,1)ASW(0,1)0	2,5/1-8	SERVICE GROUP 0 OR 1, ALL SEMMS WELL 0 OR 1
(0,1)A(0-7)SEL0	1,4/1	SERVICE GROUP 0 OR 1, A0-A7 SELECT ADDRESS LINES
(0,1)BBUS(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY B-BUS LEADS 0 - 7
(0,1)B(0-7)SEL0	1,4/1	SERVICE GROUP 0 OR 1, B0-B7 SECLECT ADDRESS LINES
(0,1)CBUS(0-10)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY C-BUS LEADS 0-10
(0,1)CURPR(N,P)	1,4/1	SERVICE GROUP 0 OR 1, CURRENT PROGRAMMING RESISTOR (NEG,POS)
(0,1)C0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, PERIPHERAL SEQUENCER CLOCK FROM PERIPHERAL INTERFACE CONTROL BUS SIDE 0 (NEG,POS)
(0,1)C1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, PERIPHERAL SEQUENCER CLOCK FROM PERIPHERAL INTERFACE CONTROL BUS SIDE 1 (NEG,POS)
(0,1)DATIN(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, DATA TO DSUCOM FROM DIGITAL SERVICE CIRCUIT's 0 - 7
(0,1)DATOUT(0-7)	1,4/1	SERVICE GROUP 0 OR 1, DATA TO DIGITAL SERVICE CIRCUIT's 0 - 7 FROM DSUCOM
(0,1)DBUS(0-10)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY D-BUS LEADS 0 - 10

(0,1)DR	2,5/1-8	SERVICE GROUP 0 OR 1, SERIAL DATA READ
(0,1)DSCFL(0-7)0	2,5/1-8	SERVICE GROUP 0 OR 1, DIGITAL SERVICE CIRCUIT 0 - 7 FAULT REPORT
(0,1)DSCLK	1,4/1	SERVICE GROUP 0 OR 1, DATA SHIFT CLOCK
(0,1)DSCPE(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, DIGITAL SERVICE CIRCUIT 0 - 7 PARITY ERROR REPORT
(0,1)DW	1,4/1	SERVICE GROUP 0 OR 1, SERIAL DATA WRITE
(0,1)EBUS(0-4)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY E-BUS LEADS 0 - 4
(0,1)FBUS(0-4)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY F-BUS LEADS 0 - 4
(0,1)GBUS(0-3)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY G-BUS LEADS 0 - 3
(0,1)GRDSCM	1,4/1	SERVICE GROUP 0 OR 1, GROUP FOR DSUCOM
(0,1)HBUS(0-7)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY H-BUS LEAD 0 - 7
(0,1)IBUS(0-3)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY I-BUS LEADS 0 - 7
(0.1)ID0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, REPLY MESSAGE FROM PERIPHERAL SEQUENCER TO PERIPHERAL INTERFACE CONTROL BUS SIDE 0 (NEG,POS)
(0,1)ID1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, REPLY MESSAGE FROM PERIPHERAL SEQUENCER TO PERIPHERAL INTERFACE CONTROL BUS SIDE 1 (NEG,POS)
(0,1)JBUS(0-3)	2,5/1-8	SERVICE GROUP 0 OR 1, TRANSMISSION TEST FACILITY J-BUS LEADS 0 - 3
(0,1)NINT0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, INTERRUPT REQUEST ON PERIPHERAL INTERFACE CONTROL BUS SIDE 0 (NEG,POS)
(0,1)NINT1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, INTERRUPT REQUEST ON PERIPHERAL INTERFACE CONTROL BUS SIDE 1 (NEG,POS)
(0,1)(N,P)LAMP	1,4/1	SERVICE GROUP 0 OR 1, (NEG,POS) POWER CONVERTER OUT-OF-SERVICE LAMP
(0,1)OD0(N,P) ·	1,4/1	SERVICE GROUP 0 OR 1, MESSAGE FROM PERIPHERAL INTERFACE CONTROL BUS SIDE 0 TO PERIPHERAL SEQUENCER (NEG,POS)

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(0,1)OD1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, MESSAGE FROM PERIPHERAL INTERFACE CONTROL BUS SIDE 1 TO PERIPHERAL SEQUENCER (NEG,POS)
(0,1)PBI0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, PCM DATA TO PERIPHERAL INTERFACE DATA BUS SIDE 0 (NEG,POS)
(0,1)PBI1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, PCM DATA TO PERIPHERAL INTERFACE DATA BUS SIDE 1 (NEG,POS)
(0,1)PBO0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, PCM DATA FROM PERIPHERAL INTERFACE DATA BUS SIDE 0 (NEG,POS)
(0,1)PBO1(N,P)	1,4/1	SERVICE GOUP 0 OR 1, PCM DATA FROM PERIPHERAL INTERFACE DATA BUS SIDE 1 (NEG,POS)
(0,1)R(0,3)SEL0	1,4/1	SERVICE GROUP 0 OR 1, READ 0-3 SELECT LEADS
(0,1)SASC	3,6/1	SERVICE GROUP 0 OR 1, PRECISION VOLTAGE ADJUSTMENT
(0,1)SMSCN(0-7)0	2,5/1-8	SERVICE GROUP 0 OR 1, DIGITAL SERVICE CIRCUIT 0 - 7 SUMMARY SCAN REPORT
(0,1)S0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, CONTROLLER SELECT ON PERIPHERAL INTERFACE CONTROL BUS SIDE 0 (NEG,POS)
(0,1)S1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, CONTROLLER SELECT ON PERIPHERAL INTERFACE CONTROL BUS SIDE 1 (NEG,POS)
(0,1)S2S3	3,6/1	SERVICE GROUP 0 OR 1, POWER CONVERTER REMOTE START
(0,1)W(0,3)SEL0	1,4/1	SERVICE GROUP 0 OR 1, WRITE 0-3 SELECT LEADAS
(0,1)4MC0(N,P)	1,4/1	SERVICE GROUP 0 OR 1, 4MHZ CLK FROM PERIPHERAL INTERFACE DATA BUS SIDE 0 (NEG,POS)
(0,1)4MC1(N,P)	1,4/1	SERVICE GROUP 0 OR 1, 4MHZ CLK FROM PERIPHERAL INTERFACE DATA BUS SIDE 1 (NEG,POS)
(0,1)4MHZCK(0-7)	1,4/1	SERVICE GROUP 0 OR 1, 4MHZ CLK TO DIGITAL SERVICE CIRCUIT 0 - 7
(0,1)8KSNC(0-7)0	1,4/1	SERVICE GROUP 0 OR 1, 8K SYNC TO DIGITAL SERVICE CIRCUIT (0 - 7)

(0,1)8KS0(N,P)   1,4/1   SERVICE GROUP 0 OR 1, 8K SYNC FROM PERIPHERAL INTERFACE DATA BUS SIDE 0 (NEG,POS)

(0,1)8KS1(N,P)   1,4/1   SERVICE GROUP 0 OR 1, 8K SYNC FROM PERIPHERAL INTERFACE DATA BUS SIDE 1 (NEG,POS)

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